MiCOM P64x
(P642, P643 & P645)

Transformer Protection Relay

P64x/EN M/A62

Software Version	04
Hardware Suffix	J (P642) & K (P643/P645)

Technical Manual

Schneider Electric

Note: The technical manual for this device gives instructions for its installation, commissioning, and operation. However, the manual cannot cover all conceivable circumstances or include detailed information on all topics. In the event of questions or specific problems, do not take any action without proper authorization. Contact the appropriate Schneider Electric technical sales office and request the necessary information.

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SAFETY INFORMATION

CHAPTER SI

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1 INTRODUCTION

This guide and the relevant equipment documentation provide full information on safe handling, commissioning and testing of this equipment. This Safety Information section also includes reference to typical equipment label markings.

Documentation for equipment ordered from Schneider Electric is dispatched separately from manufactured goods and may not be received at the same time. Therefore this guide is provided to ensure that printed information which may be present on the equipment is fully understood by the recipient.

The technical data in this Safety Information section is typical only, see the technical data section of the relevant product publication(s) for data specific to a particular equipment.

WARNING **Before carrying out any work on the equipment the user should be familiar with the contents of this Safety Information section and the ratings on the equipment's rating label.**

Reference should be made to the external connection diagram before the equipment is installed, commissioned or serviced.

Language-specific, self-adhesive User Interface labels are provided in a bag for some equipment.

2 HEALTH AND SAFETY

The information in the Safety Information section of the equipment documentation is intended to ensure that equipment is properly installed and handled in order to maintain it in a safe condition.

It is assumed that everyone who will be associated with the equipment will be familiar with the contents of that Safety Information section, or this Safety Guide.

When electrical equipment is in operation, dangerous voltages will be present in certain parts of the equipment. Failure to observe warning notices, incorrect use, or improper use may endanger personnel and equipment and also cause personal injury or physical damage.

Before working in the terminal strip area, the equipment must be isolated.

Proper and safe operation of the equipment depends on appropriate shipping and handling, proper storage, installation and commissioning, and on careful operation, maintenance and servicing. For this reason only qualified personnel may work on or operate the equipment.

Qualified personnel are individuals who:

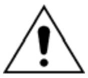
- Are familiar with the installation, commissioning, and operation of the equipment and of the system to which it is being connected;
- Are able to safely perform switching operations in accordance with accepted safety engineering practices and are authorized to energize and de-energize equipment and to isolate, ground, and label it;
- Are trained in the care and use of safety apparatus in accordance with safety engineering practices;
- Are trained in emergency procedures (first aid).

The equipment documentation gives instructions for its installation, commissioning, and operation. However, the manuals cannot cover all conceivable circumstances or include detailed information on all topics. In the event of questions or specific problems, do not take any action without proper authorization. Contact the appropriate Schneider Electric technical sales office and request the necessary information.

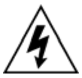
3 SYMBOLS AND LABELS ON THE EQUIPMENT

For safety reasons the following symbols and external labels, which may be used on the equipment or referred to in the equipment documentation, should be understood before the equipment is installed or commissioned.

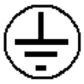
3.1 Symbols



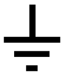
Caution: refer to equipment documentation



Caution: risk of electric shock



Protective Conductor (*Earth) terminal



Functional/Protective Conductor (*Earth) terminal

Note:	*This symbol may also be used for a Protective Conductor (Earth) Terminal if that terminal is part of a terminal block or sub-assembly e.g. power supply.*

***CAUTION: The term “Earth” used throughout this technical manual is the direct equivalent of the North American term “Ground”.**

3.2 Labels

See Safety Guide (SFTY/4L M) for typical equipment labeling information.

4 INSTALLING, COMMISSIONING AND SERVICING

Manual Handling

Plan carefully, identify any possible hazards and determine whether the load needs to be moved at all. Look at other ways of moving the load to avoid manual handling. Use the correct lifting techniques and Personal Protective Equipment to reduce the risk of injury.

Many injuries are caused by:

- Lifting heavy objects
- Lifting things incorrectly
- Pushing or pulling heavy objects
- Using the same muscles repetitively.

Follow the Health and Safety at Work, etc Act 1974, and the Management of Health and Safety at Work Regulations 1999.

Equipment Connections

Personnel undertaking installation, commissioning or servicing work for this equipment should be aware of the correct working procedures to ensure safety.

The equipment documentation should be consulted before installing, commissioning, or servicing the equipment.

Terminals exposed during installation, commissioning and maintenance may present a hazardous voltage unless the equipment is electrically isolated.

The clamping screws of all terminal block connectors, for field wiring, using M4 screws shall be tightened to a nominal torque of 1.3 Nm.

Equipment intended for rack or panel mounting is for use on a flat surface of a Type 1 enclosure, as defined by Underwriters Laboratories (UL).

Any disassembly of the equipment may expose parts at hazardous voltage, also electronic parts may be damaged if suitable ElectroStatic voltage Discharge (ESD) precautions are not taken.

If there is unlocked access to the rear of the equipment, care should be taken by all personnel to avoid electric shock or energy hazards.

Voltage and current connections shall be made using insulated crimp terminations to ensure that terminal block insulation requirements are maintained for safety.

Watchdog (self-monitoring) contacts are provided in numerical relays to indicate the health of the device. Schneider Electric strongly recommends that these contacts are hardwired into the substation's automation system, for alarm purposes.

To ensure that wires are correctly terminated the correct crimp terminal and tool for the wire size should be used.

The equipment must be connected in accordance with the appropriate connection diagram.

Protection Class I Equipment

- Before energizing the equipment it must be earthed using the protective conductor terminal, if provided, or the appropriate termination of the supply plug in the case of plug connected equipment.
- The protective conductor (earth) connection must not be removed since the protection against electric shock provided by the equipment would be lost.
- When the protective (earth) conductor terminal (PCT) is also used to terminate cable screens, etc., it is essential that the integrity of the protective (earth) conductor is checked after the addition or removal of such functional earth connections. For M4 stud PCTs the integrity of the protective (earth) connections should be ensured by use of a locknut or similar.

The recommended minimum protective conductor (earth) wire size is 2.5 mm² (3.3 mm² for North America) unless otherwise stated in the technical data section of the equipment documentation, or otherwise required by local or country wiring regulations.

The protective conductor (earth) connection must be low-inductance and as short as possible.

All connections to the equipment must have a defined potential. Connections that are pre-wired, but not used, should preferably be grounded when binary inputs and output relays are isolated. When binary inputs and output relays are connected to common potential, the pre-wired but unused connections should be connected to the common potential of the grouped connections.

Pre-Energization Checklist

Before energizing the equipment, the following should be checked:

- Voltage rating/polarity (rating label/equipment documentation);
- CT circuit rating (rating label) and integrity of connections;
- Protective fuse rating;
- Integrity of the protective conductor (earth) connection (where applicable);
- Voltage and current rating of external wiring, applicable to the application.

Accidental Touching of Exposed Terminals

If working in an area of restricted space, such as a cubicle, where there is a risk of electric shock due to accidental touching of terminals which do not comply with IP20 rating, then a suitable protective barrier should be provided.

Equipment Use

If the equipment is used in a manner not specified by the manufacturer, the protection provided by the equipment may be impaired.

Removal of the Equipment Front Panel/Cover

Removal of the equipment front panel/cover may expose hazardous live parts, which must not be touched until the electrical power is removed.

UL and CSA/CUL Listed or Recognized Equipment

To maintain UL and CSA/CUL Listing/Recognized status for North America the equipment should be installed using UL or CSA Listed or Recognized parts for the following items: connection cables, protective fuses/fuseholders or circuit breakers, insulation crimp terminals and replacement internal battery, as specified in the equipment documentation.

For external protective fuses a UL or CSA Listed fuse shall be used. The Listed type shall be a Class J time delay fuse, with a maximum current rating of 15 A and a minimum d.c. rating of 250 Vd.c., for example type AJT15.

Where UL or CSA Listing of the equipment is not required, a high rupture capacity (HRC) fuse type with a maximum current rating of 16 Amps and a minimum d.c. rating of 250 Vd.c. may be used, for example Red Spot type NIT or TIA.

Equipment Operating Conditions

The equipment should be operated within the specified electrical and environmental limits.

Current Transformer Circuits

Do not open the secondary circuit of a live CT since the high voltage produced may be lethal to personnel and could damage insulation. Generally, for safety, the secondary of the line CT must be shorted before opening any connections to it.

For most equipment with ring-terminal connections, the threaded terminal block for current transformer termination has automatic CT shorting on removal of the module. Therefore external shorting of the CTs may not be required, the equipment documentation should be checked to see if this applies.

For equipment with pin-terminal connections, the threaded terminal block for current transformer termination does NOT have automatic CT shorting on removal of the module.

External Resistors, including Voltage Dependent Resistors (VDRs)

Where external resistors, including Voltage Dependent Resistors (VDRs), are fitted to the equipment, these may present a risk of electric shock or burns, if touched.

Battery Replacement

Where internal batteries are fitted they should be replaced with the recommended type and be installed with the correct polarity to avoid possible damage to the equipment, buildings and persons.

Insulation and Dielectric Strength Testing

Insulation testing may leave capacitors charged up to a hazardous voltage. At the end of each part of the test, the voltage should be gradually reduced to zero, to discharge capacitors, before the test leads are disconnected.

Insertion of Modules and PCB Cards

Modules and PCB cards must not be inserted into or withdrawn from the equipment whilst it is energized, since this may result in damage.

Insertion and Withdrawal of Extender Cards

Extender cards are available for some equipment. If an extender card is used, this should not be inserted or withdrawn from the equipment whilst it is energized. This is to avoid possible shock or damage hazards. Hazardous live voltages may be accessible on the extender card.

External Test Blocks and Test Plugs

Great care should be taken when using external test blocks and test plugs such as the MMLG, MMLB and MiCOM P990 types, hazardous voltages may be accessible when using these. *CT shorting links must be in place before the insertion or removal of MMLB test plugs, to avoid potentially lethal voltages.

> **Note:* *When a MiCOM P992 Test Plug is inserted into the MiCOM P991 Test Block, the secondaries of the line CTs are automatically shorted, making them safe.*

Fiber Optic Communication

Where fiber optic communication devices are fitted, these should not be viewed directly. Optical power meters should be used to determine the operation or signal level of the device.

Cleaning

The equipment may be cleaned using a lint free cloth dampened with clean water, when no connections are energized. Contact fingers of test plugs are normally protected by petroleum jelly, which should not be removed.

5 DE-COMMISSIONING AND DISPOSAL

De-commissioning

The supply input (auxiliary) for the equipment may include capacitors across the supply or to earth. To avoid electric shock or energy hazards, after completely isolating the supplies to the equipment (both poles of any dc supply), the capacitors should be safely discharged via the external terminals prior to de-commissioning.

Disposal

It is recommended that incineration and disposal to water courses is avoided. The equipment should be disposed of in a safe manner. Any equipment containing batteries should have them removed before disposal, taking precautions to avoid short circuits. Particular regulations within the country of operation, may apply to the disposal of the equipment.

6 TECHNICAL SPECIFICATIONS FOR SAFETY

Unless otherwise stated in the equipment technical manual, the following data is applicable.

6.1 Protective Fuse Rating

The recommended maximum rating of the external protective fuse for equipments is 16A, High Rupture Capacity (HRC) Red Spot type NIT, or TIA, or equivalent. Unless otherwise stated in equipment technical manual, the following data is applicable. The protective fuse should be located as close to the unit as possible.

⚠ **DANGER** **CTs must NOT be fused since open circuiting them may produce lethal hazardous voltages.**

6.2 Protective Class

IEC 60255-27: 2005	Class I (unless otherwise specified in the equipment documentation).
EN 60255-27: 2005	This equipment requires a protective conductor (earth) connection to ensure user safety.

6.3 Installation Category

IEC 60255-27: 2005	Installation Category III (Overvoltage Category III)
EN 60255-27: 2005	Distribution level, fixed installation.
	Equipment in this category is qualification tested at 5 kV peak, 1.2/50 µs, 500 Ω, 0.5 J, between all supply circuits and earth and also between independent circuits.

6.4 Environment

The equipment is intended for indoor installation and use only. If it is required for use in an outdoor environment then it must be mounted in a specific cabinet of housing which will enable it to meet the requirements of IEC 60529 with the classification of degree of protection IP54 (dust and splashing water protected).

Pollution Degree	Pollution Degree 2 Compliance is demonstrated by reference to safety standards.
Altitude	Operation up to 2000m

INTRODUCTION

CHAPTER NO 1

Date:	12/2013
Hardware Suffix:	J (P642) K (P643/P645)
Software Version:	04
Connection Diagrams:	10P642xx (xx = 1 to 10) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9)

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1 MICOM DOCUMENTATION STRUCTURE

The manual provides a functional and technical description of the MiCOM protection relay and a comprehensive set of instructions for the relay’s use and application.

The chapter contents are summarized as follows.

1. Introduction **P64x/EN IT**

A guide to the MiCOM range of relays and the documentation structure. General safety aspects of handling Electronic Equipment is discussed with particular reference to relay safety symbols. Also a general functional overview of the relay and brief application summary is given.

2. Technical Data **P64x/EN TD**

Technical data including setting ranges, accuracy limits, recommended operating conditions, ratings and performance data. Compliance with norms and international standards is quoted where appropriate.

3. Getting Started **P64x/EN GS**

A guide to the different user interfaces of the protection relay describing how to start using it. This chapter provides detailed information regarding the communication interfaces of the relay, including a detailed description of how to access the settings database stored in the relay.

4. Settings **P64x/EN ST**

A list of all relay settings, including ranges, step sizes and defaults with a brief explanation of each setting.

5. Operation **P64x/EN OP**

A comprehensive and detailed functional description of all protection and non-protection functions.

6. Application Notes **P64x/EN AP**

This chapter includes a description of common power system applications of the relay, calculation of suitable settings, some typical worked examples, and how to apply the settings to the relay.

7. Programmable Logic **P64x/EN PL**

An overview of the Programmable Scheme Logic and a description of each logical node. This chapter includes the factory default (PSL) and an explanation of typical applications.

8. Measurements and Recording **P64x/EN MR**

A detailed description of the relays recording and measurements functions including the configuration of the event and disturbance recorder and measurement functions.

9. Firmware Design **P64x/EN FD**

An overview of the operation of the relay’s hardware and software. This chapter includes information on the self-checking features and diagnostics of the relay.

10. Commissioning **P64x/EN CM**

Instructions on how to commission the relay, comprising checks on the calibration and functionality of the relay.

11. Maintenance **Pxxx/EN MT**

A general maintenance policy for the relay is outlined.

12. Troubleshooting Pxxx/EN TS

Advice on how to recognize failure modes and the recommended course of action. Includes guidance on whom in Schneider Electric to contact for advice.

13. SCADA Communications P64x/EN SC

This chapter provides an overview regarding the SCADA communication interfaces of the relay. Detailed protocol mappings, semantics, profiles and interoperability tables are not provided in this manual. Separate documents are available for each protocol, downloadable from our website.

14. Symbols and Glossary Pxxx/EN SG

List of common technical abbreviations used in the product documentation.

15. Installation P64x/EN IN

Recommendations on unpacking, handling, inspection and storage of the relay. A guide to the mechanical and electrical installation of the relay is provided, incorporating earthing recommendations. All external wiring connections to the relay are shown.

16. Cyber Security Pxxx/EN CS

This chapter provides details of the Cyber Security features which are included with Software Version 03 only. Cyber Security features are not included in Software versions 01, 02 or 04.

17. Dual Redundant Ethernet Board (DREB) Pxxx/EN REB(U)

This chapter provides details of the dual redundant Ethernet board, which can be used to provide increased reliability for the system in which the relay is fitted.

18. Parallel Redundancy Protocol (PRP) Pxxx/EN PR

This chapter provides details of the Parallel Redundancy Protocol features which are included with Software Version 03V and 04X only.

19. Version History P64x/EN VH

History of all hardware and software releases for the product.

2 INTRODUCTION TO MICOM

MiCOM is a comprehensive solution capable of meeting all electricity supply requirements. It comprises a range of components, systems and services from Schneider Electric.

Central to the MiCOM concept is flexibility.

MiCOM allows you to define an application solution and integrate it with your power supply control system through extensive communication capabilities.

The components within MiCOM are:

- P range protection relays
- C range control products
- M range measurement products for accurate metering and monitoring
- S range versatile PC support and substation control packages

MiCOM products include extensive facilities for recording information on the state and behavior of the power system using disturbance and fault records. At regular intervals they can provide measurements of the system to a control center, allowing remote monitoring and control.

For up-to-date information on any MiCOM product, visit our website:

www.schneider-electric.com

3 PRODUCT SCOPE

The MiCOM P642, P643 and P645 preserves transformer service life by offering fast protection for transformer faults. Hosted on an advanced IED platform, the P64x incorporates differential, REF, thermal, and overfluxing protection, plus backup protection for uncleared external faults. Model variants cover two and three winding transformers (including autotransformers), with up to five sets of 3-phase CT inputs. Large CT counts are common in ring bus or mesh corner applications, where the P64x summates currents to create each total winding current, easing application of backup protection. Backup overcurrent can be directionalized, where the user includes the optional 3-phase VT input in their chosen model.

3.1 Functional Overview

The P642/P643/P645 transformer protection relays have a wide variety of protection functions which are summarized in the following table.

ANSII number	Description	P64x
87	Phase-segregated transformer biased differential protection is provided for high-speed discriminative protection for all fault types.	P642 / P643/ P645
64	Biased low-impedance restricted earth fault element can be used to provide high-speed earth fault protection. High impedance restricted earth fault element is also available. The 64 function is applicable to conventional transformers and autotransformers.	P642/ P643/ P645
50/51/67	Four overcurrent protection stages are provided which can be selected as non-directional, directional, forward or directional reverse. Stages 1 and 2 can be set as Inverse Definite Minimum Time (IDMT) or Definite Time (DT); stages 3 and 4 can be set as DT only.	P642/ P643/ P645
46OC	Four stages of negative phase sequence overcurrent protection are provided for remote back-up protection for both phase-to-earth and phase-to-phase faults. Each stage can be selected as non-directional, directional forward or directional reverse. Stages 1 and 2 can be set as Inverse Definite Minimum Time (IDMT) or Definite Time (DT); stages 3 and 4 can be set as DT only.	P642/ P643/ P645
49	Thermal overload protection based on IEEE Std C57.91-1995. Thermal trip can be based on either hot spot or top oil temperature, each with three time-delayed stages available. Four cooling modes are available to consider the transformer cooling classes.	P642/ P643/ P645
LoL	Two one-stage definite time delay alarms based on aging acceleration factor (F_{AA}) or Loss of Life (LoL) are available.	
Thru	Through faults are a major cause of transformer damage and failure. Both the insulation and the mechanical effects of fault currents are considered. A one-stage alarm is available for through-fault monitoring.	
50N/51N/67N	Up to three derived or measured standby earth fault elements are available. Four stages are provided which can be selected as non-directional, directional, forward or directional reverse. Stages 1 and 2 can be set as Inverse Definite Minimum Time (IDMT) or Definite Time (DT); stages 3 and 4 can be set as DT only	P642/ P643/ P645
59N	The 59N element is a two-stage design, each stage having separate voltage and time delay settings. Stage 1 can be set to operate on either an IDMT or DT characteristic, while stage 2 can be set to DT only.	P642/ P643/ P645
24	Two five-stage overfluxing (V/Hz) elements protect the transformer, against overexcitation. The first stage is a Definite Time alarm, the second stage can be used to provide an inverse or Definite Time trip characteristic and stages 3, 4 and 5 are Definite Time.	P642/ P643/ P645

ANSII number	Description	P64x
27	A two-stage undervoltage protection element, configurable as either phase-to-phase or phase-to-neutral measuring is available, Stage 1 can be set as either IDMT or DT and stage 2 is DT only. *Note* *Although the P642 has two VT inputs, one is used by V/Hz protection, and the other is used by the NPS Overvoltage and VCO protection. You can't use Overvoltage or Undervoltage protection using P642 units.*	P643/ P645
59	A two-stage overvoltage protection element, configurable as either phase-to-phase or phase-to-neutral measuring is available. Stage 1 can be set as either IDMT or DT and stage 2 is DT only. *Note* *Although the P642 has two VT inputs, one is used by V/Hz protection, and the other is used by the NPS Overvoltage and VCO protection. You can't use Overvoltage or Undervoltage protection using P642 units.*	P643/ P645
47	A one-stage negative phase sequence overvoltage protection element is available. It is DT only.	P642/ P643/ P645
81U/O	Four-stage Definite Time underfrequency and two-stage Definite Time overfrequency protection is provided for load shedding and back-up protection.	P642/ P643/ P645
RTD	Ten RTDs (PT100) are available to monitor the ambient and top oil temperature accurately. Each RTD has an instantaneous alarm and Definite Time trip stage.	Option P642/ P643/ P645
50BF	A two-stage circuit breaker failure function is provided with a 3-pole initiation input from external protection.	P642/ P643/ P645
37P	Phase undercurrent elements are available for use with, for example, the circuit breaker fail function.	P642/ P643/ P645
VTS	Voltage transformer supervision is provided (1, 2 & 3-phase fuse failure detection) to prevent mal-operation of voltage-dependent protection elements when a VT input signal is lost.	P642/ P643/ P645
CTS	Current transformer supervision prevents mal-operation of current-dependent protection elements when a CT input signal is lost.	P642/ P643/ P645
CLIO	Four analog or current loop inputs are provided for transducers such as vibration sensors and tachometers. Each input has a Definite Time trip and alarm stage, each input can be set to 'Over' or 'Under' operation, and each input can be independently selected as 0 to 1, 0 to 10, 0 to 20 or 4 to 20 mA. Four analogue (or current loop) outputs are provided for the analogue measurements in the relay. Each output can be independently selected as 0 to 1, 0 to 10, 0 to 20 or 4 to 20 mA.	Option P642/ P643/ P645
	CT saturation and no gap detection algorithms have been included to enhance to low set differential element operating time	
	External fault detection algorithm has bee included to maintain stability during external faults.	
	Zero crossing detection algorithm has been included to prevent circuit breaker failure mal-operations due to subsidence current.	
	Phase rotation. The rotation of the phases ABC or ACB for all 3-phase current and voltage channels can be selected. Also, for pumped storage applications, the swapping of two phases can be emulated independently for the 3-phase voltage and 3-phase current channels.	P642/ P643/ P645
	32 programmable user alarms	P642/ P643/ P645
	10 programmable function keys	P642/ P643/ P645
	18 programmable LEDs (tri-color P645, red P642 / P643)	P642/ P643/ P645
	8 to 24 digital inputs (order option) depending on the model	P642/ P643/ P645
	Front communication port (EIA(RS)232)	P642/ P643/ P645

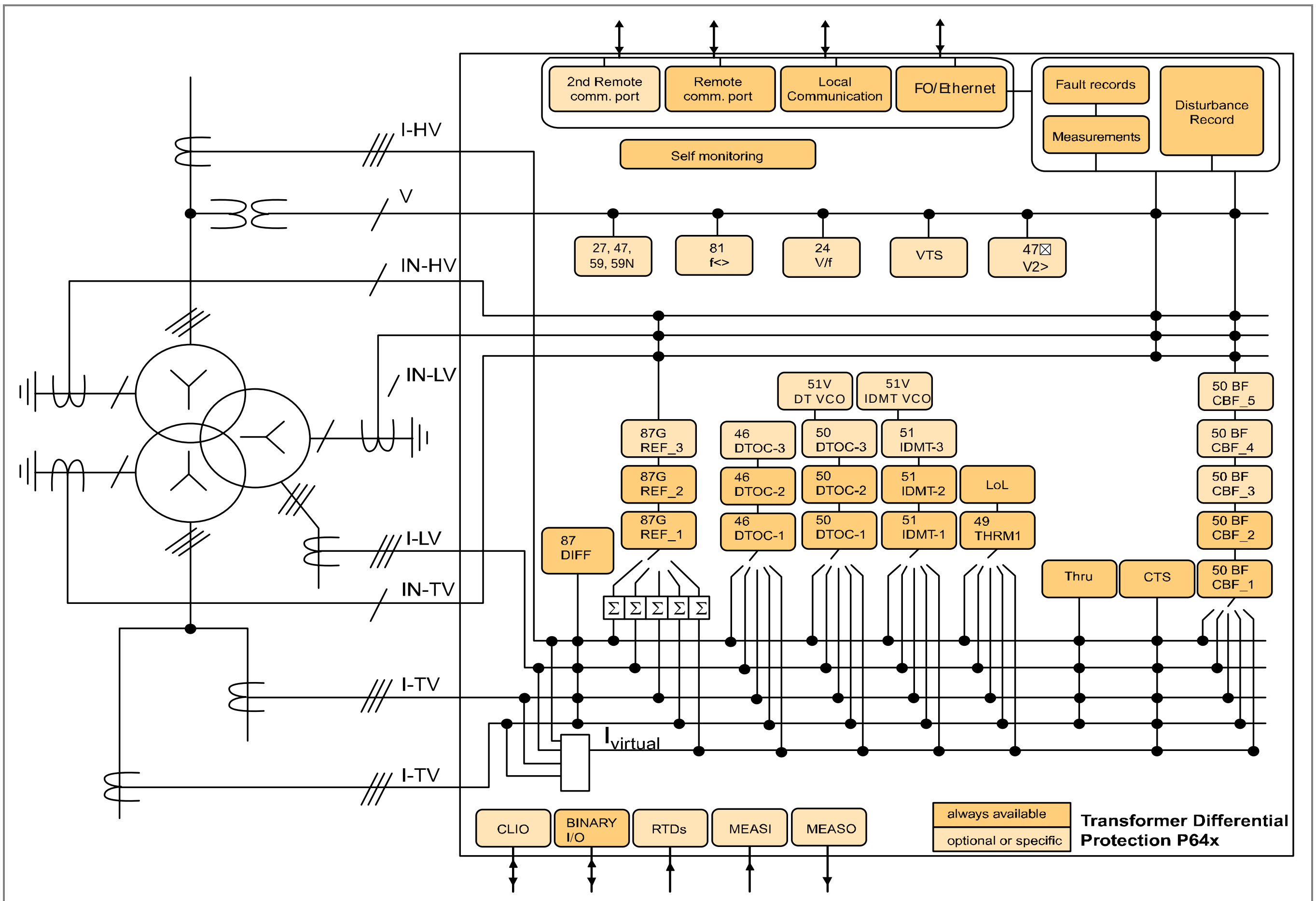
ANSII number	Description	P64x
	Rear communication port (K-Bus/EIA(RS)485). The following communications protocols are supported: Courier, MODBUS, IEC870-5-103 (VDEW), DNP3.0.	P642/ P643/ P645
	Rear communication port (Fiber Optic). The following communications protocols are supported: Courier, MODBUS, IEC870-5-103 (VDEW) and DNP3.0.	Option P642/ P643/ P645
	Second rear communication port, EIA(RS)232/EIA(RS)485. Courier, and K-Bus protocols.	Option P642/ P643/ P645
	Rear IEC 61850-8-1 Ethernet communication port.	Option P642/ P643/ P645
	Time synchronization port (IRIG-B)	Option P642/ P643/ P645

Table 1 - Protection functions overview

In addition to the functions in Table 1, the P64x supports these relay management functions:

- Measurement of all instantaneous & integrated values
- Trip circuit and coil supervision
- Four alternative setting groups
- Programmable function keys
- Control inputs
- Programmable scheme logic
- Programmable allocation of digital inputs and outputs
- Sequence of event recording
- Comprehensive disturbance recording (waveform capture)
- Fault recording
- Fully customizable menu texts
- Multi-level password protection
- Power-up diagnostics and continuous self-monitoring of the relay
- Commissioning test facilities
- Real time clock/time synchronization - time synchronization possible from IRIG-B input, opto input or communications

3.2 Application Overview


2nd Remote comm. port
Remote comm. port
Local Communication
FO/Ethernet
Fault records
Measurements
Disturbance Record
Self monitoring
I-HV
V
IN-HV
IN-LV
I-LV
IN-TV
I-TV
I-TV
27, 47, 59, 59N
81 f<>
24 V/f
VTS
47⊠ V2>
51V DT VCO
51V IDMT VCO
50 BF CBF_5
87G REF_3
46 DTOC-3
50 DTOC-3
51 IDMT-3
50 BF CBF_4
87G REF_2
46 DTOC-2
50 DTOC-2
51 IDMT-2
LoL
50 BF CBF_3
87 DIFF
87G REF_1
46 DTOC-1
50 DTOC-1
51 IDMT-1
49 THRM1
50 BF CBF_2
Thru
CTS
50 BF CBF_1
Σ Σ Σ Σ Σ
Ivirtual
CLIO
BINARY I/O
RTDs
MEASI
MEASO
always available
optional or specific
Transformer Differential Protection P64x
P4249ENg

1- The three-phase VT input is optional.
2- The 27, 59, 59N and VTS functions require the three-phase VT input.
3- The frequency required by the 81 function is obtained from any analog signal, but the voltage signals have priority over the current signals.

P4249ENg

Figure 1 - Functional diagram

3.3 Ordering Options

3.3.1 Information Required with Order - Software Version 04

Please see these sections:

- P642 Transformer Protection
- P643 Transformer Protection
- P645 Transformer Protection

3.3.2 P642 Transformer Protection

P642 Transformer Relay With Sigma-Delta Input Module	P642		1				M				J
Vx Aux Rating :											
24 - 48 Vdc		1									
48 - 110 Vdc		2									
110 - 250 Vdc (100 - 240 Vac)		3									
In/Vn Rating :											
HV-LV (In = 1A/5A), (Vn = 100/120V) (8CT/1VT)			1								
HV-LV (In = 1A/5A), (Vn = 100/120V) (8CT/2VT)			2								
Hardware Options :											
Standard - no options				1							
IRIG-B only (modulated)				2							
Fibre optic converter only				3							
IRIG-B (modulated) & fibre optic converter				4							
Ethernet with 100Mits/s fibre-optic port				6							
Second Rear Comms Port (Courier EIA232/EIA485/k-bus)				7							
Second Rear Comms Port + IRIG-B (modulated) (Courier EIA232/EIA485/k-bus)				8							
Ethernet (100Mbit/s) + IRIG-B (modulated)				A							
Ethernet (100Mbit/s) + IRIG-B (de-modulated)				B							
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Modulated IRIG-B				G							
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Un-modulated IRIG-B				H							
Redundant Ethernet RSTP, 2 multi-mode fibre ports + Modulated IRIG-B				J							
Redundant Ethernet RSTP, 2 multi-mode fibre ports + Un-modulated IRIG-B				K							
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Modulated IRIG-B				L							
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Un-modulated IRIG-B				M							
Redundant Ethernet Parallel Redundancy Protocol (PRP), 2 multimode fibre ports + Modulated IRIG-B				N							
Redundant Ethernet Parallel Redundancy Protocol (PRP), 2 multimode fibre ports + Un-modulated IRIG-B				P							
Product Specific Options :											
Size 8 (40TE) Case, 8 Optos + 8 Relays					A						
Size 8 (40TE) Case, 8 Optos + 8 Relays + RTD					B						
Size 8 (40TE) Case, 8 Optos + 8 Relays + CLIO (mA I/O)					C						
Size 8 (40TE) Case, 12 Optos + 12 Relays					D						
Size 8 (40TE) Case, 8 Optos + 12 Relays (including 4 High Break)					E						
Protocol Options :											
K-Bus/Courier						1					
Modbus						2					
IEC60870-5-103						3					
DNP3.0						4					
IEC 61850 over Ethernet and Courier via rear K-Bus/RS485						6					
DNP3.0 over Ethernet and Courier via rear K-Bus/RS485						8					
Mounting Options :											
Panel Mounting							M				
Language Options :											
English, French, German, Spanish								0			
English, French, German, Russian								5			
Chinese, English or French via HMI, with English or French only via Communications port								C			
Software Version Options :											
Unless specified the latest version will be delivered									* *		
Customisation :											
Default										8	
Customer Settings										9	
Design Suffix :											
Original											J

3.3.3 P643 Transformer Protection

P643 Transformer Relay With Sigma-Delta Input Module	P643 ☐ ☐ ☐ ☐ ☐ M ☐ ☐ ☐ K
Vx Aux Rating :	
24 - 48 Vdc	1
48 - 110 Vdc	2
110 - 250 Vdc (100 - 240 Vac)	3
In/Vn Rating :	
HV-LV In = 1A/5A, Vn = (100/120V) (12CT/1VT)	1
HV-LV In = 1A/5A, Vn = (100/120V) (12CT/4VT)	2
Hardware Options :	
Standard - no options	1
IRIG-B only (modulated)	2
Fibre optic converter only	3
IRIG-B (modulated) & fibre optic converter	4
Ethernet with 100Mits/s fibre-optic port	6
Second Rear Comms Port (Courier EIA232/EIA485/kbus)	7
Second Rear Comms Port + IRIG-B (modulated) (Courier EIA232/EIA485/kbus)	8
Ethernet (100Mbit/s) + IRIG-B (modulated)	A
Ethernet (100Mbit/s) + IRIG-B (de-modulated)	B
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Modulated IRIG-B	G
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Un-modulated IRIG-B	H
Redundant Ethernet RSTP, 2 multi-mode fibre ports + Modulated IRIG-B	J
Redundant Ethernet RSTP, 2 multi-mode fibre ports + Un-modulated IRIG-B	K
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Modulated IRIG-B	L
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Un-modulated IRIG-B	M
Redundant Ethernet Parallel Redundancy Protocol (PRP), 2 multimode fibre ports + Modulated IRIG-B	N
Redundant Ethernet Parallel Redundancy Protocol (PRP), 2 multimode fibre ports + Un-modulated IRIG-B	P
Product Specific Options :	
Size 12 (60TE) case, 16 optos + 16 relays	A
Size 12 (60TE) case, 16 optos + 16 relays + RTD	B
Size 12 (60TE) case, 16 optos + 16relays + CLIO (mA I/O)	C
Size 12 (60TE) case, 24 optos + 16 relays	D
Size 12 (60TE) case, 16 optos + 24 relays	E
Size 12 (60TE) case, 16 optos + 20 relays (including 4 High Break)	F
Protocol Options :	
K-Bus/Courier	1
Modbus	2
IEC60870-5-103	3
DNP3.0	4
IEC 61850 over Ethernet and Courier via rear K-Bus/RS485	6
DNP3.0 over Ethernet and Courier via rear K-Bus/RS485	8
Mounting Options :	
Panel Mounting	M
Language Options :	
English, French, German, Spanish	0
English, French, German, Russian	5
Chinese, English or French via HMI, with English or French only via Communications port	C
Software Version Options :	
Unless specified the latest version will be delivered	* *
Settings Files Options :	
Default	8
Customer Specific	9
Design Suffix :	
Extended Phase 2 CPU	K

3.3.4 P645 Transformer Protection

P645 Transformer Relay With Sigma-Delta Input Module	P645 ☐☐☐☐☐☐☐☐☐ K
Vx Aux Rating :	
24 - 48 Vdc	1
48 - 125 Vdc	2
110 - 250 Vdc (100 - 240 Vac)	3
In/Vn Rating :	
HV-LV In = 1A/5A, Vn = (100/120V) (18CT/1VT)	1
HV-LV In = 1A/5A, Vn = (100/120V) (18CT/4VT)	2
Hardware Options :	
Standard - no options	1
IRIG-B only (modulated)	2
Fibre optic converter only	3
IRIG-B (modulated) & fibre optic converter	4
Ethernet with 100Mits/s fibre-optic port	6
Second Rear Comms Port (Courier EIA232/EIA485/k-bus)	7
Second Rear Comms Port + IRIG-B (modulated) (Courier EIA232/EIA485/k-bus)	8
Ethernet (100Mbit/s) + IRIG-B (modulated)	A
Ethernet (100Mbit/s) + IRIG-B (de-modulated)	B
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Modulated IRIG-B	G
Redundant Ethernet Self-Healing Ring, 2 multi-mode fibre ports + Un-modulated IRIG-B	H
Redundant Ethernet RSTP, 2 multi-mode fibre ports + Modulated IRIG-B	J
Redundant Ethernet RSTP, 2 multi-mode fibre ports + Un-modulated IRIG-B	K
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Modulated IRIG-B	L
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + Un-modulated IRIG-B	M
Redundant Ethernet Parallel Redundancy Protocol (PRP), 2 multimode fibre ports + Modulated IRIG-B	N
Redundant Ethernet Parallel Redundancy Protocol (PRP), 2 multimode fibre ports + Un-modulated IRIG-B	P
Product Specific Options :	
Size 12 (60TE) case, 16 optos + 16 relays	A
Size 12 (60TE) case, 16 optos + 16 relays + RTD	B
Size 12 (60TE) case, 16 optos + 16 relays + CLIO (mA I/O)	C
Size 12 (60TE) case, 24 optos + 16 relays	D
Size 12 (60TE) case, 16 optos + 24 relays	E
Size 16 (80TE) case, 24 optos + 24 relays	F
Size 16 (80TE) case, 24 optos + 24 relays + RTD	G
Size 16 (80TE) case, 24 optos + 24 relays + CLIO (mA I/O)	H
Size 16 (80TE) case, 24 optos + 24 relays + RTD + CLIO (mA I/O)	J
Size 12 (60TE) case, 16 optos + 20 relays (including 4 high break)	K
Size 16 (80TE) case, 24 optos + 20 relays (including 4 high break)	L
Size 16 (80TE) case, 24 optos + 20 relays (including 4 high break) + RTD	M
Size 16 (80TE) case, 24 optos + 20 relays (including 4 high break) + CLIO (mA I/O)	N
Size 16 (80TE) case, 24 optos + 20 relays (including 4 high break) + RTD + CLIO (mA I/O)	P
Size 16 (80TE) case, 16 optos + 24 relays (including 8 high break)	Q
Size 16 (80TE) case, 16 optos + 24 relays (including 8 high break) + RTD	R
Size 16 (80TE) case, 16 optos + 24 relays (including 8 high break) + CLIO (mA I/O)	S
Size 16 (80TE) case, 16 optos + 24 relays (including 8 high break) + RTD + CLIO (mA I/O)	T
Protocol Options :	
K-Bus/Courier	1
Modbus	2
IEC60870-5-103	3
DNP3.0	4
IEC 61850 over Ethernet and Courier via rear K-Bus/RS485	6
DNP3.0 over Ethernet and Courier via rear K-Bus/RS485	8
Mounting Options :	
Panel Mounting	M
Rack Mounting	N
Language Options :	
English, French, German, Spanish	0
English, French, German, Russian	5

P645 Transformer Relay With Sigma-Delta Input Module	P645										K
Chinese, English or French via HMI, with English or French only via Communications port								C			
Software Version Options : Unless specified the latest version will be delivered									* *		
Settings Files Options : Default										8	
Customer Settings										9	
Design Suffix : Original											K

Notes:

TECHNICAL DATA

CHAPTER NO 2

Date:	12/2013
Hardware Suffix:	J (P642) K (P643/P645)
Software Version:	04
Connection Diagrams:	10P642xx (xx = 1 to 10) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9)

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Notes:

MECHANICAL SPECIFICATIONS

Design

Modular MiCOM Px40 platform relay, P642 in 40TE case, P643 in 60TE and P645 in 60TE or 80TE case. Mounting is front of panel flush mounting, or 19” rack mounted (ordering options).

Enclosure Protection

Per IEC 60529: 1992:

IP 52 Protection (front panel) against dust and dripping water.
IP 50 Protection for the rear and sides of the case against dust.
IP 10 Product safety protection for the rear due to live connections on the terminal block.

Weight

P642	(40TE):	7.9kg
P643	(60TE):	11.5kg
P645	(60TE):	11.5kg
P645	(80TE):	15.5kg

TERMINALS

AC Current and Voltage Measuring Inputs

Located on heavy duty (black) terminal block:
Threaded M4 terminals, for ring terminal connection.
CT inputs have integral safety shorting, upon removal of the terminal block.

General Input/Output Terminals

For power supply, opto inputs, output contacts and RP1 rear communications.
Located on general purpose (grey) blocks:
Threaded M4 terminals, for ring terminal connection.

Case Protective Earth Connection

Two rear stud connections, threaded M4.
Must be earthed (grounded) for safety, minimum earth wire size 2.5mm^2.

Front Port Serial PC Interface

EIA(RS)-232 DCE, 9 pin D-type female connector Socket SK1.
Courier protocol for interface to MiCOM S1 Studio software.
Isolation to ELV (Extra Low Voltage) level.
Maximum cable length 15m.

Front Download/Monitor Port

EIA(RS)-232, 25 pin D-type female connector Socket SK2.
For firmware and menu text downloads.
Isolation to ELV level.

Rear Communications Port (RP1)

EIA(RS)-485 signal levels, two wire connections located on general purpose block, M4 screw.
For screened twisted pair cable, multidrop, 1000 m max.
For Courier (K-Bus), IEC-60870-5-103, MODBUS or DNP3.0 protocol (ordering options).
Isolation to SELV (Safety Extra Low Voltage) level.

Optional Rear Fiber Connection for SCADA/DCS

BFOC 2.5 -(ST$^{\circledR}$)-interface for glass fiber, as for IEC 874-10.
850nm short-haul fibers, one Tx and one Rx. For Courier, IEC-60870-5-103, MODBUS or DNP3.0 (Ordering options).

Optional Second Rear Communications Port (RP2)

EIA(RS)-232, 9 pin D-type female connector, socket SK4.
Courier protocol: K-Bus, EIA(RS)-232, or EIA(RS)485 connection.
Isolation to SELV level.
Maximum cable length 15 m.

Optional Rear IRIG-B Interface (Modulated or Unmodulated)

BNC plug
Isolation to SELV level.
50 ohm coaxial cable.

Optional Rear Ethernet or Redundant Ethernet Connection for IEC 61850 or DNP3.0

10BaseT/100BaseTX Communications

Interface in accordance with IEEE802.3 and IEC 61850
Isolation: 1.5 kV
Connector type: RJ45
Cable type: Screened Twisted Pair (STP)
Max. cable length: 100 m

100Base FX Interface

Interface in accordance with IEEE802.3 and IEC 61850
Wavelength: 1300 nm
Fiber: multi-mode 50/125 µm or 62.5/125 µm
Connector type: BFOC 2.5 -(ST$^{\circledR}$)

RATINGS

AC Measuring Inputs

Nominal frequency: 50 and 60 Hz (settable)
Operating range: 45 to 66 Hz
Phase rotation ABC or ACB

AC Current

Nominal current (In): 1 and 5 A dual rated.
Nominal burden: Phase <0.2 VA at In
Earth <0.2 VA at In
Thermal withstand: continuous 4 In
for 10 s: 30 In
for 1 s; 100 In
Standard: linear to 64 In (non-offset AC current).

AC Voltage

Nominal voltage (Vn): 100 to 120 V
Nominal burden per phase:
< 0.06 VA at 110 V
Thermal withstand: continuous 2 Vn
for 10s: 2.6 Vn
Linear to 200V (100V/120V).

POWER SUPPLY

Auxiliary Voltage (Vx)

Three ordering options:
(i) Vx: 24 to 48 Vdc
(ii) Vx: 48 to 110 Vdc, and
40 to 100Vac (rms)
(iii) Vx: 110 to 250 Vdc, and
100 to 240Vac (rms)

Operating Range

(i) 19 to 65V (dc only for this variant)
(ii) 37 to 150V (dc), 32 to 110 V (ac)
(iii) 87 to 300V (dc), 80 to 265 V (ac).
With a tolerable ac ripple of up to 12% for a dc supply, as for IEC 60255-11: 1979.

Nominal Burden

Quiescent burden: 11W or 24 VA. (Extra 1.25 W when fitted with second rear communications board).
Additions for energized binary inputs/outputs:
For each opto input:
0.09 W (24 to 54 V)
0.12 W (110/125 V)
0.19 W (220/250 V)
For each energized output relay: 0.13W

Power-Up Time

Time to power up < 11 s.

Power Supply Interruption

As for IEC 60255-11: 1979:
The relay withstands a 20 ms interruption in the DC auxiliary supply, without de-energizing.
As for IEC 61000-4-11: 2004:
The relay withstands a 20 ms interruption in an AC auxiliary supply, without de-energizing.
A MiCOM E124 extends these limits. It is an auxiliary device used to provide energy to the trip coil of a circuit breaker.

Battery Backup

Front panel mounted
Type ½ AA, 3.6 V Lithium Thionyl Chloride (SAFT advanced battery reference LS14250)
Battery life (assuming relay energized for 90% time) >10 years

Field Voltage Output

Regulated 48 Vdc
Current limited at 112 mA maximum output
Operating range 40 to 60 V

Digital (“Opto”) Inputs

Universal opto inputs with programmable voltage thresholds (24/27, 30/34, 48/54, 110/125, 220/250 V). May be energized from the 48 V field voltage, or the external battery supply.
Rated nominal voltage: 24 to 250 Vdc
Operating range: 19 to 265 Vdc
Withstand: 300 Vdc, 300 Vrms.
Peak current of opto input when energized is 3.5 mA (0-300 V)
Nominal pick-up and reset thresholds:
Pick-up approx 70% of battery nominal set
Reset approx 66% of battery nominal set
Nominal battery 24/27: 60 - 80% DO/PU
(logic 0) <16.2 (logic 1) >19.2
Nominal battery 24/27: 50 - 70% DO/PU
(logic 0) <12.0 (logic 1) >16.8
Nominal battery 30/34: 60 - 80% DO/PU
(logic 0) <20.4 (logic 1) >24.0
Nominal battery 30/34: 50 - 70% DO/PU
(logic 0) <15.0 (logic 1) >21.0
Nominal battery 48/54: 60 - 80% DO/PU
(logic 0) <32.4 (logic 1) >38.4
Nominal battery 48/54: 50 - 70% DO/PU
(logic 0) <24.0 (logic 1) >33.6
Nominal battery 110/125: 60 - 80% DO/PU
(logic 0) <75.0 (logic 1) >88.0
Nominal battery 110/125: 50 - 70% DO/PU
(logic 0) <55.0 (logic 1) >77.0
Nominal battery 220/250: 60 - 80% DO/PU
(logic 0) <150.0 (logic 1) >176.0
Nominal battery 220/250: 50 - 70% DO/PU
(logic 0) <110 (logic 1) >154
Recognition time: 7 ms
<2 ms with long filter removed,
<12 ms with half cycle ac immunity filter on

OUTPUT CONTACTS

Standard Contacts

General purpose relay outputs for signaling, tripping and alarming:

Rated voltage: 300 V
Continuous current: 10 A
Short-duration current: 30 A for 3 s
Making capacity: 250 A for 30 ms
Breaking capacity:
DC: 50 W resistive
DC: 62.5 W inductive (L/R = 50 ms)
AC: 2500 VA resistive (cos ϕ = unity)
AC: 2500 VA inductive (cos ϕ = 0.7)
AC: 1250 VA inductive (cos ϕ = 0.5)
Subject to maxima of 10 A and 300 V
Response to command: < 5 ms
Durability:
Loaded contact: 10 000 operations minimum,
Unloaded contact: 100 000 operations minimum.

High Break Contacts

Relay outputs for tripping:

Rated voltage: 300 V
Continuous current: 10 A dc
Short-duration current: 30 A dc for 3 s
Making capacity: 250 A dc for 30 ms
Breaking capacity:
DC: 7500 W resistive
DC: 2500 W inductive (L/R = 50 ms)
Subject to maxima of 10 A and 300 V
Response to command: < 0.2 ms
Durability:
Loaded contact: 10 000 operations minimum,
Unloaded contact: 100 000 operations minimum.

Watchdog Contacts

Non-programmable contacts for relay healthy or relay fail indication:

Breaking capacity:
DC: 30 W resistive
DC: 15 W inductive (L/R = 40 ms)
AC: 375 VA inductive (cos ϕ = 0.7)

IRIG-B 12X Interface (Modulated)

External clock synchronization to IRIG standard 200-98, format B12x

Input impedance 6 kΩ at 1000 Hz
Modulation ratio: 3:1 to 6:1
Input signal, peak-peak: 200 mV to 20 V

IRIG-B B00X Interface (Un-Modulated)

External clock synchronization to IRIG standard 200-98, format B00X.

Input signal TTL level

Input impedance at dc 10 kΩ

ENVIRONMENTAL CONDITIONS

Ambient Temperature Range

As for EN 60088-2-1: 2007:
EN 60168-2-2: 2007
Operating temperature range:
-25°C to +55°C (or -13°F to +131°F)
Storage and transit:
-25°C to +70°C (or -13°F to +158°F)
Tested as per:
IEC 60068-2-1: 2007
-25°C storage (96 hours)
-40°C operation (96 hours)
IEC 60068-2-2: 2007
+85°C storage (96 hours)
+85°C operation (96 hours)

Ambient Humidity Range

As for EN 60078-2-78: 2002:
56 days at 93% relative humidity and +40 °C
As for IEC 60068-2-14: 2000
5 cycles, -25°C to +55 °C
1°C / min rate of change

Corrosive Environments

Per IEC 60068-2-60: 1995, Part 2, Test Ke, Method (class) 3
Industrial corrosive environment/poor environmental control, mixed gas flow test.
21 days at 75% relative humidity and +30^{o}C exposure to elevated concentrations of H_2S, (100 ppb) NO_2, (200 ppb) Cl_2 (20 ppb).
Per IEC 60068-2-52 Salt mist (7 days)
Per IEC 60068-2-43 for H_2S (21 days), 15 ppm
Per IEC 60068-2-42 for SO_2 (21 days), 25 ppm

TYPE TESTS

Insulation

As for IEC 60255-27: 2005
(incorporating corrigendum March 2007):
Insulation resistance > 100 MΩ at 500 Vdc
(Using only electronic/brushless insulation tester).

Creepage Distances and Clearances

IEC 60255-27: 2005
(incorporating corrigendum March 2007)
Pollution degree 3,
Overvoltage category III,
Impulse test voltage 5 kV.

High Voltage (Dielectric) Withstand

(EIA RS-232 ports excepted and normally- open contacts of output relays excepted).

(i) As for IEC 60255-27: 2005 (incorporating corrigendum March 2007), 2 kV rms AC, 1 minute:

Between terminals of all independent circuits.
Between all case terminals connected together, and the case earth (ground).
1 kV rms AC for 1 minute, across open watchdog contacts.
1 kV rms AC for 1 minute, across open contacts of changeover output relays.
1 kV rms AC for 1 minute for all D-type EIA(RS)-232 or EIA(RS)-485 ports between the communications port terminals and protective (earth) conductor terminal.

(ii) As for ANSI/IEEE C37.90-1989 (reaffirmed 1994):

1.5 kV rms AC for 1 minute, across open contacts of normally open output relays.
1k V rms AC for 1 minute, across open watchdog contacts.
1k V rms AC for 1 minute, across open contacts of changeover output relays.

Impulse Voltage Withstand Test

As for IEC 60255-27: 2005
(incorporating corrigendum March 2007):
Front time: 1.2 µs, Time to half-value: 50 µs,
Peak value: 5 kV, 0.5 J
Between all independent circuits.
Between all independent circuits and case earth ground).
EIA(RS)-232 & EIA(RS)-485 ports and normally open contacts of output relays excepted.

ELECTROMAGNETIC COMPATIBILITY (EMC)

1 MHz Burst High Frequency Disturbance Test

As for EN 60255-22-1: 2008, Class III,
Common-mode test voltage: 2.5 kV,
Differential test voltage: 1.0 kV,
Test duration: 2 s, Source impedance: 200 Ω
(EIA(RS)-232 ports excepted).

100 kHz Damped Oscillatory Test

EN 61000-4-18: 2007: Levels
Common mode test voltage: 2.5 kV
Differential mode test voltage: 1 kV

Immunity to Electrostatic Discharge

As for IEC 60255-22-2: 1997, Class 4,
15 kV discharge in air to user interface, display, communication ports and exposed metalwork.
8 kV point contact discharge in air to all communications ports.
6 kV point contact discharge to any part of the front of the product.

Electrical Fast Transient or Burst Requirements

As for IEC 60255-22-4: 2002 and EN61000-4-4:2004. Test severity Class III and IV:
Amplitude: 2 kV, burst frequency 5 kHz (Class III),
Amplitude: 4 kV, burst frequency 2.5 kHz (Class IV).
Applied directly to auxiliary supply, and applied to all other inputs. (EIA(RS)-232 ports excepted).
Amplitude: 4 kV, burst frequency 5 kHz
(Class IV) applied directly to auxiliary.

Surge Withstand Capability

As for IEEE/ANSI C37.90.1: 2002:
4 kV fast transient and 2.5 kV oscillatory applied directly across each output contact, optically isolated input, and power supply circuit.

Surge Immunity Test

(EIA(RS)-232 ports excepted).
As for IEC 61000-4-5: 2006 Level 4,
Time to half-value: 1.2 to 50 µs,
Amplitude: 4 kV between all groups and case earth (ground),
Amplitude: 2 kV between terminals of each group.

Conducted/Radiated Immunity

For RTDs used for tripping applications the conducted and radiated immunity performance is guaranteed only when using totally shielded RTD cables (twisted leads).

Immunity to Radiated Electromagnetic Energy

As for IEC 60255-22-3: 2001, Class III:
Test field strength,
frequency band 80 to 1000 MHz:
10 V/m,
Test using AM: 1 kHz / 80%,
Spot tests at 80, 160, 450, 900 MHz
As for IEEE/ANSI C37.90.2: 2004:
25, 80 MHz to 1000 MHz, zero and 100% square wave modulated, 1 kHz 80% am and am pulse modulated. Field strength 35 V/m.

Radiated Immunity from Digital Communications

As for EN61000-4-3: 2002, Level 4:
Test field strength, frequency band 800 to 960 MHz, and 1.4 to 2.0 GHz:
30 V/m,
Test using AM: 1 kHz/80%.

Radiated Immunity from Digital Radio Telephones

As for EN 61000-4-3: 2002:
10 V/m, 900 MHz and 1.89 GHz.

Immunity to Conducted Disturbances Induced by Radio Frequency Fields

As for EN 61000-4-6: 1996, Level 3,
Disturbing test voltage: 10 V.

Power Frequency Magnetic Field Immunity

As for EN 61000-4-8: 2001, Level 5,
100 A/m applied continuously,
1000 A/m applied for 3 s.
As for EN 61000-4-9: 2001, Level 5,
1000 A/m applied in all planes.
As for EN 61000-4-10: 2001, Level 5,
100 A/m applied in all planes at 100 kHz to 1 MHz with a burst duration of 2 s.

Conducted Emissions

As for EN 55022: 1998 Class A:
0.15 - 0.5 MHz, 79 dBμV (quasi peak)
66 dBμV (average)
0.5 - 30 MHz, 73 dBμV (quasi peak)
60 dBμV (average).

Radiated Emissions

As for EN 55022: 1998 Class A:
30 to 230 MHz, 40 dBμV/m at 10 m measurement distance
230 to 1 GHz, 47 dBμV/m at 10 m measurement distance.

EU DIRECTIVES

EMC Compliance

As for 2004/108/EC:
Compliance to the European Commission Directive on EMC is demonstrated using a Technical File. Product Specific Standards were used to establish conformity:
EN 50263: 2000

Product Safety

As for 2006/95/EC:
Compliance to the European Commission Low Voltage Directive. Compliance is demonstrated by reference to generic safety standards:
EN60255-27: 2005 (incorporating corrigendum March 2007)

R&TTE Compliance

Radio and Telecommunications Terminal Equipment (R & TTE) directive 99/5/EC.
Compliance demonstrated by compliance to both the EMC directive and the Low voltage directive, down to zero volts.
Applicable to rear communications ports.
Compliance demonstrated by Notified Body certificates of compliance.

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MECHANICAL ROBUSTNESS

Vibration Test

As for IEC 60255-21-1: 1996:
Response Class 2
Endurance Class 2

Shock and Bump

As for IEC 60255-21-2: 1996:
Shock response Class 2
Shock withstand Class 1
Bump Class 1

Seismic Test

As for IEC 60255-21-3: 1995:
Class 2

PROTECTION FUNCTIONS

Transformer Differential Protection

Accuracy

Pick-up: formula ±5%
Drop-off: 95% of formula ±5%
Pick-up and drop-off repeatability: <1%
Low set differential element operating time: <33 ms using normal contact, and <28 ms using high-break contact, for currents applied at 3x pickup level or greater
High set 1 differential element operating time: <15 ms for currents applied at 2x pickup level or greater
High set 2 differential element operating time: <25 ms for currents applied at 2x pickup level or greater
DT operating time: ±5% or <33 ms using normal contact, and <28 ms using high-break contact, for currents applied at 3x pickup level or greater
Operating time repeatability: < 2 ms Disengagement time: <15 ms

Circuitry Fault Alarm

Accuracy

Pick-up: formula ±5%
Drop-off: 0.95 of formula ±5%
Pick-up and drop-off repeatability: <4%
Instantaneous operating time: <26 ms at 2.5x pick-up value
Disengagement time: <26 ms
Operating time repeatability: <8 ms
Timer ±2% or 50 ms, whichever is greater
ID>1 Alarm Timer: ±2% or 50 ms whichever is greater

Low Impedance Restricted Earth Fault

Accuracy

Pick-up: formula ±5%
Drop-off: 0.90 × formula ±5%
Pick-up and drop-off repeatability <5%
Low impedance operating time: <45 ms for currents applied at 2x pickup level or greater
High impedance operating time: <30 ms
Low impedance DT operation: < 45 ms for currents applied at 2x pickup level or greater
Operating time repeatability: <5 ms
Disengagement time: <30 ms

High Impedance Restricted Earth Fault

Accuracy

Pick-up: formula ±5%
Drop-off: 0.90 × formula ±5%
Pick-up and drop-off repeatability <5%
High impedance operating time: <30 ms
Operating time repeatability: <5 ms
Disengagement time: <30 ms

Through Fault Monitoring

Accuracy

TF I> pick-up: setting ±5% or 50 mA whichever is greater
TF I> drop-off: 0.95 of setting ±5% or 50 mA whichever is greater
TF I^2t> pick-up: setting ±2% or $5A^2s$ whichever is greater

SYSTEM BACK-UP

Transient Overreach and Overshoot

Accuracy

Additional tolerance due to increasing X/R ratios: ±5% over X/R 1 to 120
Overshoot of overcurrent elements: <40 ms
Disengagement time <30 ms

Non-Directional/Directional Phase Sequence Overcurrent and Voltage Controlled Overcurrent

Accuracy

Pick-up: Setting ±5% or 20 mA whichever is greater
Drop-off: 0.95 x Setting ±5% or 20 mA whichever is greater
V_{VCO} pick-up: Setting ±5% or 50 mV whichever is greater
V_{VCO} drop-off: 0.95 × Setting ±5% or 50 mV whichever is greater
V_{POL} pick-up: Setting ±5% or 50 mV whichever is greater
V_{POL} drop-off: 0.95 × Setting ±5% or 50 mV whichever is greater
Pick-up and drop-off repeatability: <1%
Operating boundary pick-up: ±2% of RCA
Operating boundary hysteresis: <2°
Operating boundary repeatability: <2%
Instantaneous operating time: < 60ms
Disengagement time: <35ms
Operating time repeatability: <6 ms
Characteristic: UK curves: IEC 60255-3 - 1998
US curves: IEEEC37.112 - 1996

Negative Phase Sequence Overcurrent

Accuracy

I2>Pick-up: Setting ±5% or 20 mA, whichever is greater
I2> Drop-off: 0.95 x Setting ±5% or 20 mA, whichever is greater
Vpol Pick-up: Setting ±5% or 50 mV whichever is greater
Vpol Drop-off: 0.95 x Setting ±5% or 50 mV, whichever is greater
Pick-up and drop-off repeatability: <1%
Operating boundary pick-up: ±2° of RCA ±90°
Operating boundary hysteresis: < 2°
Operating boundary repeatability: <2%
DT operation: ±2% or 65 ms, whichever is greater
Instantaneous operating time: <65 ms
Disengagement time: <35 ms
Operating time repeatability: <6 ms
Characteristic:
UK curves: IEC 60255-3 - 1998
US curves: IEEEC37.112 - 1996

Thermal Overload

Accuracy

Hot Spot> Pick-up: Expected pick-up time ±5% or 50ms whichever is greater (expected pick-up time is the time required to reach the temperature setting)
Hot Spot> DT: ±5%or 50 ms whichever is greater
Top Oil> Pick-up: Expected Pick-up Time ±5% or 50ms whichever is greater (expected pick-up time is the time required to reach the temperature setting)
Top Oil> DT: ±5%or 50 ms whichever is greater
Repeatability: <2.5%

Non-Directional/Directional Earth Fault

Accuracy

Measured pick-up: Setting ±5% or 20mA whichever is greater
Measured drop-off: 95% × setting ±5% or 20mA whichever is greater
Derived pick-up: Setting ±5% or 20mA whichever is greater
Derived drop-off: 90% × setting ±5% or 20mA whichever is greater
Pick-up and drop-off repeatability: <1%
Vpol pick-up: Vpol ± 5% or 50mV whichever is greater
Vpol drop-off: 0.95 × Vpol ± 5% or 50mV whichever is greater
Operating boundary pick-up: ±2% of RCA
Operating boundary hysteresis: <1°
Operating boundary repeatability: <1%
Instantaneous operating time: < 60ms
Disengagement time: <35 ms
Operating time repeatability: <6 ms

2-Stage Neutral Displacement or Residual Overvoltage

Accuracy

Pick-up VN> ±5% or 50 mV whichever is greater
Drop-off: 0.95 x Setting ±5%
Pick-up and Drop-off Repeatability: <1%
IDMT shape: ±2% or 55 ms whichever is greater
DT operation: ±2% or 70 ms whichever is greater
Reset: <50 ms
Timer repeatability: <10 ms
Disengagement time <35 ms

Volts/Hz

Accuracy

Pick-up: V/Hz> ±5%
Drop-off: 98% of V/Hz> ±5%
Repeatability (operating threshold): <1%
IDMT operating time: ±5% or 50 ms whichever is greater
Definite time: ±2% or 50 ms whichever is greater
Instantaneous Operation: <50 ms
Disengagement time: <50 ms
Repeatability (operating times): <10 ms
V/Hz measurement: ±1%
Reset time: ±2% or 50 ms whichever is greater

2-Stage Undervoltage

Accuracy

Pick-up for DT and IDMT: Setting ±5%
Drop-off: 1.02 x Setting ±5%
IDMT shape: ±2% or 50 ms whichever is greater
DT operation: ±2% or 50 ms whichever is greater
Reset: <50 ms
Repeatability: <1%

2-Stage Overvoltage

Accuracy

DT Pick-up: Setting ±5%
IDMT Pick-up: Setting ±5%
Drop-off: 0.98 x Setting ±5%
IDMT characteristic shape: ±2% or 50 ms whichever is greater
DT operation: ±2% or 50 ms whichever is greater
Reset: <50 ms
Repeatability: <1%

1-Stage NPS Overvoltage

Accuracy

Pick-up: Setting ±5%
Drop-off: 0.95 x Setting ±5%
Repeatability (operating threshold): <1%
Instantaneous operating time (accelerated mode) <50 ms
Instantaneous operating time (normal mode) <60 ms
DT operation (accelerated mode): ±2% or 50 ms whichever is greater
DT operation (normal mode): ±2% or 100 ms whichever is greater
Disengagement time: <35 ms
Operating time repeatability: <52 ms

4-Stage Underfrequency

Accuracy

Pick-up: Setting ±0.01 Hz
Drop-off: (Setting +0.025 Hz) ±0.01 Hz
DT operation: ±2% or 70 ms whichever is greater.
Repeatability: <1%

The operation also includes a time for the relay to frequency track (20 Hz/second)

2-Stage Overfrequency

Accuracy

Pick-up: Setting ±0.01 Hz
Drop-off: (Setting -0.025 Hz) ±0.01 Hz
Repeatability: <1%
DT operation: ±2% or 70 ms whichever is greater.
The operation also includes a time for the relay to frequency track (20 Hz/second)

CB Fail

Accuracy

I < Pick-up:	110% of setting ±5% or 20 mA whichever is greater
I < Drop-off:	100% of setting ±5% or 20 mA whichever is greater
Pick-up and drop-off repeatability:	<1%
Timers:	±2% or 50 ms whichever is greater
Disengagement time:	<30ms
Reset time:	< 1 cycle fully offset current waveforms considered

Pole Dead

I > Pick-up:	Fixed Threshold (50 mA) ±20 mA
I > Drop-off:	Fixed Threshold (55 mA) ±20 mA
V< Pick-up:	Fixed Threshold (10 V) ±5%
V< Drop-off:	Fixed Threshold (30 V) ±5%
Instantaneous operation:	< 50 ms

SUPERVISION FUNCTIONS

Voltage Transformer Supervision (VTS)

Accuracy

VTS I> Pick-up: Setting ±5% or 50 mA whichever is greater
VTS I> Drop-off: 90% of setting ±5% or 50 mA whichever is greater
VTS I2> Pick-up: Setting ±5% or 50 mA whichever is greater
VTS I2> Drop-off: 95% of setting ±5% or 50 mA whichever is greater
P643/P645 models:
VTS V< Pick-up: Fixed Threshold (10 V) ±5%
VTS V< Drop-off: Fixed Threshold (30 V) ±5%
P642 model:
VTS V< Pick-up: Fixed Threshold (70 V) ±5%
VTS V< Drop-off: Fixed Threshold (95 V) ±5%
VTS V2> Pick-up: Fixed Threshold (10 V) ±5%
VTS V2> Drop-off: Fixed Threshold (9.5 V) ±5%
Pick-up and drop-off repeatability: <1%
Fast block operation: <25 ms
Fast block reset: <30 ms
Time delay: Setting ±2% or 50 ms whichever is greater

Differential Current Transformer Supervision (CTS)

Accuracy

CTS I1 Pick-up ratio: Setting ±5% or 20 mA whichever is greater
CTS I2/I1>1 Pick-up ratio: 95% of setting ±5% or 20 mA whichever is greater
CTS I2/I1>2 Pick-up ratio: 105% of setting ±5% or 20 mA whichever is greater
CTS I1 Drop-off ratio: 95% of setting ±5% or 20 mA whichever is greater
CTS I2/I1>1 Drop-off ratio: setting ±5% or 20 mA whichever is greater
CTS I2/I1>2 Drop-off ratio: setting ±5% or 20 mA whichever is greater
Pick-up and drop-off repeatability: <3%
Time delay operation: ±2% or 50 ms whichever is greater
CTS terminal block operation: <25 ms
CTS differential block operation < 30 ms
CTS reset < 25 ms
CTS Disengagement time <30 ms

PROGRAMMABLE SCHEME LOGIC

Accuracy

Output conditioner timer: Setting ±2% or 50 ms whichever is greater
Dwell conditioner timer: Setting ±2% or 50 ms whichever is greater
Pulse conditioner timer: Setting ±2% or 50 ms whichever is greater

MEASUREMENTS AND RECORDING FACILITIES

Measurements

Accuracy

Current: 0.05 to 3 In: ±1% or 3 mA of reading

Voltage: 0.05 to 2 Vn: ±1% of reading

Power (W): 0.2 to 2 Vn, 0.05 to 3 In: ±5% of reading at unity power factor

Reactive Power (VArs): 0.2 to 2 Vn, 0.05 to 3 In: ±5% of reading at zero power factor

Apparent Power (VA): 0.2 to 2 Vn, 0.05 to 3 In: ±5% of reading

Energy (Wh): 0.2 to 2 Vn, 0.2 to 3 In: ±5% of reading at zero power factor

Energy (Varh): 0.2 to 2 Vn, 0.2 to 3 In: ±5% of reading at zero power factor

Phase accuracy: 0° to 360: ±5%

Frequency: 5 to 70 Hz: ±0.025 Hz

IRIG-B and Real-Time Clock

Performance

Year 2000: Compliant

Real time accuracy: < ±1 second / day

External clock synchronisation: Conforms to IRIG standard 200-98, format B

Features

Real time 24 hour clock settable in hours, minutes and seconds

Calendar settable from January 1994 to December 2092

Clock and calendar maintained via battery after loss of auxiliary supply

Internal clock synchronization using IRIG-B Interface for IRIG-B signal is BNC

Current Loop Inputs and Outputs

Accuracy

Current loop input accuracy: ±1% of full scale

CLI drop-off threshold Under:
setting ±1% of full scale

CLI drop-off threshold Over:
setting ±1% of full scale

CLI sampling interval: 50 ms

CLI instantaneous operating time: < 200 ms for 20 Hz to 70 Hz; < 300 ms for 5 Hz to 20 Hz

CLI DT operating time: ±2% setting or 150 ms whichever is the greater for 20 Hz to 70 Hz;
±2% setting or 200 ms whichever is the greater for 5 Hz to 20 Hz

CLO conversion interval: 50 ms

CLO latency: < 1.07 s or <70 ms depending on CLO output parameter’s internal refresh rate - (1 s or 0.5 cycle)

Current loop output accuracy:
±0.5% of full scale

Repeatability: <5%

CLI - Current Loop Input

CLO - Current Loop Output

Other Specifications

CLI load resistance 0-1 mA: < 4 kΩ

CLI load resistance 0-1 mA/0-20 mA /4-20 mA: <300 Ω

Isolation between common input channels: zero

Isolation between input channels and case earth/other circuits: 2 kV rms for 1 minute

CLO compliance voltage 0-1 mA / 0 10 mA: 10 V

CLO compliance voltage 0-20 mA / 4-20 mA: 8.8 V

Current Loop output open circuit voltage: < 15 V

Disturbance Records

Accuracy

Magnitude and relative phases: ±5% of applied quantities

Duration: ±2%

Trigger Position: ±2% (minimum 100 ms)

Record length: 50 records each 1.5 s duration (75 s total memory) with 8 analog channels and 32 digital channels (Courier, MODBUS, DNP 3.0), 8 records each 3 s (50 Hz) or 2.5 s (60 Hz) duration (IEC60870-5-103).

Event, Fault and Maintenance Records

Maximum 512 events in a cyclic memory
Maximum 5 fault records
Maximum 10 maintenance records

Accuracy

Event time stamp resolution: 1 ms

IEC 61850 Ethernet Data

100 Base FX Interface

Transmitter Optical Characteristics
(TA = 0°C to 70°C, VCC = 4.75 V to 5.25 V)

Parameter	Sym	Min.	Typ.	Max.	Unit
Output Optical Power BOL 62.5/125 µm, NA = 0.275 Fiber EOL	PO	-19 -20	-16.8	-14	dBm avg.
Output Optical Power BOL 50/125 µm, NA = 0.20 Fiber EOL	PO	-22.5 -23.5	-20.3	-14	dBm avg.
Optical Extinction Ratio				10 -10	% dB
Output Optical Power at Logic “0” State	PO (“0”)			-45	dBm avg.
BOL - Beginning of life					
EOL - End of life					

Table 1 - Transmitter Optical Characteristics

Receiver Optical Characteristics
(TA = 0°C to 70°C, VCC = 4.75 V to 5.25 V)

Parameter	Sym	Min.	Typ.	Max.	Unit
Input Optical Power Minimum at Window Edge	PIN Min. (W)		-33.5	–31	dBm avg.
Input Optical Power Minimum at Eye Center	PIN Min. (C)		-34.5	-31.8	Bm avg.
Input Optical Power Maximum	PIN Max.	-14	-11.8		dBm avg.
Note	The 10BaseFL connection will no longer be supported as IEC 61850 does not specify this interface.				

Table 2 - Receiver Optical Characteristics

SETTINGS, MEASUREMENTS AND RECORDS LIST

Settings List

Global Settings (System Data)

Language: English / French / German / Spanish / Russian / Chinese
Frequency: 50/60 Hz

Date and Time

IRIG-B Sync: Disabled/Enabled
Battery Status: data
Battery Alarm: Disabled/Enabled
LocalTime Enable: Disabled/Fixed/Flexible
LocalTime Offset: -720 min…720 min
DST Enable: Disabled/Enabled
DST Offset: 30 min…60 min
DST Start: First / Second / Third / Fourth / Last
DST Start Day: Sun / Mon / Tues / Wed / Thurs / Fri / Sat
DST Start Month: Jan / Feb / Mar / Apr / May / Jun / Jul / Aug / Sept / Oct / Nov / Dec
DST Start Mins: 0 min…1425 min
DST End: First / Second / Third / Fourth / Last
DST End Day: Sun / Mon / Tues / Wed / Thurs / Fri / Sat
DST End Month: Jan / Feb / Mar / Apr / May / Jun / Jul / Aug / Sept / Oct / Nov / Dec
DST End Mins: 0 min…1425 min
RP1 Time Zone: UTC/Local
RP2 Time Zone: UTC/Local
Tunnel Time Zone: UTC/Local

Configuration

Restore Defaults: No Operation/All settings,
Setting Group 1,
Setting Group 2,
Setting Group 3,
Setting Group 4
Setting Group: Select from Menu
Select from Opto
Active Settings: Group 1/2/3/4
Save Changes: No Operation /
Save /
Abort
Copy From: Group 1/2/3/4
Copy To: Group 1/2/3/4
Setting Group 1: Disabled/Enabled
Setting Group 2: Disabled/Enabled
Setting Group 3: Disabled/Enabled
Setting Group 4: Disabled/Enabled
Diff Protection Disabled/Enabled
REF Protection Disabled/Enabled
Overcurrent Disabled/Enabled
NPS Overcurrent Disabled/Enabled
Thermal Overload Disabled/Enabled
Earth Fault Disabled/Enabled
Residual O/V NVD Disabled/Enabled
V/Hz Disabled/Enabled
Through Fault Disabled/Enabled
Volt Protection Disabled/Enabled
Freq Protection Disabled/Enabled
RTD Inputs Disabled/Enabled
CB Fail Disabled/Enabled
Supervision: Disabled/Enabled
Input Labels: Invisible/Visible
Output Labels: Invisible/Visible
RTD Labels: Invisible/Visible
CT & VT Ratios: Invisible/Visible
Record Control Invisible/Visible
Disturb Recorder: Invisible/Visible
Measure't Setup: Invisible/Visible
Comms Settings: Invisible/Visible
Commission Tests: Invisible/Visible
Setting Values: Primary/Secondary
Control Inputs: Invisible/Visible
CLIO Inputs: Disabled/Enabled
CLIO Outputs: Disabled/Enabled
Ctrl I/P Config: Invisible/Visible
Ctrl I/P Labels: Invisible/Visible
Direct Access: Disabled /
Enabled /
Hotkey
IEC GOOSE: Invisible/Visible
Function Keys: Invisible/Visible
LCD Contrast: 0…31

CT and VT Ratios

Main VT Location HV/LV/TV
Aux' VT Location HV/LV
Main VT Primary: 100...1 000 000 V
Main VT Secondary: 80...140 V (100/120 V) Aux'
VT Primary: 100...1 000 000 V
Aux' VT Secondary: 80...140 V (100/120 V)
T1 CT: CT Polarity
Standard/Inverted
CT Primary: 1 A…30 kA
CT Secondary: 1 A / 5 A
T2 CT: CT Polarity
Standard/Inverted
CT Primary: 1 A…30 KA
CT Secondary: 1 A / 5 A
T3 CT: CT Polarity
Standard/Inverted
CT Primary: 1 A…30 KA
CT Secondary: 1 A / 5 A
T4 CT: CT Polarity
Standard/Inverted
CT Primary: 1 A…30 KA
CT Secondary: 1 A / 5 A
T5 CT: CT Polarity
Standard/Inverted
CT Primary: 1 A…30 KA
CT Secondary: 1 A / 5 A
TN1 CT: CT Polarity
Standard/Inverted
CT Primary: 1 A…30 KA
CT Secondary: 1 A / 5 A
TN2 CT: CT Polarity
Standard/Inverted
CT Primary: 1 A…30 KA
CT Secondary: 1 A / 5 A
TN3 CT: CT Polarity
Standard/Inverted
CT Primary: 1 A…30 KA
CT Secondary: 1 A / 5 A

Sequence of Event Recorder (Record Control)

Clear Events: No/Yes
Clear Faults: No/Yes
Clear Maint: No/Yes
Alarm Event: Disabled/Enabled
Relay O/P Event: Disabled/Enabled
Opto Input Event: Disabled/Enabled
General Event: Disabled/Enabled
Fault Rec Event: Disabled/Enabled
Maint Rec Event: Disabled/Enabled
Protection Event: Disabled/Enabled
Clear Dist Recs: No/Yes
DDB 31 - 0: *(up to):*
DDB 2047 - 2016: Binary function link strings selects which DDB signals are stored as events and which are filtered out.

Oscillography (Disturbance Recorder)

Duration: 0.10…10.50 s
Trigger Position: 0.0…100.0%
Trigger Mode: Single/Extended
Analog Channel 1: *(up to):*
Analog Channel 30 (depending on model):

> Disturbance channels selected from:
> IA-1 / IB-1 / IC-1 / IN-1 / IA-2 / IB-2 / IC-2 / IN-2, etc (*depending on model)*

Digital Input 1: *(up to):*
Digital Input 32:
Selected binary channel assignment from any DDB status point in the relay such as opto input, output contact, alarms, starts, trips, controls, logic.
Input 1 Trigger: No Trigger /
(up to): Trigger L/H/
Input 32 Trigger: Trigger H/L
Notes L/H (Low to High)
H/L (High to Low)

Measured Operating Data (Measure't Setup)

Default Display: 3Ph + N Current,
3Ph Neutral Voltage,
Power,
Date and Time,
Description,
Plant
Reference,
Frequency or
Access Level
Local Values: Primary/Secondary
Remote Values: Primary/Secondary
Measurement Ref: Vx, VA, VB, VC, IA1, IB1, IC1, IA2, IB2, IC2, IA3, IB3, IC3, IA4, IB4, IC4, IA5, IB5, IC5, VAB or VBC
Measurement Mode: 0 / 1 / 2 / 3

Communications

RP2 Protocol: (data)
RP1 Address: (Courier or IEC870-5-103): 0…255
RP1 Address: *(DNP3.0):* 0…65534
RP1 Address: *(MODBUS):* 1…247
RP1 InactivTimer: 1…30 mins
RP1 Baud Rate: (IEC870-5-103):
9600/
19200/
38400 bits/s
RP1 Baud Rate: (MODBUS, Courier):
9600/
19200/
38400 bits/s
RP1 Baud Rate: *(DNP3.0):*
9600/
19200/
38400 bits/s
RP1 Parity: Odd/Even/None
(MODBUS, DNP3.0)
RP1 Meas Period: 1…60 s
(IEC870-5-103)
RP1 PhysicalLink: Copper (EIA(RS)-485 or K bus) or
Fiber Optic
RP1 Time Sync: Disabled/Enabled
MODBUS IEC Timer: Standard/Reverse
RP1 CS103Blocking: Disabled
Monitor Blocking
Command Blocking
RP1 Card Status: (data)
K-Bus OK
EIA485 OK
Fiber Optic OK (Courier)
RP1 Port Config: *(Courier):*
K Bus
EIA485 (RS485)
RP1 Comms Mode: *(Courier):*
IEC60870 FT1.2 IEC60870 10-bit, no parity
RP1 Baud Rate: 9600/
19200/
38400 bits/s

Note *If RP1 Port Config is K Bus the baudrate is fixed at 64 kbits/s*

DNP Need Time: 1…30 mins
DNP App Fragment: 100…2048 bytes
DNP App Timeout: 1…120 s
DNP SBO Timeout: 1…10 s
DNP Link Timeout: 0.1…60 s

Optional Ethernet or Redundant Ethernet Port

NIC Protocol: data
NIC MAC Address: data
NIC Tunl Timeout: 1...30 mins
NIC Link Report: Alarm, Event, None
NIC Link Timeout: 0.1...60 s

Optional Additional Second Rear Communication (Rear Port2 (RP2))

RP2 Protocol: (data)
RP2 Card Status: (data)
Unsupported,
Card not fitted,
EIA232 OK,
EIA485 OK
Kbus OK
RP2 Port Config: EIA(RS)-232
EIA(RS)-485
K-Bus
RP2 Comms Mode: IEC60870 FT1.2
IEC60870 10-bit,
no parity
RP2 Address: 0…255
RP2 InactivTimer: 1…30 mins
RP2 Baud Rate: 9600/
19200/
38400 bits/s

Note *If RP2 Port Config is K Bus the baud rate is fixed at 64 kbits/s*

DNP Need Time: 1…30 mins
DNP App Fragment: 100…2048 bytes
DNP App Timeout: 1…120 s
DNP SBO Timeout: 1…10 s

Commission Tests

Opto I/P Status: (data) indicates the status of the opt-inputs.
Rly O/P Status: (data) indicates the status of the output relays.
Test Port Status: (data) indicates the status of monitor bits 1 to 8.
Monitor bit 1: Binary function link
(up to): strings, selecting which
Monitor bit 8: DDB signals have their status visible in the Commissioning menu, for test purposes
Test Mode: Disabled
Test Mode
Blocked Contacts
Test Pattern: Configuration of which output contacts are to be energized when the contact test is applied

Opto Coupled Binary Inputs (Opto Config)

Global Nominal V: 24 – 27 V
30 – 34 V
48 – 54 V
110 – 125 V
220 – 250 V
Custom Opto Input 1:
(up to):
Opto Input #. (# = max. opto no. fitted):
Custom options allow independent thresholds to be set for each opto, from thesame range as above.
Opto Filter Control: Binary function link string, selecting which optos have an extra 1/2 cycle noise filter, and which do not.
Characteristics: Standard 60% - 80%
50% - 70%

Control Inputs into PSL (Ctrl. I/P Config.)

Hotkey Enabled: Binary function link string, selecting which of the control inputs are driven from Hotkeys.
Control Input 1: Latched/Pulsed
(up to):
Control Input 32:
Ctrl Command 1: ON/OFF
(up to): SET/RESET
Ctrl Command 32: IN/OUT
ENABLED/DISABLED

Function Keys

Fn. Key Status 1: Disable
(up to): Lock
Fn. Key Status 10 Unlock/Enable
Fn. Key 1 Mode: Toggled/Normal
(up to):
Fn. Key 10 Mode:
Fn. Key 1 Label: User defined text string
(up to): to describe the function
Fn. Key 10 Label: of the particular function key

IED Configurator

Switch Conf. Bank: No Action/ Switch Banks

IEC 61850 GOOSE

GoEna: Disabled/ Enabled
Test Mode: Disabled/ Pass Through/ Forced
VOP Test Pattern: 0x00000000... 0xFFFFFFFF
Ignore Test Flag: No/ Yes

Control Input User Labels

(Ctrl. I/P Labels)

Control Input 1:
(up to):
Control Input 32: User defined text string to describe the function of the particular control input

Settings in Multiple Groups

Note All settings here onwards apply for setting groups # = 1 to 4.

PROTECTION FUNCTIONS

System Config

Winding Config: HV+LV+TV, HV+LV
Winding Type: Conventional/Auto
HV CT Terminals: 00001
LV CT Terminals: 10000
TV CT Terminals: 00100
Ref power S: 100kVA to 5GVA
HV Connection: D-Delta / Y-Wye / Z-Zigzag
HV Grounding: Grounded/Ungrounded
HV Nominal: 100 V to 100 MV
HV Rating: 100 KVA to 5 GVA
Reactance: 1.00% to 100.00%
LV Vector Group: 0 to 11
LV Connection: D-Delta / Y-Wye / Z-Zigzag
LV Grounding: Grounded/Ungrounded
LV Nominal: 100 V to 100 MV
LV Rating: 100 kVA to 5 GVA
TV Vector Group: 0 to 11
TV Connection: D-Delta / Y-Wye / Z-Zigzag
TV Grounding: Grounded/Ungrounded
TV Nominal: 100 V to 100 MV
TV Rating: 100 kVA to 5 GVA
Match Factor CT1: 0.05 to 20
Match Factor CT2: 0.05 to 20
Match Factor CT3: 0.05 to 20
Match Factor CT4: 0.05 to 20
Match Factor CT5: 0.05 to 20
Phase Sequence: Standard ABC / Reverse ACB
VT Reversal: No Swap / A-B Swapped / B-C Swapped / C-A Swapped
CT1 Reversal: No Swap / A-B Swapped / B-C Swapped / C-A Swapped
CT2 Reversal: No Swap / A-B Swapped / B-C Swapped / C-A Swapped
CT3 Reversal: No Swap / A-B Swapped / B-C Swapped / C-A Swapped
CT4 Reversal: No Swap / A-B Swapped / B-C Swapped / C-A Swapped
CT5 Reversal: No Swap / A-B Swapped / B-C Swapped / C-A Swapped

Differential Protection

Trans Diff: Enabled/Disabled
Set Mode: Simple/Advance
Is1: 100.0e-3 to 2.500 PU
K1: 0 to 150.0%
Is2: 100.0e-3 to 10 PU
K2: 15 to 150.00%
tDIFF LS: 0 to 10.00 s
Is-CTS: 100.0e-3 to 2.500 PU
Is-HS1: 2.500 to 32.00 PU
H2S status: Enabled/Disabled
Is-HS2: 2.500 to 32.00 PU
Zero seq filt HV: Enabled/Disabled
Zero seq filt LV: Enabled/Disabled
Zero seq filt TV: Enabled/Disabled
2nd harmonic blocked: Enabled/Disabled
Ih(2)%>: 5.000 to 50.000%
Cross blocking: Enabled/Disabled
CTSat and NoGap: Enabled/Disabled
5th harm blocked: Enabled/Disabled
Ih(5)%>: 0 to 100.00%
Circuitry Fail: Enabled/Disabled
Is-cctfail>: 30.00e-3 to 1.000 PU
K-cctfail: 0 to 50.00%
tls-cctfail>: 0 to 10.00 s

REF Protection

REF HV status: LowZ REF/
HighZ REF/Disabled
HV CT input: TN1
HV IS1 Set: 6.00 to 300.00 A
HV IS2 Set: 30.00 to 3000.00 A
HV IREF K1: 0 to 150.0%
HV IREF K2: 15.00 to 150.0%
HV tREF: 0 to 10.00 s
REF LV status: LowZ REF/
HighZ REF/Disabled
LV CT input: TN2
LV IS1 Set: 6.00 to 300.00 A
LV IS2 Set: 30.00 to 3000.00 A
LV IREF K1: 0 to 150.0%
LV IREF K2: 15.00 to 150.0%
LV tREF: 0 to 10.00 s
REF TV status: LowZ REF/
HighZ REF/Disabled
TV CT input: TN3
TV IS1 Set: 6.00 to 300.00 A
TV IS2 Set: 30.00 to 3000.00 A
TV IREF K1: 0 to 150.0%
TV IREF K2: 15.00 to 150.0%
TV tREF: 0 to 10.00 s
REF Auto status: LowZ REF/
HighZ REF/Disabled
Auto CT input: TN1
Auto IS1 Set: 6.00 to 300.00 A
Auto IS2 Set: 30.00 to 3000.00 A
Auto IREF K1: 0 to 150.0%
Auto IREF K2: 15.00 to 150.0%
TV tREF: 0 to 10.00 s

NPS Overcurrent

NPS O/C 1: T1/T2/T3/T4/T5/
HV winding/
LV winding/
TV winding
I2>1 Status: Disabled/Enabled
I2>1 Char: DT
IEC S Inverse
IEC V Inverse
IEC E Inverse
UK LT Inverse
UK Rectifier
RI
IEEE M Inverse
IEEE V Inverse
IEEE E Inverse
US Inverse
US ST Inverse
I2>1 Directional: Non-directional, Directional
Fwd, Directional Rev
I2>1 Current Set: 0.08 to 4.00 In
I2>1 Time Delay: 0.00 to 100.00 s
I2>1 TMS: 0.025 to 1.200
I2>1 Time Dial: 0.01 to 100.00
I2>1 K (RI): 0.10 to10.00
I2>1 Reset Char: DT/Inverse
I2>1 tRESET: 0.00 to 100.00 s
I2>2 the same as I2>1
I2>3 Status: Disabled/Enabled
I2>3 Directional: Non-directional, Directional
Fwd, Directional Rev
I2>3 Current Set: 0.08 to 4.00 In
I2>3 Time Delay: 0.00 to 100.00 s
I2>4 the same as I2>3
I2> VTS Blocking: 1111
I2> V2pol Set: 0.5 to 25V
I2> Char Angle: -95° to 95°
NPS O/C 2 and NPS O/C 3 same as NPS O/C 1

Phase Overcurrent

Overcurrent1: T1/T2/T3/T4/T5/
HV winding/
LV winding/
TV winding
I>1 Status: Enabled/Disabled
I> 1 Char: DT
IEC S Inverse
IEC V Inverse
IEC E Inverse
UK LT Inverse
UK Rectifier
RI
IEEE M Inverse
IEEE V Inverse
IEEE E Inverse
US Inverse
US ST Inverse

I>1 Direction: Non-directional, Directional Fwd, Directional Rev
I>1 Current Set: 0.08 to 4.00 In
I>1 Time Delay: 0.00 to 100.00 s
I>1 TMS: 0.025 to 1.200
I>1 Time Dial: 0.01 to 100.00
I>1 K (RI): 0.10 to10.00
I>1 Reset Char: DT/Inverse
I>1 tRESET: 0.00 to 100.00 s
I>2 the same as I>1
I>3 Status: Disabled/Enabled
I>3 Direction: Non-directional, Directional Fwd, Directional Rev
I>3 Current Set: 0.08 to 32.00 In
I>3 Time Delay: 0.00 to 100.00 s
I>4 the same as I>3
I> Char Angle: -95° to 95°
I> Function Link: 1111
Overcurrent2 and Overcurrent3 the same as Overcurrent1

V Controlled O/C

VCO>1: T1/T2/T3/T4/T5/
HV winding/
LV winding/
TV winding
VCO>1 Char: DT
IEC S Inverse
IEC V Inverse
IEC E Inverse
UK LT Inverse
UK Rectifier
RI
IEEE M Inverse
IEEE V Inverse
IEEE E Inverse
US Inverse
US ST Inverse
VCO>1 Direction: Non-directional, Directional Fwd, Directional Rev
VCO>1 Curr' Set: 0.08 to 4.00 In
VCO>1 Time Delay: 0.00 to 100.00 s
VCO>1 TMS: 0.025 to 1.200
VCO>1 Time Dial: 0.01 to 100.00
VCO>1 K (RI): 0.10 to10.00
VCO>1 Reset Char: DT/Inverse
VCO>1 tRESET: 0.00 to 100.00 s
VCO>1 Angle: -95° to 95°
VCO>1 V<Setting: 5 V to 120.00 V
VCO>1 K Setting: 0.1 to 1
VCO>2 the same as VCO>1

Thermal Overload

Mon't Winding: HV/LV/TV/ Biased Current
Ambient T: RTD1 / RTD2 / RTD3 / RTD4 / RTD5 / RTD5 / RTD7 / RTD8 / RTD9 / RTD10 / AVERAGE / CLIO1 / CLIO2 / CLIO3 / CLIO4
Amb CLIO Type: 0-1 / 0-10 / 0-20 / 4-20 mA
Amb CLIO Min: -9999 to +9999
Amb CLIO Max: -9999 to +9999
Average Amb T: -25.00 to +75.00 Cel
Top Oil T: RTD1 / RTD2 / RTD3 / RTD4 / RTD5 / RTD5 / RTD7 / RTD8 / RTD9 / RTD10 / CALCULATED / CLIO1 / CLIO2 / CLIO3 / CLIO4
Top Oil CLIO Typ: 0-1 / 0-10 / 0-20 / 4-20 mA
Top Oil CLIO Min: -9999 to +9999
Top Oil CLIO Max: -9999 to +9999
IB: 0.1 to 4.0 PU
Rated NoLoadLoss: 0.1 to 100
Hot Spot overtop: 0.1 to 200.0 Cel
Top Oil overamb: 0.1 to 200.0 Cel
Cooling mode: Cooling mode 1 / Cooling mode 2 / Cooling mode 3 / Cooling mode 4 / Select Via PSL
Cooling Status: (data) Cooling mode 1 / Cooling mode 2 / Cooling mode 3 / Cooling mode 4
Cooling mode 1
Winding exp m: 0.01 to 2.0
Oil exp n: 0.01 to 2.0
Cooling mode 2, Cooling mode 3 and Cooling mode 4 same as Cooling mode 1
Hot spot rise co: 0.01 to 20.0 min
Top oil rise co: 1.0 to 1000.0 min
TOL Status: Enabled/Disabled
Hot Spot>1 to 3 Set: 1.0 to 300.0 Cel
tHot Spot>1 to 3 Set: 0 to 60 k min
Top Oil>1 to 3 Set: 1.0 to 300.0 Cel
tTop Oil>1 to 3 Set: 0 to 60k min
tPre-trip Set: 0 to 60 k min
LOL Status: Enabled/Disabled
Life Hours at HS: 1 to 300 000 hr
Designed HS temp: 1 to 200.0 Cel
Constant B Set: 1 to 100 000
FAA> Set: 0.1 to 30
tFAA> Set: 0 to 60 k min
LOL>1 Set: 0.1 to 300 000hr
tLOL> Set: 0 to 60 k min
Rst Life Hours: 0 to 300 000 hr

4-Stage Directional Earth Fault

Earth Fault 1: Enabled, Disabled
EF 1 Input: Measured / Derived
EF 1 Derived: (data) T1/T2/T3/T4/T5/
HV winding/
LV winding/
TV winding
EF 1 Measured: (data) TN1/TN2/TN3
IN>1 Status: Enabled/Disabled
IN>1 Char: DT
IEC S Inverse
IEC V Inverse
IEC E Inverse
UK LT Inverse
RI
IEEE M Inverse
IEEE V Inverse
IEEE E Inverse
US Inverse
US ST Inverse
IDG
IN>1 Direction: Non-directional, Directional Fwd, Directional Rev
IN>1 Current: 0.08 to 4 In
IN>1 IDG Is: 1 to 4 In
IN>1 Time Delay: 0.00 to 200.0 s
IN>1 TMS: 0.025 to 1.200
IN>1 Time Dial: 0.01 to 100.00
IN>1 K(RI): 0.1 to 10.00
IN>1 IDG Time: 1 to 2.00
IN>1 Reset Char: DT, Inverse
IN>1 tRESET: 0.00 to 100.00 s
IN>2 same as IN>1
IN>3 Status: Disabled, DT
IN>3 Current: 0.08 to 32.00 In
IN>3 Time Delay: 0.00 to 200.00 s
IN>4 same as IN>3
Earth fault 2 and Earth fault 3 same as Earth fault 1

The IDG curve is commonly used for time delayed earth fault protection in the Swedish market. This curve is available in stage 1 of the Earth Fault protection.
The IDG curve is represented by:

$$t = 5.8 - 1.35 \log_e \left(\frac{I}{IN > \text{Setting}} \right) \text{ in seconds}$$

Where:
I = Measured current
IN>Setting = An adjustable setting which defines the start point of the characteristic

Although the start point of the characteristic is defined by the “IN>” setting, the actual relay current threshold is a different setting called “IDG Is”. The “IDG Is” setting is set as a multiple of “IN>”.
An additional setting “IDG Time” is also used to set the minimum operating time at high levels of fault current.

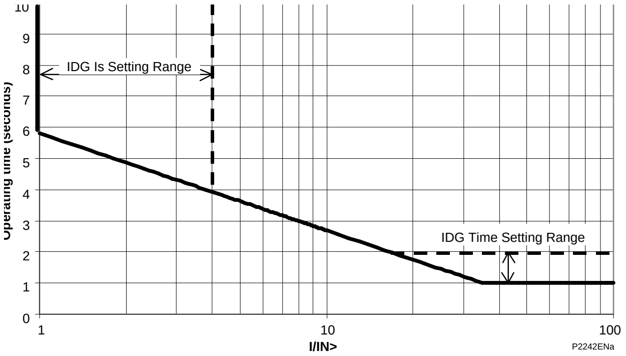

Figure 1 - IDG Characteristic

Through Fault

Through Fault: Disabled/Enabled
Monitored Input: HV / LV / TV
TF I> Trigger: 0.08 to 20.00PU
TF I2t> Alarm: 0 to 500 000 A2 s

Residual Overvoltage (nvd)

VN>1 Function: Disabled/DT/IDMT
VN>1 Voltage Set: 1 to 80 V
VN>1 Time Delay: 0 to 100 s
VN>1 TMS: 0.5 to 100
VN>1 tReset: 0 to 100 s
VN>2 Status: Enabled/Disabled
VN>2 Voltage Set: 1 to 80 V
VN>2 Time Delay: 0 to 100 s

Overfluxing (Volts/Hz)

Volts/Hz W2
V/Hz Alm Status: Disabled/Enabled
V/Hz Alarm Set: 1.5 to 3.5 V/Hz
V/Hz Alarm Delay: 0 to 6000 s
V/Hz>1 Status: Disabled/Enabled
V/Hz>1 Trip Func DT / IDMT
V/Hz>1 Trip Set: 1.5 to 3.5 V/Hz
V/Hz>1 Trip TMS: 0.01 to 12
V/Hz>1 Delay: 0 to 6000 s
V/Hz>1 tReset: 0 to 6000 s
V/Hz>2 Status: Disabled/Enabled
V/Hz>2 Trip Set: 1.5 to 3.5 V/Hz
V/Hz>2 Delay: 0 to 6000 s
V/Hz>3 and 4 same as V/Hz>2
TPre-trip Alarm:1 to 6000.0 s
Volts/Hz W1 the same as Volts/Hz W2
The inverse time characteristic is given by

$$t = \frac{TMS}{(M - 1)^2}$$

Where:

$$M = \frac{V/f}{(\text{ V/f Trip Setting })}$$

V = Measured voltage
F = Measured frequency

VOLTAGE PROTECTION

Undervoltage

V< Measur't Mode: Phase-Phase/
Phase-Neutral
V< Operate Mode: Any Phase/Three Phase
V< 1 Function: Disabled/DT/IDMT
V<1 Voltage Set: 10 to 120 V (100/120 V)
V<1 Time Delay: 0.00 to 00.00 s
V<1 TMS: 0.05 to 100.0
V<1 Poledead Inh: Disabled/Enabled
V<2 Function: Disabled/DT
V<2 Status: Disabled/Enabled
V<2 Voltage Set: 10 to 120 V (100/120 V)
V<2 Time Delay: 0.00 to 100.00 s
V<2 Poledead Inh: Disabled/Enabled
The inverse characteristic is given by:

$$t = \frac{K}{(1 - M)}$$

Where:
K = Time multiplier setting
t = Operating time in seconds
M = Applied input voltage/ undervoltage setting

Overvoltage

V> Measur't Mode: Phase-Phase/
Phase-Neutral
V> Operate Mode: Any Phase/Three Phase
V> 1 Function: Disabled/DT/IDMT
V>1 Voltage Set: 60 to 185 V(100/120 V)
V>1 Time Delay: 0.00 to 100.00 s
V>1 TMS: 0.05 to 100.0
V>2 Status: Disabled/Enabled
V>2 Voltage Set: 60 to 185 V
(100/120 V)
V>2 Time Delay: 0.00 to 100.00 s
The inverse characteristic is given by:

$$t = \frac{K}{(M - 1)}$$

Where:
K = Time multiplier setting
t = Operating time in seconds
M = Applied input voltage/overvoltage setting

NPS Overvoltage

V2>1 Status: Enabled/Disabled
V2>1 Voltage Set: 1 to 110 V
V2>1 Time Delay: 0 to 100 s

FREQUENCY PROTECTION

Underfrequency

F<1 Status: Disabled/Enabled
F<1 Setting: 46.00 to 65.00 Hz
F<1 Time Delay: 0 to 100.0 s
F<2/3/4 the same as F<1

Overfrequency

F>1 Status: Disabled/Enabled
F>1 Setting: 46.00 to 65.00 Hz
F>1 Time Delay: 0 to 100.0 s
F>2 the same as F>1

RTD Protection

Select RTD: Bit 0 - Select RTD 1
Bit 1 - Select RTD 2
through to
Bit 9 - Select RTD 10
Binary function link string, selecting which RTDs (1 - 10) are enabled.
RTD 1 Alarm Set: 0°C to 200°C
RTD 1 Alarm Dly: 0 s to 100 s
RTD 1 Trip Set: 0°C to 200°C
RTD 1 Trip Dly: 0 s to 100 s
RTD2/3/4/5/6/7/8/9/10 the same as RTD1

Current Loop Input

CLIO1 Input 1: Disabled/Enabled
CLI1 Input Type: 0 – 1 mA
0 – 10 mA
0 – 20 mA
4 – 20 mA
CLI1 Input Label: 16 characters
(CLIO input 1)
CLI1 Minimum: -9999…+9999
CLI1 Maximum: -9999…+9999
CLI1 Alarm: Disabled/Enabled
CLI1 Alarm Fn: Over/Under
CLI1 Alarm Set: CLI1 min to CLI1 max
CLI1 Alarm Delay: 0.0 to 100.0 s
CLI1 Trip: Disabled/Enabled
CLI1 Trip Fn: Over/Under
CLI1 Trip Set: CLI1 min to CLI1 max
CLI1 Trip Delay: 0.0 to 100.0 s
CLI1 I< Alarm (4 to 20 mA input only):
Disabled/Enabled
CLI1 I< Alm Set (4 to 20 mA input only):
0.0 to 4.0 mA
CLI2/3/4 the same as CLI1

Current Loop Output

CLO1 Output 1: Disabled/Enabled
CLO1 Output Type: 0 – 1 mA
0 – 10 mA
0 – 20 mA
4 – 20 mA
CLO1 Set Values: Primary/Secondary
CLO1 Parameter: As shown below*
CLO1 Min: Range, step size and unit corresponds to the selected parameter
CLO1 Max: Same as CLO1 Min
CLO2/3/4 the same as CLO1
Current Loop Output Parameters:

IA-1 Magnitude
IB-1 Magnitude
IC-1 Magnitude
IA-2 Magnitude
IB-2 Magnitude
IC-2 Magnitude
IA-3 Magnitude
IB-3 Magnitude
IC-3 Magnitude
IA-4 Magnitude
IB-4 Magnitude
IC-4 Magnitude
IA-5 Magnitude
IB-5 Magnitude
IC-5 Magnitude
I1-1 Magnitude
I2-1 Magnitude
I0-1 Magnitude
I1-2 Magnitude
I2-2 Magnitude
I0-2 Magnitude
I1-3 Magnitude
I2-3 Magnitude
I0-3 Magnitude
I1-4 Magnitude
I2-4 Magnitude
I0-4 Magnitude
I1-5 Magnitude
I2-5 Magnitude
I0-5 Magnitude
IA HV Magnitude
IB HV Magnitude
IC HV Magnitude
IN HV Measured Mag
IN HV Derived Mag
IA LV Magnitude
IB LV Magnitude
IC LV Magnitude
IN LV Measured Mag
IN LV Derived Mag
IA TV Magnitude
IB TV Magnitude
IC TV Magnitude
IN TV Measured Mag
IN TV Derived Mag
VAB Magnitude
VBC Magnitude
VCA Magnitude
VAN Magnitude
VBN Magnitude
VCN Magnitude
Vx Magnitude
VN Derived Mag
V1 Magnitude
V2 Magnitude
V0 Magnitude
VAN RMS
VBN RMS
VCN RMS
Frequency
RTD 1 through to RTD 10
CL Input 1 through to CL Input 4
Volts/Hz W1
V/Hz W1 Thermal
Volts/Hz W2
V/Hz W2 Thermal
Hot Spot T
Top Oil T
Ambient T
LOL Status

CB Fail & I<

T1 CBF Status: Enabled/Disabled
I< Current Set: 5% to 400%
IN< Status: Enabled/Disabled
IN< Input: Measured/Derived
IN< Terminal: TN1/TN2/TN3
IN< Current Set: 5% to 400%
CB Fail 1 Status: Enabled/Disabled
CB Fail 1 Timer: 0 to 10s
CB Fail 2 Status: Enabled/Disabled
CB Fail 2 Timer: 0 to 10s
CBF Non I Reset: I< Only,
CB Open & I<,
Prot Reset & I<
CBF Ext Reset: I< Only,
CB Open & I <,
Prot Reset & I<
T2 CBF, T3 CBF, T4 CBF and T5 CBF the same as T1 CBF

INPUT LABELS

Opto Input 1 to 32: Input L1 to Input L32
User-defined text string to describe the function of the particular opto input.

OUTPUT LABELS

Relay 1 to 32: Output R1 to Output R32
User-defined text string to describe the function of the particular relay output contact.

RTD LABELS

RTD 1-10: RTD1 to RTD10
User-defined text string to describe the function of the particular RTD.

SUPERVISORY FUNCTIONS

Voltage Transformer Supervision

VTS Status: Blocking/ Indication/ Disabled
VTS Reset Mode: Manual/Auto
VTS Time Delay: 1.0 to 10.0 s
VTS I> Inhibit: 0.08 In to 32.0 In
VTS I2> Inhibit: 0.05 In to 0.50 In
Negative phase sequence voltage (V2):
10 V (100/120 V)
Phase overvoltage:
Pick-up 30 V,
Drop-off 10 V (100/120 V)
Superimposed Current: 0.1 In

Current Transformer Supervision

Diff CTS: Enabled/Disabled
CTS Status: Restrain/Indication
CTS Time Delay: 0 to 10 s
CTS I1: 5 to 100%
CTS I2/I1>1: 5 to 100%
CTS I2/I1>2: 5 to 100%

MEASUREMENTS LIST

Measurements 1

P642

IA-1 Magnitude
IA-1 Phase Angle
IB-1 Magnitude
IB-1 Phase Angle
IC-1 Magnitude
IC-1 Phase Angle
IA-2 Magnitude
IA-2 Phase Angle
IB-2 Magnitude
IB-2 Phase Angle
IC-2 Magnitude
IC-2 Phase Angle
IA-HV Magnitude
IA-HV Phase Ang
IB-HV Magnitude
IB-HV Phase Ang
IC-HV Magnitude
IC-HV Phase Ang
IA-LV Magnitude
IA-LV Phase Ang
IB-LV Magnitude
IB-LV Phase Ang
IC-LV Magnitude
IC-LV Phase Ang
I0-1 Magnitude
I1-1 Magnitude
I2-1 Magnitude
IN-HV Mea Mag
IN-HV Mea Ang
IN-HV Deriv Mag
IN-HV Deriv Ang
I0-2 Magnitude
I1-2 Magnitude
I2-2 Magnitude
IN-LV Mea Mag
IN-LV Mea Ang
IN-LV Deriv Mag
IN-LV Deriv Ang
IA-HV RMS
IB-HV RMS
IC-HV RMS
IA-LV RMS
IB-LV RMS
IC-LV RMS
Vx Magnitude
Vx Phase Angle
V1 Magnitude
V2 Magnitude
VAB Magnitude
VAB Phase Angle
VBC Magnitude
VBC Phase Angle
VCA Magnitude

VCA Phase Angle
Frequency

P643

IA-1 Magnitude
IA-1 Phase Angle
IB-1 Magnitude
IB-1 Phase Angle
IC-1 Magnitude
IC-1 Phase Angle
IA-2 Magnitude
IA-2 Phase Angle
IB-2 Magnitude
IB-2 Phase Angle
IC-2 Magnitude
IC-2 Phase Angle
IA-3 Magnitude
IA-3 Phase Angle
IB-3 Magnitude
IB-3 Phase Angle
IC-3 Magnitude
IC-3 Phase Angle
IA-HV Magnitude
IA-HV Phase Ang
IB-HV Magnitude
IB-HV Phase Ang
IC-HV Magnitude
IC-HV Phase Ang
IA-LV Magnitude
IA-LV Phase Ang
IB-LV Magnitude
IB-LV Phase Ang
IC-LV Magnitude
IC-LV Phase Ang
IA-TV Magnitude
IA-TV Phase Ang
IB-TV Magnitude
IB-TV Phase Ang
IC-TV Magnitude
IC-TV Phase Ang
I0-1 Magnitude
I1-1 Magnitude
I2-1 Magnitude
IN-HV Mea Mag
IN-HV Mea Ang
IN-HV Deriv Mag
IN-HV Deriv Ang
I0-2 Magnitude
I1-2 Magnitude
I2-2 Magnitude
IN-LV Mea Mag
IN-LV Mea Ang
IN-LV Deriv Mag
IN-LV Deriv Ang
I0-3 Magnitude
I1-3 Magnitude
I2-3 Magnitude
IN-TV Mea Mag
IN-TV Mea Ang
IN-TV Deriv Mag
IN-TV Deriv Ang
IA-HV RMS
IB-HV RMS
IC-HV RMS
IA-LV RMS
IB-LV RMS
IC-LV RMS
IA-TV RMS
IB-TV RMS
IC-TV RMS
VAN Magnitude
VAN Phase Angle
VBN Magnitude
VBN Phase Angle
VCN Magnitude
VCN Phase Angle
Vx Magnitude
Vx Phase Angle
V1 Magnitude
V2 Magnitude
V0 Magnitude
VN Derived Mag
VN Derived Angle
VAB Magnitude
VAB Phase Angle
VBC Magnitude
VBC Phase Angle
VCA Magnitude
VCA Phase Angle
VAN RMS
VBN RMS
VCN RMS
Frequency

P645

IA-1 Magnitude
IA-1 Phase Angle
IB-1 Magnitude
IB-1 Phase Angle
IC-1 Magnitude
IC-1 Phase Angle
IA-2 Magnitude
IA-2 Phase Angle
IB-2 Magnitude
IB-2 Phase Angle
IC-2 Magnitude
IC-2 Phase Angle
IA-3 Magnitude
IA-3 Phase Angle
IB-3 Magnitude
IB-3 Phase Angle
IC-3 Magnitude
IC-3 Phase Angle
IA-4 Magnitude
IA-4 Phase Angle
IB-4 Magnitude
IB-4 Phase Angle
IC-4 Magnitude

IC-4 Phase Angle
IA-5 Magnitude
IA-5 Phase Angle
IB-5 Magnitude
IB-5 Phase Angle
IC-5 Magnitude
IC-5 Phase Angle
IA-HV Magnitude
IA-HV Phase Ang
IB-HV Magnitude
IB-HV Phase Ang
IC-HV Magnitude
IC-HV Phase Ang
IA-LV Magnitude
IA-LV Phase Ang
IB-LV Magnitude
IB-LV Phase Ang
IC-LV Magnitude
IC-LV Phase Ang
IA-TV Magnitude
IA-TV Phase Ang
IB-TV Magnitude
IB-TV Phase Ang
IC-TV Magnitude
IC-TV Phase Ang
I0-1 Magnitude
I1-1 Magnitude
I2-1 Magnitude
IN-HV Mea Mag
IN-HV Mea Ang
IN-HV Deriv Mag
IN-HV Deriv Ang
I0-2 Magnitude
I1-2 Magnitude
I2-2 Magnitude
IN-LV Mea Mag
IN-LV Mea Ang
IN-LV Deriv Mag
IN-LV Deriv Ang
I0-3 Magnitude
I1-3 Magnitude
I2-3 Magnitude
IN-TV Mea Mag
IN-TV Mea Ang
IN-TV Deriv Mag
IN-TV Deriv Ang
I0-4 Magnitude
I1-4 Magnitude
I2-4 Magnitude
I0-5 Magnitude
I1-5 Magnitude
I2-5 Magnitude
IA-HV RMS
IB-HV RMS
IC-HV RMS
IA-LV RMS
IB-LV RMS
IC-LV RMS
IA-TV RMS
IB-TV RMS
IC-TV RMS
VAN Magnitude
VAN Phase Angle
VBN Magnitude
VBN Phase Angle
VCN Magnitude
VCN Phase Angle
Vx Magnitude
Vx Phase Angle
V1 Magnitude
V2 Magnitude
V0 Magnitude
VN Derived Mag
VN Derived Angle
VAB Magnitude
VAB Phase Angle
VBC Magnitude
VBC Phase Angle
VCA Magnitude
VCA Phase Angle
VAN RMS
VBN RMS
VCN RMS
Frequency

Measurements 2

P642

IA Differential
IB Differential
IC Differential
IA Bias
IB Bias
IC Bias
IA Diff 2H
IB Diff 2H
IC Diff 2H
IA Diff 5H
IB Diff 5H
IC Diff 5H
IREF HV LoZ Diff
IREF HV LoZ Bias
IREF LV LoZ Diff
IREF LV LoZ Bias
IREF Auto LoZ Diff
IREF Auto LoZ Bias
IREF HV HighZ Op
IREF LV HighZ Op
IREF Auto HighZ Op
Thermal Overload
Hot Spot T
Top Oil T
Reset Thermal
Ambient T
TOL Pretrip left
LOL status
Reset LOL
Rate of LOL
LOL Aging Factor
Lres at designed
FAA,m
Lres at FAA,m
Volts/Hz
Volts/Hz W2
V/Hz W2 tPretrip
V/Hz W2 Thermal
Reset V/Hz W2
RTD 1 label
RTD 2 label
RTD 3 label
RTD 4 label
RTD 5 label
RTD 6 label
RTD 7 label
RTD 8 label
RTD 9 label
RTD 10 label
RTD Open Cct
RTD Short Cct
RTD Data Error
Reset RTD Flags
CLIO Input 1
CLIO Input 2
CLIO Input 3
CLIO Input 4

P643 and P645

A Phase Watts
A Phase Watts
A Phase Watts
B Phase Watts
B Phase Watts
B Phase Watts
C Phase Watts
C Phase Watts
C Phase Watts
A Phase VArs
A Phase VArs
A Phase VArs
B Phase VArs
B Phase VArs
B Phase VArs
C Phase VArs
C Phase VArs
C Phase VArs
A Phase VA
A Phase VA
A Phase VA
B Phase VA
B Phase VA
B Phase VA
C Phase VA
C Phase VA
C Phase VA
3 Phase Watts
3 Phase Watts
3 Phase Watts
3 Phase VArs
3 Phase VArs
3 Phase VArs
3 Phase VA
3 Phase VA
3 Phase VA
3Ph Power Factor
APh Power Factor
BPh Power Factor
CPh Power Factor
3Ph WHours Fwd
3Ph WHours Rev
3Ph VArHours Fwd
3Ph VArHours Rev
3Ph W Fix Demand
3Ph VArs Fix Dem
3 Ph W Roll Dem
3Ph VArs RollDem
3Ph W Peak Dem
3Ph VAr Peak Dem
Reset Demand

Measurements 3

P643 and P645

IA Differential
IB Differential
IC Differential
IA Bias
IB Bias
IC Bias
IA Diff 2H
IB Diff 2H
IC Diff 2H
IA Diff 5H
IB Diff 5H
IC Diff 5H
IREF HV LoZ Diff
IREF HV LoZ Bias
IREF LV LoZ Diff
IREF LV LoZ Bias
IREF TV LoZ Diff
IREF TV LoZ Bias
IREF Auto LoZ Diff
IREF Auto LoZ Bias
IREF HV HighZ Op
IREF LV HighZ Op
IREF TV HighZ Op
IREF Auto HighZ Op
Thermal Overload
Hot Spot T
Top Oil T
Reset Thermal
Ambient T
TOL Pretrip left
LOL status
Reset LOL
Rate of LOL
LOL Aging Factor
Lres at designed
FAA,m
Lres at FAA,m
Volts/Hz
Volts/Hz W1
V/Hz W1 tPretrip
V/Hz W1 Thermal
Reset V/Hz W1
Volts/Hz W2
V/Hz W2 tPretrip
V/Hz W2 Thermal
Reset V/Hz W2
RTD 1 label
RTD 2 label
RTD 3 label
RTD 4 label
RTD 5 label
RTD 6 label
RTD 7 label
RTD 8 label
RTD 9 label
RTD 10 label
RTD Open Cct
RTD Short Cct
RTD Data Error
Reset RTD Flags
CLIO Input 1
CLIO Input 2
CLIO Input 3
CLIO Input 4

Notes:

GETTING STARTED

CHAPTER NO 3

Date:	12/2013
Hardware Suffix:	J (P642) K (P643/P645)
Software Version:	04
Connection Diagrams:	10P642xx (xx = 1 to 10) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9)

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1 INTRODUCTION TO THE RELAY

1.1 User Interfaces and Menu Structure

The settings and functions of the MiCOM protection relay are available from the front panel keypad and LCD, and through the front and rear communication ports.

1.2 Front Panel

Figure 1 and Figure 2 show the front panel of the relay; the hinged covers at the top and bottom of the front panel are shown open. An optional transparent front cover physically protects the front panel. With the cover in place, access to the user interface is read-only. Removing the cover allows access to the relay settings and does not compromise the protection of the product from the environment.

When editing relay settings, full access to the relay keypad is needed. To remove the front panel:

1. Open the top and bottom covers, then unclip and remove the transparent cover. If the lower cover is secured with a wire seal, remove the seal.
2. Using the side flanges of the transparent cover, pull the bottom edge away from the relay front panel until it is clear of the seal tab.
3. Move the cover vertically down to release the two fixing lugs from their recesses in the front panel.

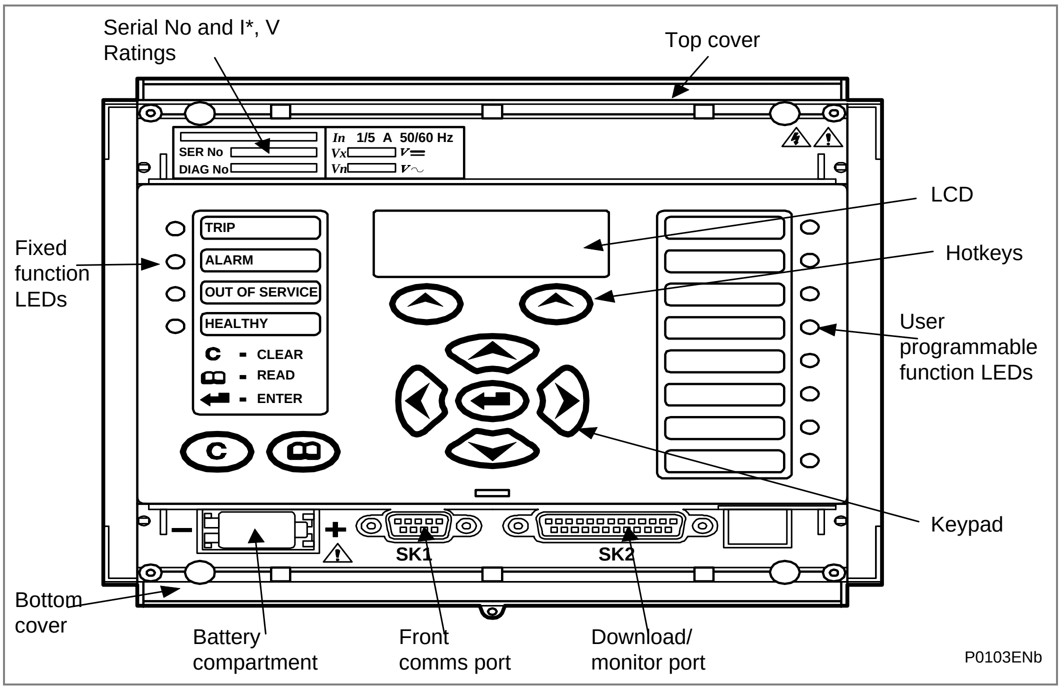

Serial No and I*, V Ratings
Top cover
SER No
DIAG No
In 1/5 A 50/60 Hz
Vx
Vn
LCD
Hotkeys
Fixed function LEDs
TRIP
ALARM
OUT OF SERVICE
HEALTHY
CLEAR
READ
ENTER
User programmable function LEDs
Keypad
SK1
SK2
Bottom cover
Battery compartment
Front comms port
Download/ monitor port
P0103ENb

Figure 1 - Relay front view (P642)

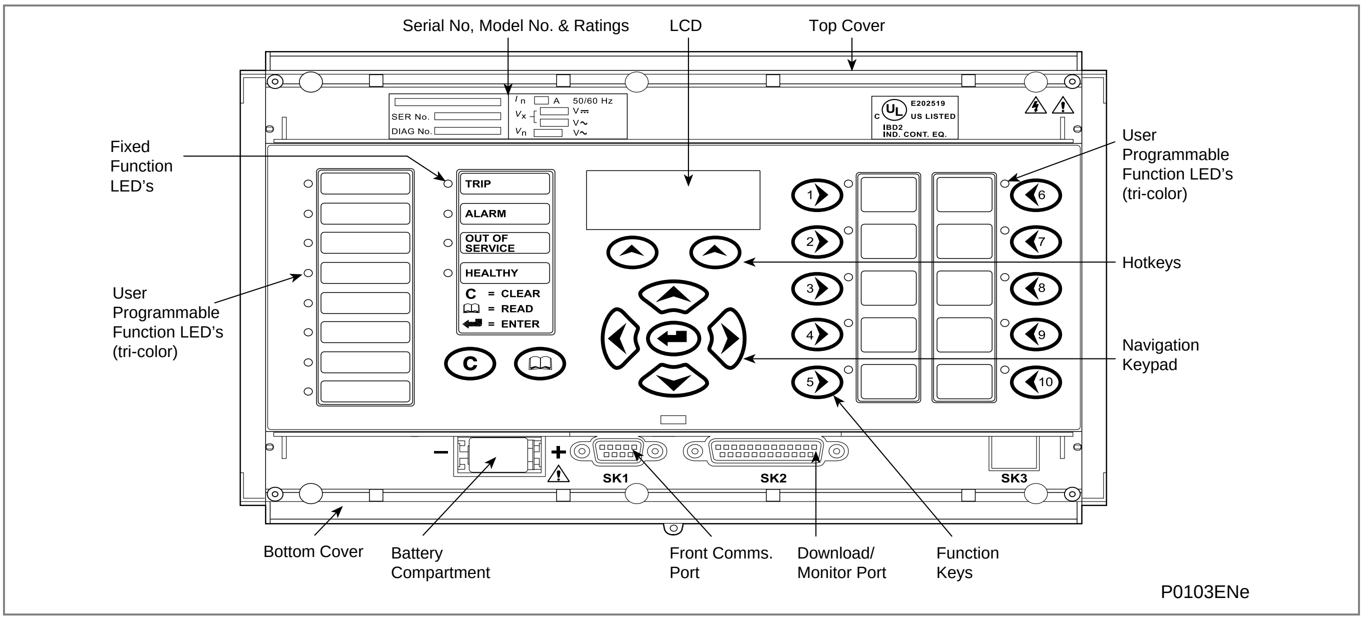

Serial No, Model No. & Ratings
LCD
Top Cover
Fixed Function LED's
User Programmable Function LED's (tri-color)
User Programmable Function LED's (tri-color)
Hotkeys
Navigation Keypad
TRIP
ALARM
OUT OF SERVICE
HEALTHY
C = CLEAR
= READ
= ENTER
SER No.
DIAG No.
In
A
50/60 Hz
Vx
Vn
E202519
US LISTED
IBD2
IND. CONT. EQ.
1
2
3
4
5
6
7
8
9
10
SK1
SK2
SK3
Bottom Cover
Battery Compartment
Front Comms. Port
Download/ Monitor Port
Function Keys
P0103ENe

Figure 2 - Relay front view (P643 and 645)

The front panel of the relay includes these features. See Figure 1 and Figure 2.

- A 16-character by 3-line alphanumeric Liquid Crystal Display (LCD).
- A 19-key (P643/P645), 9-key (P643) keypad with 4 arrow keys (◀, ▶, ▲ and ▼), an enter key (↵), a clear key (Ⓒ), a read key (📖), 2 hot keys (▲) and 10 (① – ⑩) programmable function keys (P645).
- Function key functionality (P643/P645). The relay front panel has control keys with programmable LEDs for local control. Factory default settings associate specific relay functions with these 10 direct-action keys and LEDs, such as Enable or Disable the auto-recloser function. Using programmable scheme logic, the user can change the default functions of the keys and LEDs to fit specific needs.
- Hotkey functionality:
  - **SCROLL** starts scrolling through the various default displays.
  - **STOP** stops scrolling the default display.
  - Control inputs and circuit breaker operation to control setting groups.
- 22 LEDs (P643/P645), 12 LEDs (P642); 4 fixed function LEDs, 8 tri-color (P643/P645), 8 red (P642) programmable function LEDs on the left-hand side of the front panel and 10 tri-color programmable function LEDs on the right-hand side associated with the function keys (P643/P645).
- Under the top hinged cover:
  - The relay's serial number.
  - The relay's current and voltage rating.
- Under the bottom hinged cover:
  - Compartment for a 1/2 AA size backup battery used for the real time clock and event, fault, and disturbance records.
  - A 9-pin female D-type front port for a connection of up to 15 m between a PC and the relay using an EIA(RS)232 serial data connection.
  - A 25-pin female D-type parallel port for monitoring internal signals and downloading high-speed local software and language text.

1.2.1 LED Indications

1.2.1.1 Fixed Function

The four fixed-function LEDs on the left-hand side of the front panel indicate the following conditions.

- **Trip** (Red) switches ON when the relay issues a trip signal. It is reset when the associated fault record is cleared from the front display. Also the trip LED can be configured as self-resetting.
- **Alarm** (Yellow) flashes when the relay registers an alarm. This may be triggered by a fault, event or maintenance record. The LED flashes until the alarms have been accepted (read), then changes to constantly ON. When the alarms are cleared, the LED switches OFF.
- **Out of Service** (Yellow) is ON when the relay's protection is unavailable.
- **Healthy** (Green) is ON when the relay is in correct working order, and should be ON at all times. It goes OFF if the relay's self-tests show there is an error in the relay's hardware or software. The state of the healthy LED is reflected by the watchdog contacts at the back of the relay.

To adjust the LCD contrast, from the **CONFIGURATION** column, select **LCD Contrast**. This is only needed in very hot or cold ambient temperatures.

1.2.1.2 Programmable LEDs

The P642 has eight RED programmable LEDs (numbers 1 to 8) used for alarm indications.

The P643 and P645 have eight programmable LEDs (numbers 1 to 8) for alarm conditions and ten programmable LEDs (F1 to F10) to show the status of the function keys. All of the programmable LEDs on the P643 and P645 are tri-color and can be set to RED, YELLOW or GREEN.

The default settings are shown in Table 1:

LED No	Default indication	P64x relay
1	Red	Differential trip
2	Red	REF trip - REF HV Trip, REF LV trip, REF TV trip
3	Red	Top oil trip – Top oil 1 trip, Top oil 2 trip, Top oil 3 trip Hot spot trip – Hot spot 1 trip, Hot spot 2 trip, Hot spot 3 trip
4	Red	Overflux trip – W1 V/Hz>1, W1 V/Hz>2, W1 V/Hz>3, W1 V/Hz>4, W2 V/Hz>1, W2 V/Hz>2, W2 V/Hz>3, W2 V/Hz>4 Underfrequency trip – F<1, F<2, F<3, F<4 Overfrequency trip – F>1, F>2 Undervoltage trip – V<1, V<2 Overvoltage trip – V>1, V>2 Residual overvoltage trip - VN>1, VN>2
5	Red	HV overcurrent trip – POC 1I>1, POC 1I>2, POC 1 I>3, POC 1 I>4, HV earth fault trip – EF 1 IN>1, EF 1 IN>2, EF 1 IN>3, EF 1IN>4 HV NPOC trip – NPOC1I2>1, NPOC1 I2>2, NPOC I2>3, NPOC I2>4
6	Red	LV overcurrent trip – POC 2 I>1, POC 2 I>2, POC 2 I>3, POC 2 I>4, LV earth fault trip - EF 2 IN>1, EF 2 IN>2, EF 2 IN>3, EF 2 IN>4 LV NPSOC trip - NPOC2 I2>1, NPOC2 I2>2, NPOC2 I2>3, NPOC2 I2>4

LED No	Default indication	P64x relay
7	Green	TV overcurrent trip – POC 3 I>1, POC 3 I>2, POC 3 I>3, POC 3 I>4 TV earth fault trip - EF 3 IN>1, EF 3 IN>2, EF 3 IN>3, EF 3 IN>4 TV NPOC trip - NPOC3 I2>1, NPOC3 I2>2, NPOC3 I2>3, NPOC3 I2>4
8	Red/Yellow/Green	CB Fail
F1	Red/Yellow/Green	Not used
F2	Red/Yellow/Green	Not used
F3	Red/Yellow/Green	Not used
F4	Red/Yellow/Green	Not used
F5	Red	Setting Group 2 Enabled
F6	Yellow	Overfluxing Reset
F7	Yellow	Thermal overload reset
F8	Yellow	Loss of life reset
F9	Yellow	Relay/LED reset
F10	Yellow	Manual Trigger Disturbance Recorder

Table 1 - Default settings

1.3 Relay Rear Panel

Figure 3 shows the rear panel of the relay. Slots A and B are for optional IRIG-B boards providing time-synchronization input and fiber optic communications.

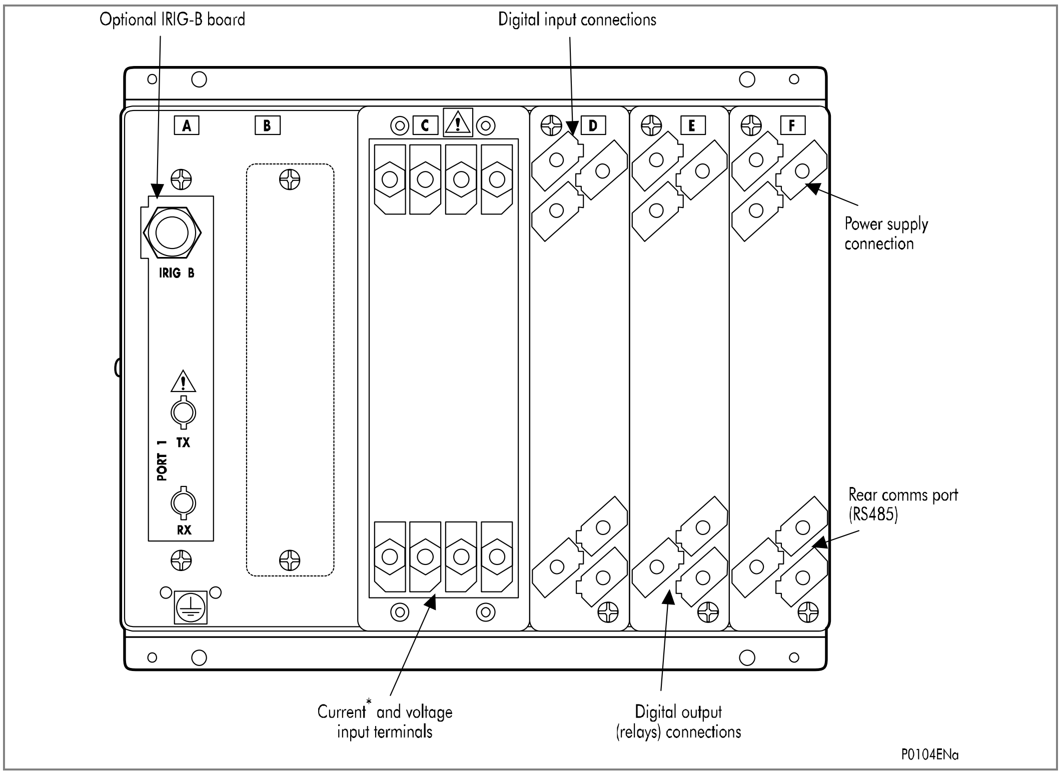

Optional IRIG-B board
Digital input connections
A
B
C
D
E
F
IRIG B
PORT 1
TX
RX
Power supply connection
Rear comms port (RS485)
Current* and voltage input terminals
Digital output (relays) connections
P0104ENa

Figure 3 - Relay rear view

See the wiring diagrams in the *Installation* chapter for complete connection details.

2 RELAY CONNECTION AND POWER-UP

Before powering up the relay, make sure the relay power supply voltage and nominal ac signal magnitudes are appropriate for your application. The relay serial number and its current, voltage and power rating are under the top hinged cover. The relay is available in the auxiliary voltage versions specified in Table 2.

Nominal ranges	Operative dc range	Operative ac range
24 – 48 V dc	19 to 65 V	-
48 – 110 V dc (30 – 100 V ac rms) **	37 to 150 V	24 to 110 V
110 – 250 V dc (100 – 240 V ac rms) **	87 to 300 V	80 to 265 V
** rated for ac or dc operation		
Note The label does not specify the logic input ratings.		

Table 2 - Ranges

The P64x relay has universal opto isolated logic inputs. These can be programmed for the nominal battery voltage of the circuit where they are used. See *Universal Opto isolated logic inputs* in the *Firmware* chapter *P64x/EN FD* for more information on logic input specifications.

Note *The opto inputs have a maximum input voltage rating of 300 V dc at any setting.*

Once the ratings have been verified for the application, connect external power according to the power requirements specified on the label. See *P64x external connection diagrams* in the *Installation* chapter *P64x/EN IN* for complete installation details, ensuring the correct polarities are observed for the dc supply.

3 USER INTERFACES AND SETTINGS

The relay has these user interfaces:

- The front panel using the LCD and keypad.
- The front port which supports Courier communication.
- The rear port which supports one of these protocols: Courier, MODBUS, IEC 60870-5-103 or DNP3.0. The protocol for the rear port must be specified when the relay is ordered.
- An optional Ethernet port supports IEC 61850-8-1 or DNP 3.0.
- A second optional rear port which supports Courier, KBUS or InterMiCOM communication.

	Keypad or LCD	Courier	MODBUS	IEC870-5-103	IEC61850-8-1	DNP3.0
Display & modification of all settings	•	•	•			
Digital I/O signal status	•	•	•	•	•	•
Display/extraction of measurements	•	•	•	•	•	•
Display/extraction of fault records	•	•	•	•		•
Extraction of disturbance records		•	•	•	•	
Programmable scheme logic settings		•				
Reset of fault & alarm records	•	•	•	•		•
Clear event & fault records	•	•	•			•
Time synchronization		•	•	•	•	•
Control commands	•	•	•	•	•	•

Table 3 - Measurement information and relay settings that can be accessed from the interfaces

4 MENU STRUCTURE

The relay's menu is arranged in a table. Each setting in the menu is known as a cell, and each cell in the menu can be accessed using a row and column address. The settings are arranged so that each column contains related settings, for example all of the disturbance recorder settings are in the same column. As shown in Figure 4, the top row of each column contains the heading that describes the settings in that column. You can only move between the columns of the menu at the column heading level. For a complete list of all of the menu settings, see the *Settings* chapter *P64x/EN ST* and the *Relay Menu Database* document *P64x/EN MD*.

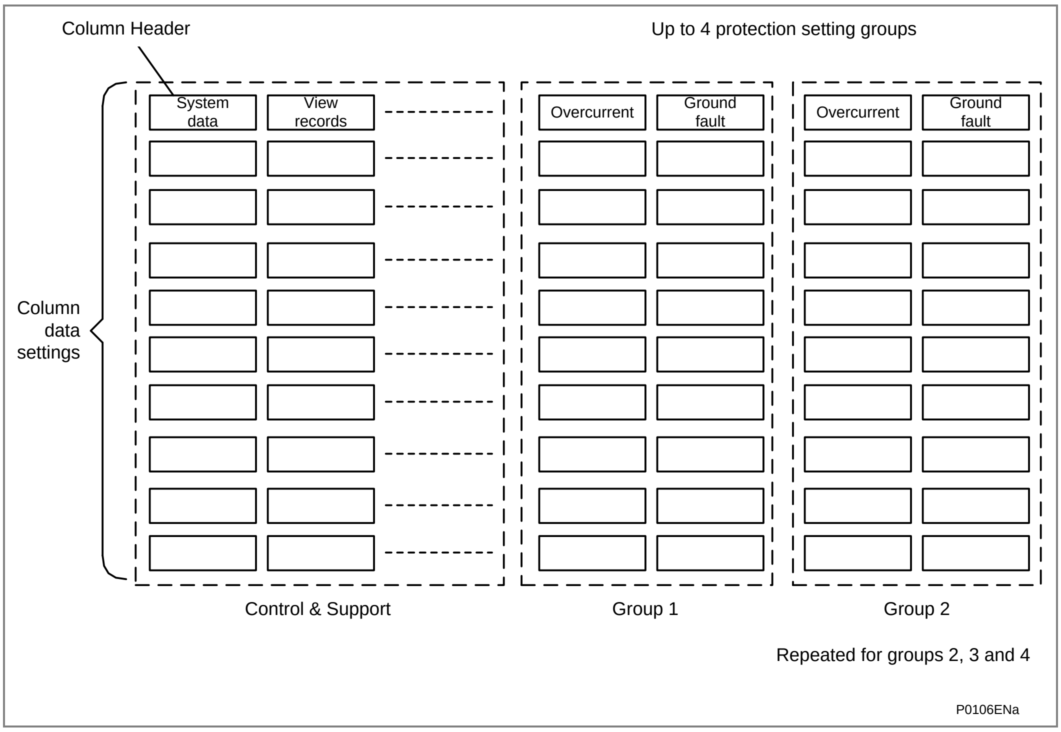

Column Header
Up to 4 protection setting groups
System data
View records
Overcurrent
Ground fault
Overcurrent
Ground fault
Column data settings
Control & Support
Group 1
Group 2
Repeated for groups 2, 3 and 4
P0106ENa

Figure 4 - Menu structure

The settings in the menu are in three categories: protection settings, disturbance recorder settings, or Control and Support (C&S) settings.

New control and support settings are stored and used by the relay immediately after they are entered. New Protection settings or disturbance recorder settings are stored in a temporary 'scratchpad'. Once the new settings have been confirmed, the relay activates all the new settings together. This provides extra security so that several setting changes, made in a group of protection settings, all take effect at the same time.

4.1 Protection Settings

The protection settings include these items:

- Protection element settings
- Scheme logic settings

There are four groups of protection settings, with each group containing the same setting cells. One group of protection settings is selected as the active group, and is used by the protection elements.

4.2 Disturbance Recorder Settings

The disturbance recorder settings include the record duration and trigger position, selection of analog and digital signals to record, and the signal sources that trigger the recording.

4.3 Control and Support Settings

The Control and Support settings include:

- Relay configuration settings
- Open/close circuit breaker (may vary according to relay type or model)
- CT & VT ratio settings
- Reset LEDs
- Active protection setting group
- Password & language settings
- Circuit breaker control & monitoring settings (may vary according to relay type/model)
- Communications settings
- Measurement settings
- Event & fault record settings
- User interface settings
- Commissioning settings

5 PASSWORD PROTECTION

The menu structure contains three levels of access. The level of access that is enabled determines which of the relay’s settings can be changed and is controlled by entering two different passwords. The levels of access are summarized in Table 4.

Set the "Password Control" cell to	The "Access Level" cell displays	Operations	Type of password required
0	0	**Read** Access to all settings, alarms, event records and fault records	None
		Execute Control Commands, such as circuit breaker open or close. Reset of fault and alarm conditions. Reset LEDs. Clearing of event and fault records	Level 1 Password
		Edit All other settings	Level 2 Password
1	1	**Read** Access to all settings, alarms, event records and fault records	None
		Execute Control Commands, such as circuit breaker open or close. Reset of fault and alarm conditions. Reset LEDs. Clearing of event and fault records	None
		Edit All other settings	Level 2 Password
2 (Default)	2 (Default)	**Read** Access to all settings, alarms, event records and fault records	None
		Execute Control Commands, such as circuit breaker open or close. Reset of fault and alarm conditions. Reset LEDs. Clearing of event and fault records	None
		Edit All other settings	None

Table 4 - Password protection

Each of the two passwords are 4 characters of upper-case text. The factory default for both passwords is AAAA. Each password is user-changeable once it has been correctly entered. To enter a password, either use the prompt when a setting change is attempted, or from the menu select **System data** > **Password**. The access level is independently enabled for each interface, therefore if level 2 access is enabled for the rear communication port, the front panel access remains at level 0 unless the relevant password is entered at the front panel.

The access level, enabled by the password, times out independently for each interface after a period of inactivity and reverts to the default level. If the passwords are lost, contact Schneider Electric with the relay’s serial number and an emergency password can be supplied. To find the current level of access enabled for an interface, select **System data** > **Access level**. The access level for the front panel User Interface (UI) is one of the default display options.

The relay is supplied with a default access level of 2, so no password is needed to change any of the relay settings. It is also possible to set the default menu access level to either level 0 or level 1, preventing write access to the relay settings without the correct password. The default menu access level is set in **System data** > **Password control**.

Note	*This setting can only be changed when level 2 access is enabled.*

6 RELAY CONFIGURATION

The relay is a multi-function device that supports many different protection, control and communication features. To simplify the setting of the relay, there is a configuration settings column which can be used to enable or disable many of the functions of the relay. The settings associated with any function that is disabled are not shown in the menu. To disable a function, change the relevant cell in the **Configuration** column from **Enabled** to **Disabled**.

The configuration column controls which of the four protection settings groups is selected as active using the **Active settings** cell. A protection setting group can also be disabled in the configuration column, provided it is not the present active group. Similarly, a disabled setting group cannot be set as the active group.

7 FRONT PANEL USER INTERFACE (KEYPAD AND LCD)

When the keypad is exposed it provides full access to the menu options of the relay, with the information displayed on the LCD.

The ◀, ▶, ▲ and ▼ keys are used for menu navigation and setting value changes. These keys have an auto-repeat function if any of them are held continually. This can speed up both setting value changes and menu navigation: the longer the key is held pressed, the faster the rate of change or movement.

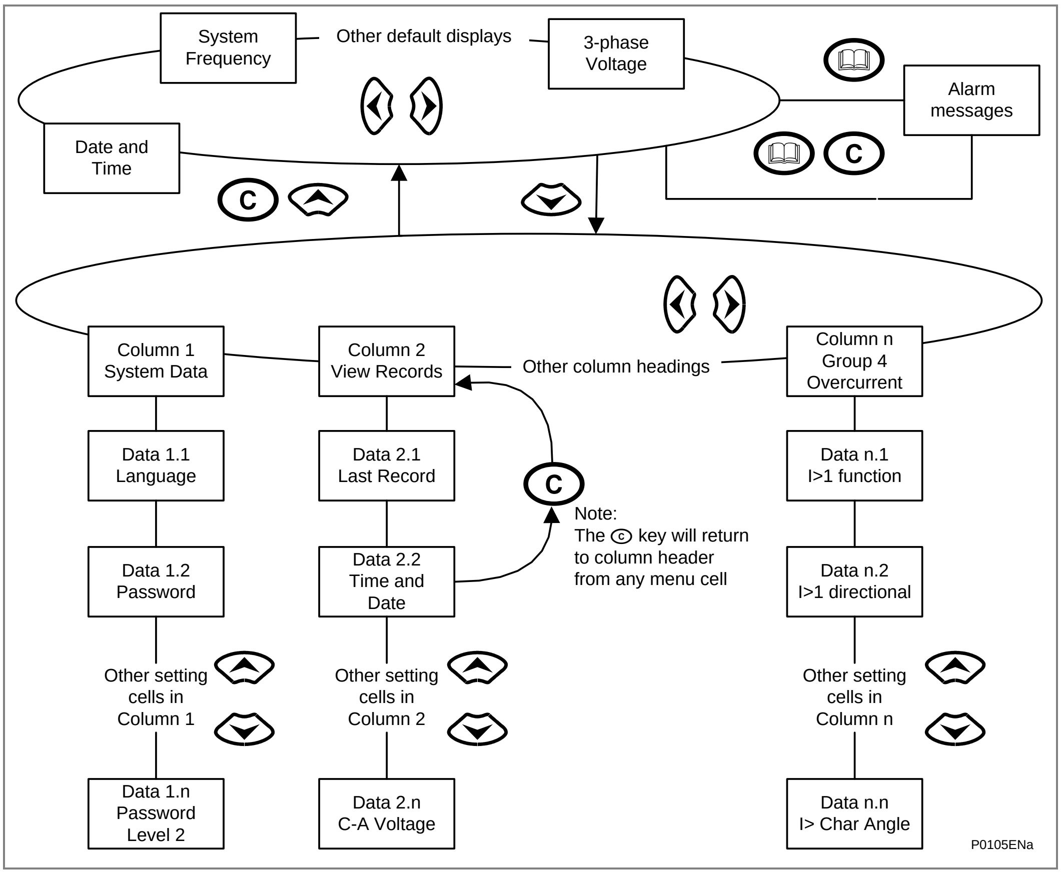

System Frequency
Other default displays
3-phase Voltage
Alarm messages
Date and Time
C
C
Column 1 System Data
Column 2 View Records
Other column headings
Column n Group 4 Overcurrent
Data 1.1 Language
Data 2.1 Last Record
C
Note:
The C key will return to column header from any menu cell
Data n.1 I>1 function
Data 1.2 Password
Data 2.2 Time and Date
Data n.2 I>1 directional
Other setting cells in Column 1
Other setting cells in Column 2
Other setting cells in Column n
Data 1.n Password Level 2
Data 2.n C-A Voltage
Data n.n I> Char Angle
P0105ENa

Figure 5 - Front panel user interface

7.1 Default Display and Menu Time-Out

The front panel menu has a default display. To change it, select **Measure’t. setup** > **default display** and the following items can be selected:

- Date and time
- Relay description (user defined)
- Plant reference (user defined)
- System frequency
- 3-phase voltage
- 3-phase and neutral current
- Power
- Access level

From the default display you can view the other default display options using the ⏴ and ⏵ keys. If there is no keypad activity for 15 minutes, the default display reverts to the previous setting and the LCD backlight switches off. Any setting changes that have not been confirmed are lost and the original setting values are maintained.
Whenever the relay has an uncleared alarm (such as fault record, protection alarm, or control alarm) the default display is replaced by the following display.

```
Alarms/Faults
Present
```

Enter the menu structure of the relay from the default display, even if the display shows the **Alarms/Faults present** message.

7.2 Navigating Menus and Browsing the Settings

Use the four arrow keys to browse the menu, following the structure shown in Figure 5.

1. Starting at the default display, press the ⏶ key to show the first column heading.
2. Use the ⏴ and ⏵ keys to select the required column heading.
3. Use the ⏷ and ⏶ keys to view the setting data in the column.
4. To return to the column header, either hold the ⏶ key down or press the clear key Ⓒ once. It is only possible to move across columns at the column heading level.
5. To return to the default display, press the ⏶ key or the clear key Ⓒ from any of the column headings. If you use the auto-repeat function of the ⏶ key, you cannot go straight to the default display from one of the column cells because the auto-repeat stops at the column heading.
6. Press the ⏶ key again to go to the default display.

7.3 Navigating the Hotkey Menu

1. To access the hotkey menu from the default display, press the key directly below the **HOTKEY** text on the LCD.
2. Once in the hotkey menu, use the ◀ and ▶ keys to scroll between the available options, then use the hotkeys to control the function currently displayed.
   If neither the ◀ or ▶ keys are pressed within 20 seconds of entering a hotkey sub menu, the relay reverts to the default display.
3. Press the clear key ⓒ□ to return to the default menu from any page of the hotkey menu.

The layout of a typical page of the hotkey menu is as follows:

- The top line shows the contents of the previous and next cells for easy menu navigation
- The center line shows the function
- The bottom line shows the options assigned to the direct access keys

The functions available in the hotkey menu are listed in the following sections.

7.3.1 Setting Group Selection

To select the setting group, scroll through the available setting groups using **NXT GRP**, or press **SELECT** to select the setting group that is currently displayed.

When you press **SELECT**, the current setting group appears for 2 seconds, then the **NXT GRP** or **SELECT** options appear again.

To exit the sub menu, use the left and right arrow keys. For more information see Changing setting groups in the Operation chapter P64x/EN OP.

7.3.2 Control Inputs - User Assignable Functions

The control inputs are user-assignable functions or **USR ASS**.

Use the **CTRL I/P CONFIG** column to configure the number of **USR ASS** shown in the hotkey menu. To SET/RESET the chosen inputs, use the **HOTKEY** menu.

For more information see the *Control Inputs* section in the *Operation* chapter *P64x/EN OP*.

7.4 Password Entry

1. When a password is required to edit a setting, an **Enter password** prompt appears.

```
Enter password
**** Level 1
```

2. A flashing cursor shows which character field of the password can be changed. Press the ⏶ and ⏷ keys to change each character between A and Z.

3. Use the ◀ □and ▶ keys to move between the character fields of the password. Press the enter key ↵ □to confirm the password.□
If an incorrect password is entered, the display reverts to **Enter password**. A message then appears indicating that the password is correct and if so what level of access has been unlocked. If this level is sufficient to edit the selected setting, the display returns to the setting page to allow the edit to continue. If the correct level of password has not been entered, the password prompt page appears again.

4. To escape from this prompt press the clear key □Ⓒ. Alternatively, enter the password using **System data** > **Password**.
If the keypad is inactive for 15 minutes, the password protection of the front panel user interface reverts to the default access level.

5. To manually reset the password protection to the default level, select **System data** > **Password**, then press the clear key instead of entering a password.

7.5 Reading and Clearing Alarm Messages and Fault Records

One or more alarm messages appear on the default display and the yellow alarm LED flashes. The alarm messages can either be self-resetting or latched, in which case they must be cleared manually.

6. To view the alarm messages, press the read key 📖. When all alarms have been viewed but not cleared, the alarm LED change from flashing to constantly ON and the latest fault record appears (if there is one).

7. Scroll through the pages of the latest fault record, using the 📖 key. When all pages of the fault record have been viewed, the following prompt appears.

```
Press clear to
reset alarms
```

8. To clear all alarm messages, press Ⓒ. To return to the display showing alarms or faults present, and leave the alarms uncleared, press 📖.

9. Depending on the password configuration settings, you may need to enter a password before the alarm messages can be cleared. See *section 5 Password Protection.*

10. When all alarms are cleared, the yellow alarm LED switches OFF; also the red trip LED switches OFF if it was switched ON after a trip.

11. To speed up the procedure, enter the alarm viewer using the 📖 key, then press the Ⓒ key. This goes straight to the fault record display. Press Ⓒ again to move straight to the alarm reset prompt, then press Ⓒ again to clear all alarms.

7.6 Setting Changes

1. To change the value of a setting, go to the relevant cell in the menu, then press the enter key ↵ □to change the cell value. A flashing cursor on the LCD shows the value can be changed. If a password is required to edit the cell value, a password prompt appears □□.
2. To change the setting value, press the ▼ or ▲□ keys. If the setting to be changed is a binary value or a text string, select the required bit or character to be changed using the ◄ and ► keys.
3. Press ↵ to confirm the new setting value or the clear key ⓒ to discard it. The new setting is automatically discarded if it is not confirmed in 15 seconds.
4. For protection group settings and disturbance recorder settings, the changes must be confirmed before they are used by the relay.
5. To do this, when all required changes have been entered, return to the column heading level and press the ▼ key. Before returning to the default display, the following prompt appears.

```
Update settings?
Enter or clear
```

6. Press ↵ to accept the new settings or press ⓒ to discard the new settings.

Note	*If the menu time-out occurs before the setting changes have been confirmed, the setting values are also discarded.*

Control and support settings are updated immediately after they are entered, without the **Update settings?** prompt.

8 FRONT COMMUNICATION PORT USER INTERFACE

The front communication port is a 9-pin female D-type connector under the bottom hinged cover. It provides EIA(RS)232 serial data communication up to 15 m with a PC, see Figure 6. This port supports the Courier communication protocol only. Courier is the communication language developed by Schneider Electric to allow communication with its range of protection relays. The front port is intended for use with the relay settings program MiCOM S1 Studio which runs on Windows^{TM} 2000 or XP.

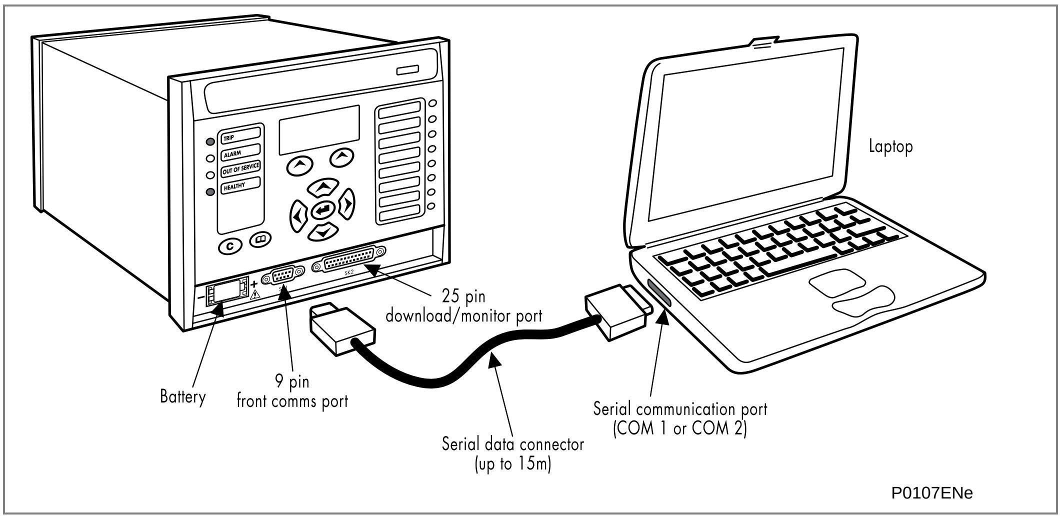


Figure 6 - Front port connection

The relay is a Data Communication Equipment (DCE) device with the pin connections shown in Table 5 on the 9-pin front port.

Pin Number	Description
2	Tx Transmit data
3	Rx Receive data
5	0 V Zero volts common

Table 5 - Relay serial port connections

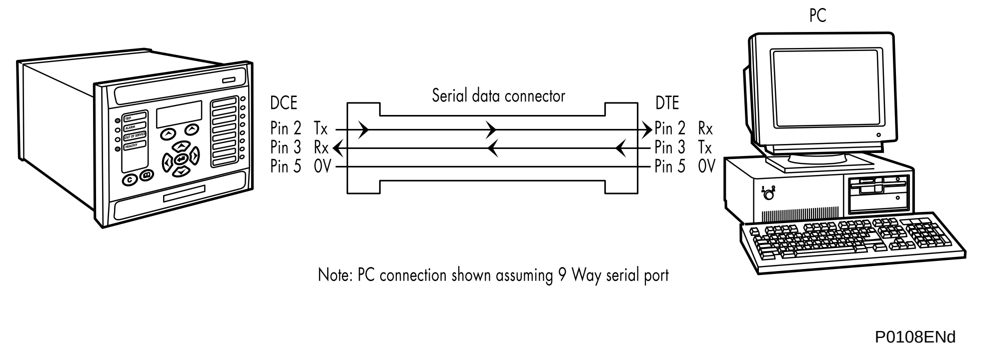
None of the other pins are connected in the relay. The relay should be connected to the COM1 or COM2 serial port of a PC. PCs are normally Data Terminal Equipment (DTE) devices which have the serial port pin connections shown in Table 6 (if in doubt check your PC manual).

Pin Number	25-way	9-way	Description
2	3	2	x Receive data
3	2	3	Tx Transmit data
5	7	5	0 V Zero volts common

Table 6 - PC serial port connections

For successful data communication, connect the Tx pin on the relay to the Rx pin on the PC, and the Rx pin on the relay to the Tx pin on the PC. See Figure 7. Normally a straight-through serial cable is required, connecting pin 2 to pin 2, pin 3 to pin 3, and pin 5 to pin 5.

Note	*A common cause of difficulty with serial data communication is connecting Tx to Tx and Rx to Rx. This could happen if a cross-over serial cable is used, connecting pin 2 to pin 3, and pin 3 to pin 2, or if the PC has the same pin configuration as the relay.*



Note: PC connection shown assuming 9 Way serial port

Figure 7 - PC - relay signal connection

Once the physical connection from the relay to the PC is made, the PC's communication settings must be set to match those of the relay. Table 7 shows the relay's communication settings for the front port.

Protocol	Courier
Baud rate	19,200 bits/s
Courier address	1
Message format	11-bit - 1 start bit, 8 data bits, 1 parity bit (even parity), 1 stop bit

Table 7 - Relay front port settings

If there is no communication using the front port for 15 minutes, any password access level that has been enabled is cancelled.

8.1 Front Courier Port

The front EIA(RS)232 9-pin port supports the Courier protocol for one-to-one communication. This port is compliant with EIA(RS)574, the 9-pin version of EIA(RS)232; see www.tiaonline.org. It is designed for use during installation, and commissioning or maintenance, and is not suitable for permanent connection. Since this interface is not used to link the relay to a substation communication system, the following features of Courier are not used.

Automatic Extraction of Event Records:

- The Courier Status byte does not support the Event flag
- The Send Event or Accept Event commands are not used

Automatic Extraction of Disturbance Records:

- The Courier Status byte does not support the Disturbance flag

Busy Response Layer:

- The Courier Status byte does not support the Busy flag; the only response to a request is the final data

Fixed Address:

- The address of the front courier port is always 1; the Change Device address command is not supported.

Fixed Baud Rate:

- 19200 bps

Note *Although automatic extraction of event and disturbance records is not supported, this data can be manually accessed using the front port.*

9 MICOM S1 STUDIO RELAY COMMUNICATIONS BASICS

The EIA(RS)232 front communication port is intended for use with the relay settings program MiCOM S1 Studio. This program runs on Windows 2000, XP or Vista, and is the universal MiCOM IED Support Software used for direct access to all stored data in any MiCOM IED.

MiCOM S1 Studio provides full access to:

- MiCOM Px10, Px20, Px30, Px40, Modulex series, K series, L series relays
- MiCOM Mx20 measurements units

9.1 PC Requirements

To run MiCOM S1 Studio on a PC, the following requirements are advised.

Minimum

- 1 GHz processor
- 256 MB RAM
- Windows 2000
- Resolution 800 x 600 x 256 colors
- 1 GB free hard disk space

Recommended

- 2 GHz processor
- 1 GB RAM
- Windows XP
- Resolution 1024 x 768
- 5 GB free hard disk space

Microsoft Windows Vista

- 2 GHz processor
- 1 GB RAM
- 5 GB free hard disk space
- MiCOM S1 Studio must be started with Administrator rights

9.2 Connecting to the P64x Relay using MiCOM S1 Studio

This section is intended as a quick start guide to using MiCOM S1 Studio and assumes you have a copy installed on your PC. See the *MiCOM S1 Studio program online help* for more detailed information.

1. Make sure the EIA(RS)232 serial cable is properly connected between the port on the front panel of the relay and the PC. See section 8.
2. To start Micom S1 Studio, select Programs > Schneider Electric > MiCOM S1 Studio > MiCOM S1 Studio.
3. Click the Quick Connect tab and select Create a New System.
4. Check the **Path to System file** is correct, then enter the name of the system in the **Name** field. If you need to add a brief description of the system, use the **Comment** field.
5. Click **OK**.
6. Select the device type.
7. Select the communications port.
8. Once connected, select the language for the settings file, the device name, then click **Finish**. The configuration is updated.
9. In the **Studio Explorer** window, select **Device** > **Supervise Device…** to control the relay directly.

9.3 Off-Line Use of MiCOM S1 Studio

Micom S1 Studio can also be used as an off-line tool to prepare settings, without access to the relay.

1. If creating a new system, in the Studio Explorer, select **create new** system. Then right-click the new system and select **New substation**.
2. Right-click the new substation and select **New voltage level**.
3. Then right-click the new voltage level and select **New bay**.
4. Then right-click the new bay and select **New device**.
   You can add a device at any level, whether it is a system, substation, voltage or bay.
5. Select a device type from the list, then enter the relay type, such as P645. Click **Next**.
6. Enter the full model number and click **Next**.
7. Select the **Language** and **Model**, then click **Next**.
8. Enter a unique device name, then click **Finish**.
9. Right-click the **Settings** folder and select **New File**. A default file **000** is added.
10. Right-click file **000** and select click **Open**. You can then edit the settings. See the *MiCOM S1 Studio program online help* for more information.

SETTINGS

CHAPTER NO 4

Date:	12/2013
Hardware Suffix:	J (P642) K (P643/P645)
Software Version:	04
Connection Diagrams:	10P642xx (xx = 1 to 10) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9)

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Notes:

1 SETTINGS

The P642/P643/P645 must be configured to the system and application using appropriate settings. In this chapter the settings are described in the sequence: protection settings, control and configuration settings and disturbance recorder settings. The relay is supplied with a factory-set configuration of default settings.

2 RELAY SETTINGS CONFIGURATION

The relay is a multi-function device that supports many different protection, control and communication features. To simplify the setting of the relay, there is a configuration settings column, used to enable or disable many of the relay functions. The settings associated with any disabled function are not shown in the menu. To disable a function, change the relevant cell in the **Configuration** column from **Enabled** to **Disabled**.

The configuration column controls which of the four protection settings groups is selected as active through the **Active settings** cell. A protection setting group can also be disabled in the configuration column, provided it is not the present active group. Similarly, a disabled setting group cannot be set as the active group.

The configuration column also allows all of the setting values in one group of protection settings to be copied to another group.

To do this first set the **Copy from** cell to the protection setting group to be copied, then set the **copy to** cell to the protection group where the copy is to be placed. The copied settings are initially placed in a temporary scratchpad and are only used by the relay following confirmation.

To restore the default values to the settings in any protection settings group, set the **restore defaults** cell to the relevant group number. Alternatively, set the **restore defaults** cell to **all settings** to restore all of the relay's settings to default values, not just the protection groups' settings. The default settings are initially placed in the scratchpad and are only used by the relay after they have been confirmed.

Note *If you restore defaults to all settings, it includes the rear communication port settings. If the new (default) settings do not match those of the master station, rear port communication may be disrupted.*

Menu text	Default setting	Available settings
Restore Defaults	No Operation	No Operation All Settings Setting Group 1 Setting Group 2 Setting Group 3 Setting Group 4
Setting to restore a setting group to factory default settings.		
Setting Group	Select from Menu	Select from Menu Select from PSL
Allows setting group changes to be initiated using 2 DDB signals in the programmable scheme logic or from the Menu settings.		
Active Settings	Group 1	Group 1, 2, 3 or 4
Selects the active setting group.		
Save Changes	No Operation	No Operation, Save, Abort
Saves all relay settings.		
Copy from	Group 1	Group 1, 2, 3 or 4
Allows displayed settings to be copied from a selected setting group.		
Copy to	No Operation	No Operation Group 1, 2, 3 or 4
Allows displayed settings to be copied to a selected setting group.		
Setting Group 1	Enabled	Enabled or Disabled
Enables or disables Group 1 settings. If the setting group is disabled from the configuration, all associated settings and signals are hidden, with the exception of this setting.		
Setting Group 2 (as above)	Disabled	Enabled or Disabled
Setting Group 3 (as above)	Disabled	Enabled or Disabled

Menu text	Default setting	Available settings
Setting Group 4 (as above)	Disabled	Enabled or Disabled
System Config	Visible	Invisible or Visible
Sets the System Config menu visible further on in the relay settings menu.		
Diff Protection	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the differential protection. The P64x provides bias differential protection with multiple CT inputs.		
REF Protection	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Restricted Earth Fault protection. The P64x provides a low impedance REF and a high impedance REF function per transformer winding. It can also be applied for autotransformer protection.		
Over Current	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the overcurrent protection. ANSI 50/51/67P, 46OC.		
NPS Overcurrent	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Negative Phase Sequence overcurrent protection. ANSI 50/51/67P, 46OC		
Thermal Overload	Disabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Thermal Overload Protection. ANSI 49.		
Earth Fault	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Earth Fault Protection. ANSI 50N/51N.		
Residual O/V NVD	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Residual Overvoltage (Neutral Voltage Displacement) Protection function. ANSI 59N.		
Overfluxing V/Hz	Disabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Overfluxing protection. ANSI 24.		
Through Fault	Disabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Through Fault function. The Through Fault current monitoring function in the P64x gives the fault current level, the duration of the faulty condition, the date and time.		
Volt Protection	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Voltage Protection (Under/Overvoltage and NPS Overvoltage) function. ANSI 27/59/47.		
Freq. Protection	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Frequency Protection (Under/Overfrequency) function. ANSI 81O/U.		
RTD Inputs	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the RTD (Resistance Temperature Device) Inputs.		
CB Fail	Disabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Circuit Breaker Fail Protection function. ANSI 50BF.		
Supervision	Disabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Supervision (VTS&CTS) functions. ANSI VTS/CTS.		
Input Labels	Visible	Invisible or Visible
Sets the Input Labels menu visible in the relay settings menu.		
Output Labels	Visible	Invisible or Visible
Sets the Output Labels menu visible in the relay settings menu.		
RTD Labels	Visible	Invisible or Visible
Sets the RTD Labels menu visible in the relay settings menu.		
CT & VT Ratios	Visible	Invisible or Visible
Sets the Current & Voltage Transformer Ratios menu visible in the relay settings menu.		

Menu text	Default setting	Available settings
Record Control	Invisible	Invisible or Visible
Sets the Record Control menu visible in the relay settings menu.		
Disturb. Recorder	Invisible	Invisible or Visible
Sets the Disturbance Recorder menu visible in the relay settings menu.		
Measure't. Set-up	Invisible	Invisible or Visible
Sets the Measurement Setup menu visible in the relay settings menu.		
Comms. Settings	Visible	Invisible or Visible
Sets the Communications Settings menu visible in the relay settings menu. These are the settings associated with the 1st and 2nd rear communications ports.		
Commission Tests	Visible	Invisible or Visible
Sets the Commissioning Tests menu visible in the relay settings menu.		
Setting Values	Primary	Primary or Secondary
This affects all protection settings that are dependent on CT and VT ratios.		
Control Inputs	Visible	Invisible or Visible
Sets the Control Inputs menu visible in the relay setting menu.		
CLIO Inputs	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the Current Loop Input Output (CLIO) Inputs function.		
CLIO Outputs	Enabled	Enabled or Disabled
Enables (activates) or disables (turns off) the CLIO Outputs function.		
Ctrl I/P Config.	Visible	Invisible or Visible
Sets the Control Input Configuration menu visible in the relay setting menu.		
Ctrl I/P Labels	Visible	Invisible or Visible
Sets the Control Input Labels menu visible in the relay setting menu.		
Direct Access	Enabled	Enabled/Disabled/Hotkey Only.
Defines what controls are available using the direct access keys - Enabled (Hotkey and CB Control functions) / Hotkey Only (Control Inputs and Setting group selection) / CB Cntrl Only (CB open/close).		
IEC GOOSE	Visible	Invisible or Visible
Sets the IEC 61850 GOOSE menu visible in the relay setting menu.		
Function Key	Visible	Invisible or Visible
Sets the Function Key menu visible in the relay setting menu.		
LCD Contrast	11	0 to 31
Sets the LCD contrast. To confirm acceptance of the contrast setting the relay prompts the user to press the right and left arrow keys together instead of the Enter key. This is an added precaution to prevent someone accidentally selecting a contrast which would leave the display black or blank. **Note** If the LCD contrast is set incorrectly as black or blank, it can be set through the front port communications port using the MiCOM S1 Studio setting software.		

Table 1 - Relay config settings

3 PROTECTION SETTINGS

The protection settings include all the following items that become active once enabled in the configuration column of the relay menu database:

- Protection element settings
- Scheme logic settings

There are four groups of protection settings, with each group containing the same setting cells. One group of protection settings is selected as the active group, and is used by the protection elements. The settings for group 1 only are shown below. The settings are discussed in the same order in which they are displayed in the menu.

4 SYSTEM CONFIG

The P64x maintains correct operation of all the protection functions through user-configurable settings.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: SYSTEM CONFIG				
Winding Config	HV+LV+TV	HV+LV HV+LV+TV		N/A
This setting indicates if the protected transformer is a two or three winding transformer.				
Winding Type	Conventional	Conventional or Auto		
The winding type may be configured as conventional or Auto. If the winding type is set as Auto, then the REF protection for autotransformer is available. If the winding type is set as conventional, then a REF protection for each winding is available.				
HV CT Terminals	01 (P642) 001 (P643) 00001 (P645)	01 (P642) 001, 011 (P643) 000001, 00011, 00111, 01011 or 01111 (P645)		N/A
01, from right to left the current inputs are T1, T2 001, from right to left the current inputs are T1, T2, T3 00001, from right to left the current inputs are T1, T2, T3, T4, T5 For further detailed connections refer to the installation section.				
LV CT Terminals	10 (P642) 100 (P643) 10000 (P645)	10 (P642) 100, 110 (P643) 10000, 11000, 11100, 11010 or 11110 (P645)		N/A
10, from right to left the current inputs are T1, T2 100, from right to left the current inputs are T1, T2, T3 10000, from right to left the current inputs are T1, T2, T3, T4, T5 For further detailed connections refer to the installation section.				
TV CT Terminals	010 (P643) 00100 (P645)	010 (P643) 00100, 00110, 01100 or 01110 (P645)		N/A
010 from right to left the current inputs are T1, T2, T3 00100 from right to left the current inputs are T1, T2, T3, T4, T5 For further detailed connections refer to the installation section.				
Ref Power S	100 MVA	0.1 MVA	5000 MVA	0.1 MVA
Reference power. Used by the differential function to calculate the ratio correction factors. Used by the thermal function when the monitored winding is set to biased current.				
HV Connection	Y-Wye	D-Delta, Y-Wye, Z-Zigzag		
The HV winding connections can be configured as Delta, Wye, or Zigzag.				
HV Grounding	Grounded	Grounded or Ungrounded		
In simple mode when set as grounded, the P64x filters the zero sequence current in the HV side. When set as ungrounded, no zero sequence filtering is done in the HV side. In advanced mode (located in DIFF PROTECTION), the HV Grounding setting is a data cell that reflects the status of the Zero seq filt HV setting.				
HV Nominal	220 kV	100 V	1 MV	1 V
Nominal voltage of the HV winding, mid-tap voltage of the on-load tap changer, or no-load tap changer tap voltage.				
HV Rating	100 MVA	0.1 MVA	5000 MVA	0.1 MVA
This rating is used by the thermal overload function if the monitored winding is set to HV.				
% Reactance	10%	1%	100%	0.1%
Transformer leakage reactance.				
LV Vector Group	0	0	11	1

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: SYSTEM CONFIG				
This is used to provide vector correction for phase shift between HV and LV windings. The HV winding is always the reference winding.				
LV Connection	Y-Wye	D-Delta, Y-Wye, Z-Zigzag		
The LV winding connections can be configured as Delta, Wye, or Zigzag.				
LV Grounding	Grounded	Grounded or Ungrounded		
In simple mode when set as grounded, the P64x filters the zero sequence current in the LV side. When set as ungrounded, no zero sequence filtering is done in the LV side. In advanced mode (located in DIFF PROTECTION), the LV Grounding setting is a data cell that reflects the status of the Zero seq filt LV setting.				
LV Nominal	220 kV	100 V	1 MV	1 V
Nominal voltage of the LV winding, mid-tap voltage of the on-load tap changer, or no-load tap changer tap voltage.				
LV Rating	100 MVA	0.1 MVA	5000 MVA	0.1 MVA
This rating is used by the thermal overload function if the monitored winding is set to LV.				
TV Vector Group	0	1	11	1
P643, 5 only. This is used to provide vector correction for phase shift between HV and TV windings. The HV winding is always the reference winding.				
TV Connection	Y-Wye	D-Delta, Y-Wye, Z-Zigzag		
P643, 5 only. The winding connections can be configured as Delta, Wye, or Zigzag.				
TV Grounding	Grounded	Grounded or Ungrounded		
P643, 5 only. In simple mode when set as grounded, the P64x filters the zero sequence current in the TV side. When set as ungrounded, no zero sequence filtering is done in the LV side. In advanced mode (located in DIFF PROTECTION), the TV Grounding setting is is a data cell that reflects the status of the Zero seq filt TV setting.				
TV Nominal	220 kV	100 V	1 MV	1 V
P643, 5 only. Nominal voltage of the TV winding.				
TV Rating	100 MVA	0.1 MVA	5000 MVA	0.1 MVA
P643, 5 only. This rating is used by the thermal overload function if the monitored winding is set to TV.				
Match Factor CT1	This is only calculated by the relay.			
Current transformer 1 matching factor. It is used to correct T1 CT current to the transformer reference load.				
Match Factor CT2	This is only calculated by the relay.			
Current transformer 2 matching factor. It is used to correct T2 CT current to the transformer reference load.				
Match Factor CT3	This is only calculated by the relay.			
Current transformer 3 matching factor. It is used to correct T3 CT current to the transformer reference load.				
Match Factor CT4	This is only calculated by the relay.			
Current transformer 4 matching factor. It is used to correct T4 CT current to the transformer reference load.				
Match Factor CT5	This is only calculated by the relay.			
Current transformer 5 matching factor. It is used to correct T5 CT current to the transformer reference load.				
Phase Sequence	Standard ABC	Standard ABC or Reverse ACB		
This sets the phase rotation. It affects the positive and negative sequence quantities calculated by the relay. It also affects functions that are dependent on phase quantities.				
VT Reversal	No Swap	No Swap, A-B Swap, B-C Swap, C-A Swap		
P643, 5 only. For applications where 2-phase voltage inputs are swapped.				
CT1 Reversal	No Swap	No Swap, A-B Swap, B-C Swap, C-A Swap		
For applications where 2-phase current inputs are swapped.				
CT2 Reversal	No Swap	No Swap, A-B Swap, B-C Swap, C-A Swap		

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: SYSTEM CONFIG				
For applications where 2-phase current inputs are swapped.				
CT3 Reversal	No Swap	No Swap, A-B Swap, B-C Swap, C-A Swap		
P643, 5 only. For applications where 2-phase current inputs are swapped.				
CT4 Reversal	No Swap	No Swap, A-B Swap, B-C Swap, C-A Swap		
P645 only. For applications where 2-phase current inputs are swapped.				
CT5 Reversal	No Swap	No Swap, A-B Swap, B-C Swap, C-A Swap		
P645 only. For applications where 2-phase current inputs are swapped.				

Table 2 - Group 1 system config settings

4.1 Differential Protection

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: DIFF PROTECTION				
Trans Diff	Enabled	Enabled or Disabled		
This enables or disables differential protection for setting group1.				
Set Mode	Simple	Simple or Advance		
If the relay is in Simple mode, zero sequence filtering is applied when HV/LV/TV Grounding setting cells under SYSTEM CONFIG menu heading are set to grounded. If the relay is in advanced mode, the zero sequence filtering is enabled or disabled in the cell [Zero seq filt HV/LV/TV] under the DIFF PROTECTION menu heading. In simple mode the relay calculates Is-HS1 as 1/Xt, where Xt is the transformer reactance and Is-HS2 is 32pu. In simple mode under DIFF PROTECTION menu heading, Zero seq filt HV/LV/TV, Is-HS1 and Is-Hs2 are data cells. In simple mode, Zero seq filt HV/LV/TV data cells reflect the status of HV/LV/TV Grounding setting cells. In advanced mode, Zero seq filt HV/LV/TV Is-HS1 and Is-HS2 are settable. In advanced mode, HV/LV/TV Grounding data cells reflect the status of Zero seq filt HV/LV/TV setting cells.				
Is1	0.2 pu	0.1 pu	2.5 pu	0.01 pu
Minimum differential threshold of the low set differential characteristic.				
K1	30%	0 %	150 %	1 %
First slope setting of the low set differential characteristic.				
Is2	1 pu	0.1 pu	10 pu	0.1 pu
Bias current threshold for the second slope of the low set differential characteristic.				
K2	80%	15 %	150 %	1 %
Second slope setting of the low set differential characteristic.				
tDIFF LS	0 s	0 s	10 s	10 ms
Low set differential element time delay				
Is-CTS	1.5 pu	0.1 pu	2.5 pu	0.01 pu
In restrain mode, the differential protection Is1 setting is increased to Is-CTS setting after CT failure is detected. The Is-CTS setting increases the restrain region of the differential characteristic.				
Is-HS1	10 pu	2.5 pu	32 pu	0.1 pu
High set differential element one. In simple mode, the relay calculates Is-HS1 as 1/Xt. Where Xt is the transformer reactance. Is-HS1 is a data cell in simple mode. In advance mode Is-HS1 is settable.				
HS2 Status	Enabled	Enabled or Disabled		
Enables or disables Is-HS2.				
Is-HS2	32 pu	2.5 pu	32 pu	0.1 pu

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: DIFF PROTECTION				
High set differential element two. In simple mode, Is-HS2 is 32pu and it is a data cell. It is settable in advance mode.				
Zero seq filt HV	Disabled	Enabled or Disabled		
Enables or disables zero sequence filtering on the HV winding. This setting is only settable in advance mode.				
Zero seq filt LV	Disabled	Enabled or Disabled		
Enables or disables zero sequence filtering on the LV winding. This setting is only settable in advance mode.				
Zero seq filt TV	Disabled	Enabled or Disabled		
Enables or disables zero sequence filtering on the TV winding. This setting is only settable in advance mode.				
2nd harm blocked	Disabled	Enabled or Disabled		
Enables or disables the 2nd harmonic blocking. This setting should only be enabled when a transformer is protected.				
Ih(2)%>	15%	5%	50%	1 %
Second harmonic blocking threshold.				
Cross blocking	Disabled	Enabled or Disabled		
Enables or disables cross blocking. If cross blocking is enabled, all three phase low set differential elements would be blocked as long as the content of second harmonic in any of the three phase differential currents is above Ih(2)% setting. If cross blocking is disabled, only the phase low set differential differential element whose content of second harmonic is above Ih(2)% setting would be blocked.				
CTSat and NoGap	Disabled	Enabled or Disabled		
Enables or disables the CT saturation logic and no gap detection algorithms.				
5th harm blocked	Disabled	Enabled or Disabled		
Enables or disables 5th harmonic blocking.				
Ih(5)%>	35%	0%	100%	1%
Fifth harmonic blocking threshold.				
Circuitry Fail	Enabled	Enabled or Disabled		
Enables or disables the circuitry fail alarm.				
Is-cctfail	0.1 pu	0.03 pu	1 pu	0.01 pu
Minimum differential threshold of the circuitry fail alarm.				
K-cctfail	10%	0 %	50%	1%
Slope for the circuitry fail alarm function.				
Tls-cctfail	5 s	0 s	10 s	0.1 s
Sets the circuitry fail alarm time delay.				

Table 3 - Group 1 DIFF protection settings

4.2 Restricted Earth Fault Protection

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: REF PROTECTION				
REF HV status	LowZ REF	Disabled, LowZ REF, HighZ REF		
Enables LowZ or HighZ REF or disables the restricted earth fault protection for the HV winding.				
Neutral CT input	TN1			
This is a data cell and it indicates that TN1 is the current input used by the HV REF function.				
HV IS1 Set	0.09 In	0.02 In	1 In	0.01 In

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: REF PROTECTION				
Minimum differential threshold of the HV low impedance REF characteristic or threshold of the HV high impedance REF.				
HV IS2 Set	0.9 In	0.1In	10 In	0.1 In
Bias current threshold for the second slope of the HV low impedance REF characteristic.				
HV IREF K1	0%	0%	150%	1%
First slope setting of the HV low impedance REF characteristic. Normally set to 0% to give optimum sensitivity for internal faults.				
HV IREF K2	150%	15%	150%	1%
Second slope setting of the HV low impedance REF characteristic. Normally set to 150% to ensure adequate restraint for external faults.				
HV tREF	0 s	0 s	10 s	10 ms
Operating time delay for the HV low impedance REF element.				
REF LV status	LowZ REF	Disabled, LowZ REF, HighZ REF		
Enables LowZ or HighZ REF or disables restricted earth fault protection for the LV winding.				
Neutral CT input	TN2			
This is a data cell and it indicates TN2 is the current input used by the LV REF function.				
LV IS1 Set	0.09 In	0.02 In	1 In	0.01 In
Minimum differential threshold of the LV low impedance REF characteristic or threshold of the LV high impedance REF.				
LV IS2 Set	0.9 In	0.1 In	10 In	0.1 In
Bias current threshold for the second slope of the LV low impedance REF characteristic.				
LV IREF K1	0%	0%	150%	1%
First slope setting of the LV low impedance REF characteristic. Normally set to 0% to give optimum sensitivity for internal faults.				
LV IREF K2	150%	15%	150%	1%
Second slope setting of the LV low impedance REF characteristic. Normally set to 150% to ensure adequate restraint for external faults.				
LV tREF	0 s	0 s	10 s	10 ms
Operating time delay for the LV low impedance REF element.				
REF TV status (P643/P645)	LowZ REF	Disabled, LowZ REF, HighZ REF		
Enables LowZ or HighZ REF or disables restricted earth fault protection for the TV winding.				
Neutral CT input	TN3			
This is a data cell and it indicates TN3 is the current input used by the TV REF function.				
TV IS1 Set	0.09 In	0.02 In	1 In	0.01 In
Minimum differential threshold of the TV low impedance REF characteristic or threshold of the TV high impedance REF.				
TV IS2 Set	0.9 In	0.1 In	10 In	0.1 In
Bias current threshold for the second slope of the TV low impedance REF characteristic.				
TV IREF K1	0%	0%	150%	1%
First slope setting of the TV low impedance REF characteristic. Normally set to 0% to give optimum sensitivity for internal faults.				
TV IREF K2	150%	15%	150%	1%
Second slope setting of the TV low impedance REF characteristic. Normally set to 150% to ensure adequate restraint for external faults.				
TV tREF	0 s	0 s	10 s	10 ms
Operating time delay for TV low impedance REF element.				
REF auto status (P643/P645)	LowZ REF	Disabled, LowZ REF, HighZ REF		

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP1: REF PROTECTION				
Enables LowZ or HighZ REF or disables the autotransformer restricted earth fault protection.				
Neutral CT input	TN1			
This is a data cell and it indicates TN1 is the current input used by the auto transformer REF function.				
Auto IS1 Set	0.09 In	0.02 In	1 In	0.01 In
Minimum differential threshold of the auto low impedance REF characteristic or threshold of the auto high impedance REF.				
Auto IS2 Set	0.9 In	0.1 In	10 In	0.1 In
Bias current threshold for the second slope of the auto low impedance REF characteristic.				
Auto IREF K1	0%	0%	150%	1%
First slope setting of the auto low impedance REF characteristic. Normally set to 0% to give optimum sensitivity for internal faults.				
Auto TV IREF K2	150%	15%	150%	1%
Second slope setting of the auto low impedance REF characteristic. Normally set to 150% to ensure adequate restraint for external faults.				
Auto TV tREF	0 s	0 s	10 s	10 ms
Operating time delay for auto low impedance REF element.				
Note The table describing the REF protection shows the default settings and the settings range of XX IS1 Set and XX IS2 Set in pu of the line CT primary current. In MiCOM S1 Studio or MiCOM S1, these settings are actually in secondary or primary amperes.				

Table 4 - Group 1 REF protection settings

4.3 NPS Overcurrent

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: NPS OVERCURRENT				
NPS O/C 1	T1	Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5		
Sets the current signal used by the negative phase sequence overcurrent element 1.				
I2>1 Status	Disabled	Enabled or Disabled		
Enables or disables the stage 1 of NPS element 1.				
I2>1 Char	DT	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)		
Setting for the tripping characteristic for stage 1 NPS element 1.				
I2>1 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Determines the direction of measurement for this element. In the P643/P645 the three phase VT input is required to set I2>1 as directional. In the P642 two single phase VTs are required to set I2>1 as directional.				
I2>1 Current Set	0.2 In	0.08 In	4 In	0.01 In
Current pick-up setting for the stage 1 of NPS overcurrent element 1.				
I2>1 Time Delay	10 s	0 s	100 s	0.01 s
Operating time delay for the stage 1 of NPS overcurrent element 1.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: NPS OVERCURRENT				
I2>1 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
I2>1 Time Dial	1	0.01	100	0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
I2>1 K(RI)	1	0.1	10	0.05
Setting for the time multiplier to adjust the operating time for the RI curve.				
I2>1 Reset Char	DT	DT or Inverse		
Setting to determine the type of reset/release characteristic of the IEEE/US curves.				
I2>1 tReset	0 s	0 s	100 s	0.01 s
Setting that determines the reset/release time for definite time reset characteristic.				
I2>2 Status	Disabled	Enabled or Disabled		
Enables or disables the stage 2 of NPS element 1				
I2>2 Char	DT	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)		
Setting for the tripping characteristic for stage 2 NPS element 1.				
I2>2 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Determines the direction of measurement for this element. In the P643/P645 the three phase VT input is required to set I2>2 as directional. In the P642 two single phase VTs are required to set I2>2 as directional.				
I2>2 Current Set	0.2 In	0.08 In	4 In	0.01 In
Current pick-up setting for the stage 2 of NPS overcurrent element 1.				
I2>2 Time Delay	10 s	0 s	100 s	0.01 s
Operating time delay for the stage 2 of NPS overcurrent element 1.				
I2>2 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
I2>2 Time Dial	1	0.01	100	0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
I2>2 K(RI)	1	0.1	10	0.05
Setting for the time multiplier to adjust the operating time for the RI curve.				
I2>2 Reset Char	DT	DT or Inverse		
Setting to determine the type of reset/release characteristic of the IEEE/US curves.				
I2>3 Status	Disabled	Enabled or Disabled		
Enables or disables the stage 3 of NPS element 1				
I2>3 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Determines the direction of measurement for this element. In the P643/P645 the three phase VT input is required to set I2>3 as directional. In the P642 two single phase VTs are required to set I2>3 as directional.				
I2>3 Current Set	0.2 In	0.08 In	4 In	0.01 In
Current pick-up setting for the stage 3 of NPS element 1.				
I2>3 Time Delay	10 s	0 s	100 s	0.01 s

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: NPS OVERCURRENT				
Operating time delay for the stage 3 NPS overcurrent element 1.				
I2>4 Status	Disabled	Enabled or Disabled		
Enables or disables the stage 4 of NPS element 1.				
I2>4 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Determines the direction of measurement for this element. In the P643/P645 the three phase VT input is required to set I2>4 as directional. In the P642 two single phase VTs are required to set I2>4 as directional.				
I2>4 Current Set	0.2 In	0.08 In	4 In	0.01 In
Current pick-up setting for the stage 4 of NPS element 1.				
I2>4 Time Delay	10 s	0 s	100 s	0.01 s
Operating time delay for the stage 4 of NPS element 1.				
I2> VTS Block	1111	Bit 00 = VTS blocks I2>1 Bit 01 = VTS blocks I2>2 Bit 02 = VTS blocks I2>3 Bit 03 = VTS blocks I2>4		
Logic settings that determine whether VT supervision will block selected negative sequence overcurrent stages. VTS Block only affects directional overcurrent protection. Setting 0 allows continued non-directional operation.				
I2> V2pol Set	5*V1	0.5 V1	25 V1	0.5 V1
The minimum threshold above which the relay must detect a polarizing voltage for the negative phase sequence directional elements to operate.				
I2> Char deg	-60 deg	-95 deg	95 deg	1 deg
Characteristic angle for directionalized NPS overcurrent protection.				
NPS O/C 2	T2 (P642) T3 (P643) T5 (P645)	Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5		
Sets the current signal used by the negative phase sequence overcurrent element 2.				
I2>1 Status	Disabled	Enabled or Disabled		
Enables or disables the stage 1 of NPS element 2.				
I2>1 Char	DT	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)		
Setting for the tripping characteristic for stage 1 NPS element 2.				
I2>1 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Determines the direction of measurement for this element. In the P643/P645 the three phase VT input is required to set I2>1 as directional. In the P642 two single phase VTs are required to set I2>1 as directional.				
I2>1 Current Set	0.2 In	0.08 In	4 In	0.01 In
Current pick-up setting for the stage 1 of NPS overcurrent element 2.				
I2>1 Time Delay	10 s	0 s	100 s	0.01 s
Operating time delay for the stage 1 of NPS overcurrent element 2.				
I2>1 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
I2>1 Time Dial	1	0.01	100	0.01

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: NPS OVERCURRENT				
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
I2>1 K(RI)	1	0.1	10	0.05
Setting for the time multiplier to adjust the operating time for the RI curve.				
I2>1 Reset Char	DT	DT or Inverse		
Setting to determine the type of reset/release characteristic of the IEEE/US curves.				
I2>1 tReset	0 s	0 s	100 s	0.01 s
Setting that determines the reset/release time for definite time reset characteristic.				
I2>2 Status	Disabled	Enabled or Disabled		
Enables or disables the stage 2 of NPS element 2				
I2>2 Char	DT	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)		
Setting for the tripping characteristic for stage 2 NPS element 2.				
I2>2 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Determines the direction of measurement for this element. In the P643/P645 the three phase VT input is required to set I2>2 as directional. In the P642 two single phase VTs are required to set I2>2 as directional.				
I2>2 Current Set	0.2 In	0.08 In	4 In	0.01 In
Current pick-up setting for the stage 2 of NPS overcurrent element 2.				
I2>2 Time Delay	10 s	0 s	100 s	0.01 s
Operating time delay for the stage 2 of NPS overcurrent element 2.				
I2>2 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
I2>2 Time Dial	1	0.01	100	0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
I2>2 K(RI)	1	0.1	10	0.05
Setting for the time multiplier to adjust the operating time for the RI curve.				
I2>2 Reset Char	DT	DT or Inverse		
Setting to determine the type of reset/release characteristic of the IEEE/US curves.				
I2>3 Status	Disabled	Enabled or Disabled		
Enables or disables the stage 3 of NPS element 2				
I2>3 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Determines the direction of measurement for this element. In the P643/P645 the three phase VT input is required to set I2>3 as directional. In the P642 two single phase VTs are required to set I2>3 as directional.				
I2>3 Current Set	0.2 In	0.08 In	4 In	0.01 In
Current pick-up setting for the stage 3 of NPS element 2.				
I2>3 Time Delay	10 s	0 s	100 s	0.01 s
Operating time delay for the stage 3 of NPS overcurrent element 2.				
I2>4 Status	Disabled	Enabled or Disabled		
Enables or disables the stage 4 of NPS element 2.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: NPS OVERCURRENT				
I2>4 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Determines the direction of measurement for this element. In the P643/P645 the three phase VT input is required to set I2>4 as directional. In the P642 two single phase VTs are required to set I2>4 as directional.				
I2>4 Current Set	0.2 In	0.08 In	4 In	0.01 In
Current pick-up setting for the stage 4 of NPS element 2.				
I2>4 Time Delay	10 s	0 s	100 s	0.01 s
Operating time delay for the stage 4 of NPS element 2.				
I2> VTS Block	1111	Bit 00 = VTS blocks I2>1 Bit 01 = VTS blocks I2>2 Bit 02 = VTS blocks I2>3 Bit 03 = VTS blocks I2>4		
Logic settings that determine whether VT supervision will block selected negative sequence overcurrent stages. VTS Block only affects directional overcurrent protection. Setting 0 allows continued non-directional operation.				
I2> V2pol Set	5*V1	0.5*V1	25*V1	0.5*V1
The minimum threshold above which the relay must detect a polarizing voltage for the negative phase sequence directional elements to operate.				
I2> Char deg	-60 deg	-95 deg	95 deg	1 deg
Characteristic angle for directionalized NPS fault protection.				
NPS O/C 3 (P643/P645)	T2 (P643) T3 (P645)	Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5		
Sets the current signal used by the negative phase sequence overcurrent element 2.				
I2>1 Status	Disabled	Enabled or Disabled		
Enables or disables the stage 1 of NPS element 3.				
I2>1 Char	DT	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)		
Setting for the tripping characteristic for stage 1 NPS element 3.				
I2>1 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Determines the direction of measurement for this element. In the P643/P645 the three phase VT input is required to set I2>1 as directional.				
I2>1 Current Set	0.2 In	0.08 In	4In	0.01In
Current pick-up setting for the stage 1 of NPS overcurrent element 3.				
I2>1 Time Delay	10 s	0 s	100 s	0.01 s
Operating time delay for the stage 1 of NPS overcurrent element 3.				
I2>1 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
I2>1 Time Dial	1	0.01	100	0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
I2>1 K(RI)	1	0.1	10	0.05
Setting for the time multiplier to adjust the operating time for the RI curve.				
I2>1 Reset Char	DT	DT or Inverse		

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: NPS OVERCURRENT				
Setting to determine the type of reset/release characteristic of the IEEE/US curves.				
I2>1 tReset	0 s	0 s	100 s	0.01 s
Setting that determines the reset/release time for definite time reset characteristic.				
I2>2 Status	Disabled	Enabled or Disabled		
Enables or disables the stage 2 of NPS element 3				
I2>2 Char	DT	DT (DT), IEC S Inverse (TMS), IEC V Inverse (TMS), IEC E Inverse (TMS), UK LT Inverse (TMS), Rectifier (TMS), RI (K), IEEE M Inverse (TD), IEEE V Inverse (TD), IEEE E Inverse (TD), US Inverse (TD) or US ST Inverse (TD)		
Setting for the tripping characteristic for stage 2 NPS element 3.				
I2>2 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Determines the direction of measurement for this element. In the P643/P645 the three phase VT input is required to set I2>2 as directional.				
I2>2 Current Set	0.2 In	0.08 In	4 In	0.01 In
Current pick-up setting for the stage 2 of NPS overcurrent element 3.				
I2>2 Time Delay	10 s	0 s	100 s	0.01 s
Operating time delay for the stage 2 of NPS overcurrent element 3.				
I2>2 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
I2>2 Time Dial	1	0.01	100	0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
I2>2 K(RI)	1	0.1	10	0.05
Setting for the time multiplier to adjust the operating time for the RI curve.				
I2>2 Reset Char	DT	DT or Inverse		
Setting to determine the type of reset/release characteristic of the IEEE/US curves.				
I2>3 Status	Disabled	Enabled or Disabled		
Enables or disables the stage 3 of NPS element 3				
I2>3 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Determines the direction of measurement for this element. In the P643/P645 the three phase VT input is required to set I2>3 as directional.				
I2>3 Current Set	0.2 In	0.08 In	4 In	0.01 In
Current pick-up setting for the stage 3 of NPS element 3.				
I2>3 Time Delay	10 s	0 s	100 s	0.01 s
Operating time delay for the stage 3 of NPS overcurrent element 3.				
I2>4 Status	Disabled	Enabled or Disabled		
Enables or disables the stage 4 of NPS element 3.				
I2>4 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Determines the direction of measurement for this element. In the P643/P645 the three phase VT input is required to set I2>4 as directional.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: NPS OVERCURRENT				
I2>4 Current Set	0.2 In	0.08 In	4 In	0.01 In
Current pick-up setting for the stage 4 of NPS element 3.				
I2>4 Time Delay	10 s	0 s	100 s	0.01 s
Operating time delay for the stage 4 of NPS element 3.				
I2> VTS Block	1111	Bit 00 = VTS blocks I2>1 Bit 01 = VTS blocks I2>2 Bit 02 = VTS blocks I2>3 Bit 03 = VTS blocks I2>4		
Logic settings that determine whether VT supervision will block selected negative sequence overcurrent stages. VTS Block only affects directional overcurrent protection. Setting 0 allows continued non-directional operation.				
I2> V2pol Set	5*V1	0.5*V1	25*V1	0.5*V1
The minimum threshold above which the relay must detect a polarizing voltage for the negative phase sequence directional elements to operate.				
I2> Char deg	-60 deg	-95 deg	95 deg	1 deg
Characteristic angle for directionalized NPS fault protection.				

Table 5 - Group 1 NPS overcurrent settings

4.4 Overcurrent

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: OVERCURRENT				
Overcurrent 1	T1	Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5		
Sets the current signal used by the overcurrent element 1.				
I>1 Status	Disabled	Enabled or disabled		
Setting to enable or disable stage 1 of overcurrent element 1.				
I>1 Char	IEC S Inverse	Disabled, DT (DT), IEC S Inverse (TMS) IEC V Inverse (TMS), IEC E Inverse (TMS) UK LT Inverse (TMS), UK Rectifier (TMS) RI (K), IEEE M Inverse (TD) IEEE V Inverse (TD), IEEE E Inverse (TD) US Inverse (TD), US ST Inverse (TD)		
Setting for the tripping characteristic for stage 1 of overcurrent element 1.				
I>1 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Sets the directionality for stage 1 of overcurrent element 1. In the P643/P645 the three phase VT input is required to set I>1 as directional. In the P642 two single phase VTs are required to set I>1 as directional.				
I>1 Current Set	1 In	0.08 In	4 In	0.01 In
Pick-up setting for stage 1 of overcurrent element 1.				
I>1 Time Delay	1 s	0 s	100 s	0.01 s
Time delay setting for stage 1 of overcurrent element 1 when the characteristic is set as definite time.				
I>1 TMS	1	0.025	1.2	0.025
Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: OVERCURRENT				
I>1 Time Dial	1	0.01	100	0.01
Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
I>1 K (RI)	1	0.1	10	0.05
Setting for the time multiplier to adjust the operating time for the RI curve.				
I>1 Reset Char	DT	DT or Inverse		
Setting to determine the type of reset/release characteristic of the IEEE/US curves.				
I>1 tRESET	0 s	0 s	100 s	0.01 s
Setting that determines the reset/release time for definite time reset characteristic.				
I>2 Status	Disabled	Enabled or disabled		
Setting to enable or disable stage 2 of overcurrent element 1.				
I>2 Char	Disabled	Disabled, DT (DT), IEC S Inverse (TMS) IEC V Inverse (TMS), IEC E Inverse (TMS) UK LT Inverse (TMS), UK Rectifier (TMS) RI (K), IEEE M Inverse (TD) IEEE V Inverse (TD), IEEE E Inverse (TD) US Inverse (TD), US ST Inverse (TD)		
Setting for the tripping characteristic for stage 2 of overcurrent element 1.				
I>2 Direction	Non-Directional	Non-Directional Directional Fwd Directional Rev		
Sets the directionality for stage 2 of overcurrent element 1. In the P643/P645 the three phase VT input is required to set I>2 as directional. In the P642 two single phase VTs are required to set I>2 as directional.				
I>2 Current Set	1 In	0.08 In	4 In	0.01 In
Pick-up setting for stage 2 of overcurrent element 1.				
I>2 Time Delay	1 s	0 s	100 s	0.01 s
Time delay setting for stage 2 of overcurrent element 1 when the characteristic is set as definite time.				
I>2 TMS	1	0.025	1.2	0.025
Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
I>2 Time Dial	1	0.01	100	0.01
Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
I>2 K (RI)	1	0.1	10	0.05
Setting for the time multiplier to adjust the operating time for the RI curve.				
I>2 Reset Char	DT	DT or Inverse		
Setting to determine the type of reset/release characteristic of the IEEE/US curves.				
I>2 tRESET	0 s	0 s	100 s	0.01 s
Setting that determines the reset/release time for definite time reset characteristic.				
I>3 Status	Disabled	Enabled or Disabled		
Setting to enable or disable stage 3 of overcurrent element 1.				
I>3 Direction	Non-Directional	Non-Directional Directional Fwd Directional Rev		
Sets the directionality for stage 3 of overcurrent element 1. In the P643/P645 the three phase VT input is required to set I>3 as directional. In the P642 two single phase VTs are required to set I>3 as directional.				
I>3 Current Set	1 In	0.08 In	32 In	0.01 In
Pick-up setting for stage 3 of overcurrent element 1.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: OVERCURRENT				
I>3 Time Delay	0 s	0 s	100 s	0.01 s
Time delay setting for stage 3 of overcurrent element 1.				
I>4 Status	Disabled	Enabled or Disabled		
Setting to enable or disable the stage 4 of overcurrent element 1.				
I>4 Direction	Non-Directional	Non-Directional Directional Fwd Directional Rev		
Sets the directionality for stage 4 of overcurrent element 1. In the P643/P645 the three phase VT input is required to set I>4 as directional. In the P642 two single phase VTs are required to set I>4 as directional.				
I>4 Current Set	1In	0.08In	32In	0.01In
Pick-up setting for stage 4 of overcurrent element 1.				
I>4 Time Delay	0 s	0 s	100 s	0.01 s
Time delay setting for stage 4 of overcurrent element 1.				
I> Char Angle	30 deg	-95 deg	95 deg	1 deg
Setting for the relay characteristic angle used for the directional decision.				
I> Function Link	1111	Bit 00 = VTS blocks I>1 Bit 01 = VTS blocks I>2 Bit 02 = VTS blocks I>3 Bit 03 = VTS blocks I>4		
Logic Settings that determine whether blocking signals from VT supervision affect certain overcurrent stages.				
Overcurrent 2	T2 (P642) T3 (P643) T5 (P645)	Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5		
Sets the current signal used by the overcurrent element 2.				
I>1 Status	Disabled	Enabled or disabled		
Setting to enable or disable stage 1 of overcurrent element 2.				
I>1 Char	IEC S Inverse	Disabled, DT (DT), IEC S Inverse (TMS) IEC V Inverse (TMS), IEC E Inverse (TMS) UK LT Inverse (TMS), UK Rectifier (TMS) RI (K), IEEE M Inverse (TD) IEEE V Inverse (TD), IEEE E Inverse (TD) US Inverse (TD), US ST Inverse (TD)		
Setting for the tripping characteristic for stage 1 of overcurrent element 2.				
I>1 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Sets the directionality for stage 1 of overcurrent element 2. In the P643/P645 the three phase VT input is required to set I>1 as directional. In the P642 two single phase VTs are required to set I>1 as directional.				
I>1 Current Set	1 In	0.08 In	4 In	0.01 In
Pick-up setting for stage 1 of overcurrent element 2.				
I>1 Time Delay	1 s	0	100 s	0.01 s
Time delay setting for stage 1 of overcurrent element 2 when the characteristic is set as definite time.				
I>1 TMS	1	0.025	1.2	0.025
Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
I>1 Time Dial	1	0.01	100	0.01
Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: OVERCURRENT				
I>1 K (RI)	1	0.1	10	0.05
Setting for the time multiplier to adjust the operating time for the RI curve.				
I>1 Reset Char	DT	DT or Inverse		
Setting to determine the type of reset/release characteristic of the IEEE/US curves.				
I>1 tRESET	0 s	0 s	100 s	0.01 s
Setting that determines the reset/release time for definite time reset characteristic.				
I>2 Status	Disabled	Enabled or disabled		
Setting to enable or disable stage 2 of overcurrent element 2.				
I>2 Char	Disabled	Disabled, DT (DT), IEC S Inverse (TMS) IEC V Inverse (TMS), IEC E Inverse (TMS) UK LT Inverse (TMS), UK Rectifier (TMS) RI (K), IEEE M Inverse (TD) IEEE V Inverse (TD), IEEE E Inverse (TD) US Inverse (TD), US ST Inverse (TD)		
Setting for the tripping characteristic for stage 2 of overcurrent element 2.				
I>2 Direction	Non-Directional	Non-Directional Directional Fwd Directional Rev		
Sets the directionality for stage 2 of overcurrent element 2. In the P643/P645 the three phase VT input is required to set I>2 as directional. In the P642 two single phase VTs are required to set I>2 as directional.				
I>2 Current Set	1 In	0.08 In	4 In	0.01 In
Pick-up setting for stage 2 of overcurrent element 2.				
I>2 Time Delay	1 s	0 s	100 s	0.01 s
Time delay setting for stage 2 of overcurrent element 2 when the characteristic is set as definite time.				
I>2 TMS	1	0.025	1.2	0.025
Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
I>2 Time Dial	1	0.01	100	0.01
Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
I>2 K (RI)	1	0.1	10	0.05
Setting for the time multiplier to adjust the operating time for the RI curve.				
I>2 Reset Char	DT	DT or Inverse		
Setting to determine the type of reset/release characteristic of the IEEE/US curves.				
I>2 tRESET	0 s	0 s	100 s	0.01 s
Setting that determines the reset/release time for definite time reset characteristic.				
I>3 Status	Disabled	Enabled or Disabled		
Setting to enable or disable stage 3 of overcurrent element 2.				
I>3 Direction	Non-Directional	Non-Directional Directional Fwd Directional Rev		
Sets the directionality for stage 3 of overcurrent element 2. In the P643/P645 the three phase VT input is required to set I>3 as directional. In the P642 two single phase VTs are required to set I>3 as directional.				
I>3 Current Set	1 In	0.08 In	32 In	0.01 In
Pick-up setting for stage 3 of overcurrent element 2.				
I>3 Time Delay	0 s	0 s	100 s	0.01 s
Time delay setting for stage 3 of overcurrent element 2.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: OVERCURRENT				
I>4 Status	Disabled	Enabled or Disabled		
Setting to enable or disable the stage 4 of overcurrent element 2.				
I>4 Direction	Non-Directional	Non-Directional Directional Fwd Directional Rev		
Sets the directionality for stage 4 of overcurrent element 2. In the P643/P645 the three phase VT input is required to set I>4 as directional. In the P642 two single phase VTs are required to set I>4 as directional.				
I>4 Current Set	1 In	0.08 In	32 In	0.01 In
Pick-up setting for stage 4 of overcurrent element 2.				
I>4 Time Delay	0 s	0 s	100 s	0.01 s
Time delay setting for stage 4 of overcurrent element 2.				
I> Char Angle	30 deg	-95 deg	95 deg	1 deg
Setting for the relay characteristic angle used for the directional decision.				
I> Function Link	1111	Bit 00 = VTS blocks I>1 Bit 01 = VTS blocks I>2 Bit 02 = VTS blocks I>3 Bit 03 = VTS blocks I>4		
Logic Settings that determine whether blocking signals from VT supervision affect certain overcurrent stages.				
Overcurrent 3	T2 (P643) T3 (P645)	Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5		
Sets the current signal used by the overcurrent element 3.				
I>1 Status	Disabled	Enabled or disabled		
Setting to enable or disable stage 1 of overcurrent element 3.				
I>1 Char	IEC S Inverse	Disabled, DT (DT), IEC S Inverse (TMS) IEC V Inverse (TMS), IEC E Inverse (TMS) UK LT Inverse (TMS), UK Rectifier (TMS) RI (K), IEEE M Inverse (TD) IEEE V Inverse (TD), IEEE E Inverse (TD) US Inverse (TD), US ST Inverse (TD)		
Setting for the tripping characteristic for stage 1 of overcurrent element 3.				
I>1 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Sets the directionality for stage 1 of overcurrent element 3. In the P643/P645 the three phase VT input is required to set I>1 as directional. In the P642 two single phase VTs are required to set I>1 as directional.				
I>1 Current Set	1 In	0.08 In	4 In	0.01 In
Pick-up setting for stage 1 of overcurrent element 3.				
I>1 Time Delay	1 s	0 s	100 s	0.01 s
Time delay setting for stage 1 of overcurrent element 3 when the characteristic is set as definite time.				
I>1 TMS	1	0.025	1.2	0.025
Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
I>1 Time Dial	1	0.01	100	0.01
Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
I>1 K (RI)	1	0.1	10	0.05
Setting for the time multiplier to adjust the operating time for the RI curve.				
I>1 Reset Char	DT	DT or Inverse		

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: OVERCURRENT				
Setting to determine the type of reset/release characteristic of the IEEE/US curves.				
I>1 tRESET	0 s	0 s	100 s	0.01 s
Setting that determines the reset/release time for definite time reset characteristic.				
I>2 Status	Disabled	Enabled or disabled		
Setting to enable or disable stage 2 of overcurrent element 3.				
I>2 Char	Disabled	Disabled, DT (DT), IEC S Inverse (TMS) IEC V Inverse (TMS), IEC E Inverse (TMS) UK LT Inverse (TMS), UK Rectifier (TMS) RI (K), IEEE M Inverse (TD) IEEE V Inverse (TD), IEEE E Inverse (TD) US Inverse (TD), US ST Inverse (TD)		
Setting for the tripping characteristic for stage 2 of overcurrent element 3.				
I>2 Direction	Non-Directional	Non-Directional Directional Fwd Directional Rev		
Sets the directionality for stage 2 of overcurrent element 3. In the P643/P645 the three phase VT input is required to set I>2 as directional. In the P642 two single phase VTs are required to set I>2 as directional.				
I>2 Current Set	1 In	0.08 In	4 In	0.01 In
Pick-up setting for stage 2 of overcurrent element 3.				
I>2 Time Delay	1 s	0 s	100 s	0.01 s
Time delay setting for stage 2 of overcurrent element 3 when the characteristic is set as definite time.				
I>2 TMS	1	0.025	1.2	0.025
Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
I>2 Time Dial	1	0.01	100	0.01
Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
I>2 K (RI)	1	0.1	10	0.05
Setting for the time multiplier to adjust the operating time for the RI curve.				
I>2 Reset Char	DT	DT or Inverse		
Setting to determine the type of reset/release characteristic of the IEEE/US curves.				
I>2 tRESET	0 s	0 s	100 s	0.01 s
Setting that determines the reset/release time for definite time reset characteristic.				
I>3 Status	Disabled	Enabled or Disabled		
Setting to enable or disable stage 3 overcurrent element 3.				
I>3 Direction	Non-Directional	Non-Directional Directional Fwd Directional Rev		
Sets the directionality for stage 3 of overcurrent element 3. In the P643/P645 the three phase VT input is required to set I>3 as directional. In the P642 two single phase VTs are required to set I>3 as directional.				
I>3 Current Set	1 In	0.08 In	32 In	0.01 In
Pick-up setting for stage 3 overcurrent element 3.				
I>3 Time Delay	0 s	0 s	100 s	0.01 s
Time delay setting for stage 3 of overcurrent element 3.				
I>4 Status	Disabled	Enabled or Disabled		
Setting to enable or disable the stage 4 of overcurrent element 3.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: OVERCURRENT				
I>4 Direction	Non-Directional	Non-Directional Directional Fwd Directional Rev		
Sets the directionality for stage 4 of overcurrent element 3. In the P643/P645 the three phase VT input is required to set I>4 as directional. In the P642 two single phase VTs are required to set I>4 as directional.				
I>4 Current Set	1 In	0.08 In	32 In	0.01 In
Pick-up setting for stage 4 of overcurrent element 3.				
I>4 Time Delay	0 s	0 s	100 s	0.01 s
Time delay setting for stage 4 of overcurrent element 3.				
Setting for the operating time-delay for stage 4 of overcurrent element 3.				
I> Char Angle	30 deg	-95 deg	95 deg	1 deg
Setting for the relay characteristic angle used for the directional decision.				
I> Function Link	1111	Bit 00 = VTS blocks I>1 Bit 01 = VTS blocks I>2 Bit 02 = VTS blocks I>3 Bit 03 = VTS blocks I>4		
Logic Settings that determine whether blocking signals from VT supervision affect certain overcurrent stages.				
V Controlled O/C				
VCO>1	Disabled	Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5		
Sets the current signal used by the stage 1 of voltage controlled overcurrent.				
VCO>1 Char	Disabled	Disabled, DT (DT), IEC S Inverse (TMS) IEC V Inverse (TMS), IEC E Inverse (TMS) UK LT Inverse (TMS), UK Rectifier (TMS) RI (K), IEEE M Inverse (TD) IEEE V Inverse (TD), IEEE E Inverse (TD) US Inverse (TD), US ST Inverse (TD)		
Setting for the tripping characteristic for stage 1 of voltage controlled overcurrent element.				
VCO >1 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Sets the directionality for stage 1 of voltage controlled overcurrent element. In the P643/P645 the three phase VT input is required to set VCO >1 as directional. In the P642 two single phase VTs are required to set VCO >1 as directional.				
VCO >1 Current Set	1 In	0.08 In	4 In	0.01 In
Pick-up setting for stage 1 of voltage controlled overcurrent element.				
VCO >1 Time Delay	1 s	0 s	100 s	0.01 s
Time delay setting for stage 1 of voltage controlled overcurrent element when the characteristic is set as definite time.				
VCO >1 TMS	1	0.025	1.2	0.025
Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
VCO >1 Time Dial	1	0.01	100	0.01
Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
VCO >1 K (RI)	1	0.1	10	0.05
Setting for the time multiplier to adjust the operating time for the RI curve.				
VCO >1 Reset Char	DT	DT or Inverse		
Setting to determine the type of reset/release characteristic of the IEEE/US curves.				
VCO >1 tRESET	0 s	0 s	100 s	0.01 s

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: OVERCURRENT				
Setting that determines the reset/release time for definite time reset characteristic.				
VCO>1 Char Angle	30 deg	-95 deg	95 deg	1 deg
Setting for the relay characteristic angle used for the directional decision.				
VCO>1 V< Set	80 V	5 V	120 V	1 V
Undervoltage setting for the stage 1 voltage controlled overcurrent.				
VCO>1 K Set	0.25	0.1	1	0.05
K multiplier setting. When the voltage drops below VCO>1 V< Set, VCO >1 Current Set is multiplied by VCO>1 K Set.				
VCO>2	Disabled	Disabled, HV Winding, LV Winding, TV Winding, T1, T2, T3, T4 or T5		
Sets the current signal used by the stage 2 of voltage controlled overcurrent.				
VCO>2 Char	Disabled	Disabled, DT (DT), IEC S Inverse (TMS) IEC V Inverse (TMS), IEC E Inverse (TMS) UK LT Inverse (TMS), UK Rectifier (TMS) RI (K), IEEE M Inverse (TD) IEEE V Inverse (TD), IEEE E Inverse (TD) US Inverse (TD), US ST Inverse (TD)		
Setting for the tripping characteristic for stage 2 of voltage controlled overcurrent element.				
VCO >2 Direction	Non-Directional	Non-directional Directional Fwd Directional Rev		
Sets the directionality for stage 2 of voltage controlled overcurrent element. In the P643/P645 the three phase VT input is required to set VCO >2 as directional. In the P642 two single phase VTs are required to set VCO >2 as directional.				
VCO >2 Current Set	1 In	0.08 In	4 In	0.01 In
Pick-up setting for stage 1 of voltage controlled overcurrent element.				
VCO >2 Time Delay	1 s	0 s	100 s	0.01 s
Time delay setting for stage 2 of voltage controlled overcurrent element when the characteristic is set as definite time.				
VCO >2 TMS	1	0.025	1.2	0.025
Setting for the time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
VCO >2 Time Dial	1	0.01	100	0.01
Setting for the time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
VCO >2 K (RI)	1	0.1	10	0.05
Setting for the time multiplier to adjust the operating time for the RI curve.				
VCO >2 Reset Char	DT	DT or Inverse		
Setting to determine the type of reset/release characteristic of the IEEE/US curves.				
VCO >2 tRESET	0 s	0 s	100 s	0.01 s
Setting that determines the reset/release time for definite time reset characteristic.				
VCO>2 Char Angle	30 deg	-95 deg	95 deg	1 deg
Setting for the relay characteristic angle used for the directional decision.				
VCO>2 V< Set	80 V	5 V	120 V	1 V
Undervoltage setting for the stage 2 voltage controlled overcurrent.				
VCO>2 K Set	0.25	0.1	1	0.05
K multiplier setting. When the voltage drops below VCO>2 V< Set, VCO >2 Current Set is multiplied by VCO>2 K Set.				

Table 6 - Group 1 overcurrent settings

4.5 Thermal Overload

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: THERMAL OVERLOAD				
Mon’t Winding	HV	HV, LV, TV, Biased Current		
An overall through loading picture of the transformer is provided when the monitor winding is set to Biased Current				
Ambient T	AVERAGE	RTD 1 to 10, CLIO1 to 4, AVERAGE		
Ambient temperature.				
Amb CLIO Type	4-20 mA	0-1 mA, 0-10 mA, 0-20 mA, 4-20 mA		
This setting is available when Ambient T is set to CLIOx.				
Amb CLIO Min	0	-9999	9999	0.1
This setting is available when Ambient T is set to CLIOx.				
Amb CLIO Max	100	-9999	9999	0.1
This setting is available when Ambient T is set to CLIOx.				
Average Amb T	25°C	-25°C	75°C	0.1°C
This setting is available when Ambient T is set to Average.				
Top Oil T	CALCULATED	RTD 1 to 10, CLIO1 to 4, CALCULATED		
The top oil temperature may be calculated by the relay, or it may be measured using RTD or CLIO inputs.				
Top Oil CLIO Typ	4-20 mA	0-1 mA 0-10 mA 0-20 mA 4-20 mA		
This setting is available when Top Oil T is set to CLIOx.				
Top Oil CLIO Min	0	-9999	9999	0.1
This setting is available when Top Oil T is set to CLIOx.				
Top Oil CLIO Max	100	-9999	9999	0.1
This setting is available when Top Oil T is set to CLIOx.				
IB	1 pu	0.1 pu	4 pu	0.01 pu
The relay uses this setting to calculate the ratio of ultimate load to rated load.				
Rated NoLoadLoss	3	0.1	100	0.1
Ratio of load loss at rated load to no-load loss (iron loss). The transformer manufacturer should provide this parameter.				
Hot Spot Overtop	25°C	0.1°C	200°C	0.1°C
Hottest spot temperature over top oil temperature setting. The transformer manufacturer should provide this parameter.				
Top Oil Overamb	55°C	0.1°C	200°C	0.1°C
Top oil temperature over ambient temperature setting. The transformer manufacturer should provide this parameter.				
Cooling mode	Cooling mode 1	Cooling mode 1, Cooling mode 2, Cooling mode 3, Cooling mode 4, Select via PSL		
Four cooling modes are available and they can be selected either via PSL or via the setting file. To select the cooling mode via the setting file, set one of the four cooling mode options available. To select the cooling mode via PSL set Cooling mode to Select via PSL and configure DDBs CM Select 1X and CM Select X1 in the psl file.				
Cooling Status	Cooing mode 1			
Cooling Status is a data cell and it indicates which of the cooling modes is being used by the thermal function.				
Cooling mode 1				
Winding exp m	0.8	0.01	2	0.01

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: THERMAL OVERLOAD				
Winding exponent. It is an empirically derived exponent used to calculate the variation of the winding hottest-spot rise over top-oil temperature with changes in load. To set m use the suggested values given in IEEE Std. C57.91-1995 (see the application chapter for suggested values), or ask the transformer manufacturer for advice.				
Oil exp n	0.8	0.01	2	0.01
Oil exponent. It is an empirically derived exponent used to calculate the variation of top oil the winding hottest-spot rise over ambient top-oil temperature with changes in load. To set n use the suggested values given in IEEE Std. C57.91-1995 (see the application chapter for suggested values), or ask the transformer manufacturer for advice.				
Cooling mode 2				
Winding exp m	0.8	0.01	2	0.01
Winding exponent. It is an empirically derived exponent used to calculate the variation of the winding hottest-spot rise over top-oil temperature with changes in load. To set n use the suggested values given in IEEE Std. C57.91-1995 (see the application chapter for suggested values), or ask the transformer manufacturer for advice.				
Oil exp n	0.8	0.01	2	0.01
Oil exponent. It is an empirically derived exponent used to calculate the variation of top oil rise over ambient temperature with changes in load. To set n use the suggested values given in IEEE Std. C57.91-1995 (see the application chapter for suggested values), or ask the transformer manufacturer for advice.				
Cooling mode 3				
Winding exp m	0.8	0.01	2	0.01
Winding exponent. It is an empirically derived exponent used to calculate the variation of the winding hottest-spot rise over top-oil temperature with changes in load. To set n use the suggested values given in IEEE Std. C57.91-1995 (see the application chapter for suggested values), or ask the transformer manufacturer for advice.				
Oil exp n	0.8	0.01	2	0.01
Oil exponent. It is an empirically derived exponent used to calculate the variation of top oil the winding hottest-spot rise over ambient top-oil temperature with changes in load. To set n use the suggested values given in IEEE Std. C57.91-1995 (see the application chapter for suggested values), or ask the transformer manufacturer for advice.				
Cooling mode 4				
Winding exp m	0.8	0.01	2	0.01
Winding exponent. It is an empirically derived exponent used to calculate the variation of the winding hottest-spot rise over top-oil temperature with changes in load. To set n use the suggested values given in IEEE Std. C57.91-1995 (see the application chapter for suggested values), or ask the transformer manufacturer for advice.				
Oil exp n	0.8	0.01	2	0.01
Oil exponent. It is an empirically derived exponent used to calculate the variation of the winding hottest-spot rise over top-oil temperature with changes in load. To set n use the suggested values given in IEEE Std. C57.91-1995 (see the application chapter for suggested values), or ask the transformer manufacturer for advice.				
Hot spot rise co	1 min	0.01 min	20 min	0.01 min
Winding time constant at hot spot locations. The transformer manufacturer should provide this parameter.				
Top oil rise co	120 min	1 min	1000 min	1 min
Oil time constant of the transformer for any load. The transformer manufacturer should provide this parameter.				
TOL Status	Enabled	Enabled or Disabled		
This setting enables or disables the three hot spot and the three top oil thermal stages.				
Hot Spot>1 Set	110°C	1°C	300°C	0.1°C
Hot spot first stage setting. The suggested temperature limits given by IEEE Std. C57.91-1995 may be used to set it. See the application chapter for suggested values.				
tHot Spot>1 Set	10 min	0 min	60000 min	0.1 min
Hot spot first stage time delay setting.				
Hot Spot>2 Set	130°C	1°C	300°C	0.1°C

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: THERMAL OVERLOAD				
Hot spot second stage setting. The suggested temperature limits given by IEEE Std. C57.91-1995 may be used to set it. See the application chapter for suggested values.				
tHot Spot>2 Set	10 min	0 min	60000 min	0.1 min
Hot spot second stage time delay setting.				
Hot Spot>3 Set	150°C	1°C	300°C	0.1°C
Hot spot third stage setting. The suggested temperature limits given by IEEE Std. C57.91-1995 may be used to set it. See the application chapter for suggested values.				
tHot Spot>3 Set	10 min	0 min	60000 min	0.1 min
Hot spot third stage time delay setting.				
Top Oil>1 Set	70°C	1°C	300°C	0.1°C
Top oil first stage setting. The suggested temperature limits given by IEEE Std. C57.91-1995 may be used to set it. See the application chapter for suggested values.				
tTop Oil>1 Set	10 min	0 min	60000 min	0.1 min
Top oil first stage time delay setting.				
Top Oil>2 Set	80°C	1°C	300°C	0.1°C
Top oil second stage setting. The suggested temperature limits given by IEEE Std. C57.91-1995 (may be used to set it. See the application chapter for suggested values.				
tTop Oil>2 Set	10 min	0 min	60000 min	0.1 min
Top oil second stage time delay setting.				
Top Oil>3 Set	90°C	1°C	300°C	0.1°C
Top oil third stage setting. The suggested temperature limits given by IEEE Std. C57.91-1995 may be used to set it. See the application chapter for suggested values.				
tTop Oil>3 Set	10 min	0 min	60000 min	0.1 min
Top oil third stage time delay setting.				
tPre-trip Set	5 min	0 min	60000 min	0.1 min
After the tpre-trip timer has expired, a pre-trip alarm is given. This alarm indicates that if the load remains unchanged a thermal trip will be asserted after the stage timer has expired.				
LOL Status	Enabled	Enabled or Disabled		
Enables or disables the loss of life function				
Life Hours at HS	180000 hr	1 hr	300000 hr	1 hr
Life hours at the reference hottest spot temperature. Advice from the transformer manufacturer may be required.				
Designed HS temp	110°C	1°C	200°C	0.1°C
The designed hottest spot temperature is 110°C for a transformer rated 65°C average winding rise, and 95°C for a transformer rated 55°C average winding rise.				
Constant B Set	15000	1	100000	1
Constant B is associated to the life expectancy curve. It is based on modern experimental data, and it may be set to 15000 as suggested by IEEE Std. C57.91-1995.				
FAA> Set	2	0.1	30	0.01
Aging acceleration factor setting. If the aging acceleration factor calculated by the relay is above this setting and tFAA has expired, an FAA alarm would be asserted. FAA calculation depends on constant B and the hottest temperature calculated by the thermal element.				
tFAA> Set	10 min	0 min	60000 min	1 min
Aging acceleration factor timer.				
LOL>1 Set	160000 hr	1 hr	300000 hr	1 hr

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: THERMAL OVERLOAD				
Transformer loss of life setting. If the life already lost by the transformer is above this threshold, a LOL alarm would be asserted after tLOL has expired. LOL calculation depends on the life hours at design hot spot temperature and the calculated residual life.				
tLOL> Set	10 min	0 min	60000 min	1 min
Loss of life timer.				
Reset Life Hours	0 hr	0 hr	300000 hr	1 hr
Resets the LOL status parameter to the set value when the loss of life reset command is executed. For new transformers Reset Life Hours is zero, so that when the commissioning of the thermal element is over, the loss of life statistics calculations are reset to zero. For old transformers this setting should indicate how much life the transformer has already lost.				

Table 7 - Group 1 thermal overload settings

4.6 Earth Fault Protection

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: EARTH FAULT				
Earth Fault 1	Enabled	Enabled/Disabled		
Enables or disables the earth fault 1 element.				
EF 1 Input	Derived	Measured, Derived		
Selects measured neutral current or derived neutral current				
EF 1 Derived	T1	T1, T2, T3, T4, T5, HV Winding, LV Winding, TV Winding		
Selects the signal used to calculate the zero sequence current.				
EF 1 Measured	TN1	TN1, TN2, TN3		
Selects the signal used to measure the zero sequence current.				
IN>1 Status	Enabled	Enabled/Disabled		
Enables or disables the first stage of earth fault 1				
IN>1 Char	IEC S Inverse	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, RI, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse, IDG		
Tripping characteristic for the first stage of earth fault 1				
IN>1 Direction	Non-Directional	Non-directional, Directional forward, Directional reverse.		
Direction setting for the first stage of earth fault 1				
IN>1 Current	0.2 In	0.08 In	4 In	0.01 In
Pick-up setting for the first stage of earth fault 1				
IN>1 IDG Is	1.5	1	4	0.1
Multiple of IN>1 setting for the IDG curve (Scandinavia), determines the actual relay current threshold at which the element starts.				
IN>1 Time Delay	1 s	0	200 s	0.01 s
Operating time delay setting for the first stage definite time element.				
IN>1 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
IN>1 Time Dial	1	0.01	100	0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: EARTH FAULT				
IN>1 K (RI)	1	0.1	10	0.05
Time multiplier to adjust the operating time for the RI curve.				
IN>1 IDG Time	1.2	1	2	0.01
Minimum operating time at high levels of fault current for the IDG curve.				
IN>1 Reset Char	DT	DT/Inverse		
Type of reset/release characteristic of the IEEE/US curves.				
IN>1 tRESET	0 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				
IN>2 Status	Enabled	Enabled/Disabled		
Enables or disables the second stage of earth fault 1				
IN>2 Char	Disabled	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, RI, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse, IDG		
Tripping characteristic for the second stage of earth fault 1				
IN>2 Direction	Non-Directional	Non-directional, Directional forward, Directional reverse.		
Direction setting for the second stage of earth fault 1				
IN>2 Current	0.2 In	0.08 In	4 In	0.01 In
Pick-up setting for the second stage of earth fault 1				
IN>2 IDG Is	1.5	1	4	0.1
Multiple of IN>2 setting for the IDG curve (Scandinavia), determines the actual relay current threshold at which the element starts.				
IN>2 Time Delay	1 s	0	200 s	0.01 s
Operating time delay setting for the second stage definite time element.				
IN>2 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
IN>2 Time Dial	1	0.01	100	0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
IN>2 K (RI)	1	0.1	10	0.05
Time multiplier to adjust the operating time for the RI curve.				
IN>2 IDG Time	1.2 s	1 s	2 s	0.01 s
Minimum operating time at high levels of fault current for the IDG curve.				
IN>2 Reset Char	DT	DT, Inverse		
Type of reset/release characteristic of the IEEE/US curves.				
IN>2 tRESET	0 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				
IN>3 Status	Disabled	Enabled or Disabled		
Setting to enable or disable the third stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden.				
IN>3 Direction	Non-Directional	Non-directional, Directional forward, Directional reverse.		
Direction setting for the third stage HV winding earth fault protection.				
IN>3 Current	2 In	0.08 In	32 In	0.01 In
Pick-up setting for the third stage of earth fault 1				
IN>3 Time Delay	0 s	0 s	200 s	0.01 s

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: EARTH FAULT				
Operating time delay setting for the third stage definite time element.				
IN>4 Status	Disabled	Enabled or Disabled		
Setting to enable or disable the fourth stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden.				
IN>4 Direction	Non-Directional	Non-directional, Directional forward, Directional reverse.		
Direction setting for the fourth stage of earth fault 1				
IN>4 Current	2 In	0.08 In	32 In	0.01 In
Pick-up setting for the fourth stage of earth fault 1				
IN>4 Time Delay	0 s	0 s	200 s	0.01 s
Operating time delay setting for the fourth stage definite time element.				
IN> Func Link	1111	Bit 0 = VTS Blocks IN>1 Bit 1 = VTS Blocks IN>2 Bit 2 = VTS Blocks IN>3 Bit 3 = VTS Blocks IN>4.		
Settings that determine whether VT supervision logic signals block selected earth fault stages. When set to 1, the VTS operation will block the stage if directionalized. When set to 0, the stage will revert to non-directional on the operation of the VTS.				
IN> DIRECTIONAL				
IN> Char Angle	-60 deg	-95 deg	95 deg	1 deg
Setting for the relay characteristic angle used for the directional decision. In the P642, only negative sequence polarization is possible because only up to 2 single phase VT inputs are available.				
IN> Pol	Zero Sequence	Zero Sequence or Neg Sequence		
Setting that determines whether the directional function uses zero sequence or negative sequence voltage polarizing. In the P642, only negative sequence polarization is possible because only up to 2 single phase VT inputs are available.				
IN> VNpol Set P643, P645 only	5 V	0.5 V	80 V	0.5 V
Setting for the minimum zero sequence voltage polarizing quantity for directional decision. In the P642, only negative sequence polarization is possible because only up to 2 single phase VT inputs are available.				
IN> V2pol Set	5 V	0.5 V	80 V	0.5 V
Setting for the minimum negative sequence voltage polarizing quantity for directional decision. In the P642, only negative sequence polarization is possible because only up to 2 single phase VT inputs are available.				
IN> I2pol Set	0.08 In	0.08 In	1 In	0.01 In
Setting for the minimum negative sequence current polarizing quantity for directional decision. In the P642, only negative sequence polarization is possible because only up to 2 single phase VT inputs are available.				
Earth Fault 2	Enabled	Enabled/Disabled		
Enables or disables the earth fault 2 element.				
EF 2 Input	Measured	Measured, Derived		
Selects measured neutral current or derived neutral current				
EF 2 Derived	T5	T1, T2, T3, T4, T5, HV Winding, LV Winding, TV Winding		
Selects the signal used to calculate the zero sequence current.				
EF 2 Measured	TN2	TN1, TN2, TN3		
Selects the signal used to measure the zero sequence current.				
IN>1 Status	Enabled	Enabled/Disabled		
Enables or disables the first stage of earth fault 2				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: EARTH FAULT				
IN>1 Function	IEC S Inverse	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, RI, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse, IDG		
Tripping characteristic for the first stage of earth fault 2				
IN>1 Direction	Non-Directional	Non-directional, Directional forward, Directional reverse.		
Direction setting for the first stage of earth fault 2				
IN>1 Current	0.2 In	0.08 In	4 In	0.01 In
Pick-up setting for the first stage of earth fault 2				
IN>1 IDG Is	1.5	1	4	0.1
Multiple of IN>1 setting for the IDG curve (Scandinavia), determines the actual relay current threshold at which the element starts.				
IN>1 Time Delay	1 s	0 s	200 s	0.01 s
Operating time delay setting for the first stage definite time element.				
IN>1 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
IN>1 Time Dial	1	0.01	100	0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
IN>1 K (RI)	1	0.1	10	0.05
Time multiplier setting to adjust the operating time for the RI curve.				
IN>1 IDG Time	1.2 s	1 s	2 s	0.01 s
Minimum operating time at high levels of fault current for the IDG curve.				
IN>1 Reset Char	DT	DT, Inverse		
Type of reset/release characteristic of the IEEE/US curves.				
IN>1 tRESET	0 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				
IN>2 Function	Disabled	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, RI, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse, IDG		
Tripping characteristic for the second stage earth fault protection.				
IN>2 Direction	Non-Directional	Non-directional, Directional forward, Directional reverse.		
Direction setting for the second stage of earth fault 2				
IN>2 Current	0.2 In	0.08 In	4 In	0.01 In
Pick-up setting for the second stage of earth fault 2				
IN>2 IDG Is	1.5	1	4	0.1
Multiple of IN>2 setting for the IDG curve (Scandinavia), determines the actual relay current threshold at which the element starts.				
IN>2 Time Delay	1 s	0 s	200 s	0.01 s
Operating time delay setting for the second stage definite time element.				
IN>2 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
IN>2 Time Dial	1	0.01	100	0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
IN>2 K (RI)	1	0.1	10	0.05

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: EARTH FAULT				
Time multiplier to adjust the operating time for the RI curve.				
IN>2 IDG Time	1.2 s	1 s	2 s	0.01 s
Minimum operating time at high levels of fault current for the IDG curve.				
IN>2 Reset Char	DT	DT, Inverse		
Type of reset/release characteristic of the IEEE/US curves.				
IN>2 tRESET	0 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				
IN>3 Status	Disabled	Enabled or Disabled		
Setting to enable or disable the third stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden.				
IN>3 Direction	Non-Directional	Non-directional, Directional forward, Directional reverse.		
Direction setting for the third stage of earth fault 2				
IN>3 Current	2 In	0.08 In	32 In	0.01 In
Pick-up setting for the third stage of earth fault 2				
IN>3 Time Delay	0 s	0 s	200 s	0.01 s
Operating time delay setting for the third stage definite time element.				
IN>4 Status	Disabled	Enabled or Disabled		
Setting to enable or disable the fourth stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden.				
IN>4 Direction	Non-Directional	Non-directional, Directional forward, Directional reverse.		
Direction setting for the fourth stage LV winding earth fault protection.				
IN>4 Current	2 In	0.08 In	32 In	0.01 In
Pick-up setting for the fourth stage of earth fault 2				
IN>4 Time Delay	0 s	0 s	200 s	0.01 s
Operating time delay setting for the fourth stage definite time element.				
IN> Func Link	1111	Bit 0 = VTS Blocks IN>1 Bit 1 = VTS Blocks IN>2 Bit 2 = VTS Blocks IN>3 Bit 3 = VTS Blocks IN>4.		
Settings that determine whether VT supervision logic signals block selected earth fault stages. When set to 1, the VTS operation will block the stage if directionalized. When set to 0, the stage will revert to non-directional on the operation of the VTS.				
IN> DIRECTIONAL				
IN> Char Angle	-60 deg	-95 deg	95 deg	1 deg
Setting for the relay characteristic angle used for the directional decision. In the P642, only negative sequence polarization is possible because only up to 2 single phase VT inputs are available.				
IN> Pol	Zero Sequence	Zero Sequence or Neg. Sequence		
Setting that determines whether the directional function uses zero sequence or negative sequence voltage polarizing. In the P642, only negative sequence polarization is possible because only up to 2 single phase VT inputs are available.				
IN> VNpol Set P643, P645 only	5 V	0.5 V	80 V	0.5 V
Setting for the minimum zero sequence voltage polarizing quantity for directional decision. In the P642, only negative sequence polarization is possible because only up to 2 single phase VT inputs are available.				
IN> V2pol etS	5	0.5 V	25 V	0.5 V
Setting for the minimum negative sequence voltage polarizing quantity for directional decision. In the P642, only negative sequence polarization is possible because only up to 2 single phase VT inputs are available.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: EARTH FAULT				
IN> I2pol Set	0.08 In	0.08 In	1 In	0.01 In
Setting for the minimum negative sequence current polarizing quantity for directional Decision. In the P642, only negative sequence polarization is possible because only up to 2 single phase VT inputs are available.				
Earth Fault 3	Enabled	Enabled/Disabled		
Enables or disables the earth fault 3 element.				
EF 3 Input	Measured	Measured, Derived		
Selects measured neutral current or derived neutral current				
EF 3 Derived	T3	T1, T2, T3, T4, T5, HV Winding, LV Winding, TV Winding		
Selects the signal used to calculate the zero sequence current.				
EF 3 Measured	TN3	TN1, TN2, TN3		
Selects the signal used to measure the zero sequence current.				
IN>1 Status	Enabled	Enabled/Disabled		
Enables or disables the first stage of earth fault 3				
IN>1 Function	IEC S Inverse	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, RI, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse, IDG		
Tripping characteristic for the first stage of earth fault 3.				
IN>1 Direction	Non-Directional	Non-directional, Directional forward, Directional reverse.		
Direction setting for the first stage of earth fault 3				
IN>1 Current	0.2 In	0.08 In	4 In	0.01 In
Pick-up setting for the first stage of earth fault 3				
IN>1 IDG Is	1.5	1	4	0.1
Multiple of IN>1 setting for the IDG curve (Scandinavia), determines the actual relay current threshold at which the element starts.				
IN>1 Time Delay	1 s	0 s	200 s	0.01 s
Operating time delay setting for the first stage definite time element.				
IN>1 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
IN>1 Time Dial	1	0.01	100	0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
IN>1 K (RI)	1	0.1	10	0.05
Time multiplier to adjust the operating time for the RI curve.				
IN>1 IDG Time	1.2	1	2	0.01
Minimum operating time at high levels of fault current for the IDG curve.				
IN>1 Reset Char	DT	DT, Inverse		
Type of reset/release characteristic of the IEEE/US curves.				
IN>1 tRESET	0 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				
IN>2 Function	Disabled	Disabled, DT, IEC S Inverse, IEC V Inverse, IEC E Inverse, UK LT Inverse, RI, IEEE M Inverse, IEEE V Inverse, IEEE E Inverse, US Inverse, US ST Inverse, IDG		
Tripping characteristic for the second stage of earth fault 3				
IN>2 Direction	Non-Directional	Non-directional, Directional forward, Directional reverse.		

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: EARTH FAULT				
Direction setting for the second stage of earth fault 3				
IN>2 Current	0.2 In	0.08 In	4 In	0.01 In
Pick-up setting for the second stage of earth fault 3				
IN>2 IDG Is	1.5	1	4	0.1
Multiple of IN>2 setting for the IDG curve (Scandinavia), determines the actual relay current threshold at which the element starts.				
IN>2 Time Delay	1 s	0 s	200 s	0.01 s
Operating time delay setting for the second stage definite time element.				
IN>2 TMS	1	0.025	1.2	0.025
Time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
IN>2 Time Dial	1	0.01	100	0.01
Time multiplier setting to adjust the operating time of the IEEE/US IDMT curves.				
IN>2 K (RI)	1	0.1	10	0.05
Time multiplier to adjust the operating time for the RI curve.				
IN>2 IDG Time	1.2 s	1 s	2 s	0.01 s
Minimum operating time at high levels of fault current for the IDG curve.				
IN>2 Reset Char	DT	DT, Inverse		
Type of reset/release characteristic of the IEEE/US curves.				
IN>2 tRESET	0 s	0 s	100 s	0.01 s
Reset/release time setting for definite time reset characteristic.				
IN>3 Status	Disabled	Enabled or Disabled		
Setting to enable or disable the third stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden.				
IN>3 Direction	Non-Directional	Non-directional, Directional forward, Directional reverse.		
Direction setting for the third stage of earth fault 3				
IN>3 Current	2 In	0.08 In	32 In	0.01 In
Pick-up setting for the third stage of earth fault 3				
IN>3 Time Delay	0 s	0 s	200 s	0.01 s
Operating time delay setting for the third stage definite time element.				
IN>4 Status	Disabled	Enabled or Disabled		
Setting to enable or disable the fourth stage definite time element. If the function is disabled, all associated settings with the exception of this setting, are hidden.				
IN>4 Direction	Non-Directional	Non-directional, Directional forward, Directional reverse.		
Direction setting for the fourth stage of earth fault 3				
IN>4 Current	2 In	0.08 In	32 In	0.01 In
Pick-up setting for the fourth stage of earth fault 3				
IN>4 Time Delay	0 s	0 s	200 s	0.01 s
Operating time delay setting for the fourth stage definite time element.				
IN> Func Link	1111	Bit 0 = VTS Blocks IN>1 Bit 1 = VTS Blocks IN>2 Bit 2 = VTS Blocks IN>3 Bit 3 = VTS Blocks IN>4.		
Settings that determine whether VT supervision logic signals block selected earth fault stages. When set to 1, the VTS operation will block the stage if directionalized. When set to 0, the stage will revert to non-directional on the operation of the VTS.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: EARTH FAULT				
IN> DIRECTIONAL				
IN> Char Angle	-60 deg	-95 deg	95 deg	1 deg
Setting for the relay characteristic angle used for the directional decision. In the P642, only negative sequence polarization is possible because only up to 2 single phase VT inputs are available.				
IN> Pol	Zero Sequence	Zero Sequence or Neg. Sequence		
Setting that determines whether the directional function uses zero sequence or negative sequence voltage polarizing. In the P642, only negative sequence polarization is possible because only up to 2 single phase VT inputs are available.				
IN> VNpol Set P643, P645 only	5 V1	0.5 V1	80 V1	0.5 V1
Setting for the minimum zero sequence voltage polarizing quantity for directional decision. In the P642, only negative sequence polarization is possible because only up to 2 single phase VT inputs are available.				
IN> V2pol Set	5 V1	0.5 V1	25 V1	0.5 V1
Setting for the minimum negative sequence voltage polarizing quantity for directional decision. In the P642, only negative sequence polarization is possible because only up to 2 single phase VT inputs are available.				
IN> I2pol Set	0.08 In	0.08 In	1 In	0.01 In
Setting for the minimum negative sequence current polarizing quantity for directional decision. In the P642, only negative sequence polarization is possible because only up to 2 single phase VT inputs are available.				

Table 8 - Group 1 earth fault settings

4.7 TF Monitoring Protection

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: TF MONITORING				
Through Fault	Enabled	Enabled or Disabled		
Enables or disables monitoring of through faults.				
Monitored Input	HV	HV, LV, TV		
Selects the input winding to be monitored.				
TF I> Trigger	3.85 pu	0.08 pu	20 pu	0.01 pu
A through fault event is recorded if any of the phase currents is larger than this setting.				
TF I2t> Alarm	100 pu	0 pu	1600 pu	0.01 pu
An alarm is asserted if the maximum cumulative I2t in the three phases exceeds this setting.				

Table 9 - Group 1 TF monitoring settings

4.8 Residual Overvoltage (Neutral Voltage Displacement)

The P64x relays have a two-stage neutral voltage displacement (NVD) element. Each stage has separate voltage and time delay settings. Stage 1 can be set to operate on either an IDMT or DT characteristic, while stage 2 can be set to DT only.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: RESIDUAL OVERVOLTAGE NVD				
VN>1 Function	DT	Disabled, DT, IDMT		
Setting for the tripping characteristic of the first stage residual overvoltage element.				
VN>1 Voltage Set	5 V1	1 V1	80 V1	1 V1
Pick-up setting for the first stage residual overvoltage characteristic.				
VN>1 Time Delay	5 s	0 s	100 s	0.01 s
Operating time delay setting for the first stage definite time residual overvoltage element.				
VN>1 TMS	1	0.5	100	0.5
Time multiplier setting to adjust the operating time of the IDMT characteristic. The characteristic is defined as follows: t = K / (M – 1) where: K = Time multiplier setting t = Operating time in seconds M = Derived residual voltage/relay setting voltage (VN> Voltage Set)				
VN>1 tReset	0 s	0 s	100 s	0.01 s
Setting to determine the reset or release definite time for the first stage characteristic				
VN>2 Status	Disabled	Enabled or Disabled		
Setting to enable or disable the second stage definite time residual overvoltage element.				
VN>2 Voltage Set	10 V1	1 V1	80 V1	1 V1
Pick-up setting for the second stage residual overvoltage element.				
VN>2 Time Delay	10 s	0 s	100 s	0.01 s
Operating time delay for the second stage residual overvoltage element.				

Table 10 - Group 1 residual overvoltage NVD settings

4.9 Overfluxing

The P64x relays have four-stage overfluxing elements. The P642 has one overfluxing element and the P643 and P645 may have up to two overfluxing elements. The element measures the ratio of voltage, (VAB), to frequency i.e. (V/Hz) and operates when this ratio exceeds the setting. The higher the voltage-to-frequency ratio, the greater the magnetizing current that would lead to heating and possible isolation failure. One stage can be set to operate with a definite time or inverse time delay (IDMT), this stage can be used to provide the protection trip output. When the flux level drops below pickup, the reset timer starts. The different stages can be combined to create a multi-stage V/Hz trip characteristic using PSL.

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: OVERFLUXING				
Volts/Hz Overfluxing element W1. P643 and P645 only if the optional three-phase VT is available.				
V/HZ Alm Status	Enable	Enabled or Disabled		
Enables or disables the V/Hz alarm element.				
V/HZ Alm Set	2.31 V/Hz	1.5 V/Hz	3.5 V/Hz	0.01 V/Hz
Pick-up setting for the V/Hz element.				
V/Hz Alarm Delay	10 s	0 s	6000 s	0.1 s
Operating time delay setting of the V/Hz alarm element.				

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: OVERFLUXING				
V/Hz>1 Status	Enable	Enabled or Disabled		
Enables or disables the V/Hz first stage trip element.				
V/Hz>1 Function	DT	DT or IDMT		
Tripping characteristic setting of the V/Hz first stage trip element.				
V/Hz>1 Trip Set	2.42 V/Hz	1.5 V/Hz	3.5 V/Hz	0.01 V/Hz
Pick-up setting for the V/Hz first stage trip element.				
V/Hz>1 Trip TMS	0.1	0.01	12	0.01
Setting for the time multiplier setting to adjust the operating time of the IDMT characteristic.				
V/Hz>1 Delay	60 s	0 s	6000 s	0.1 s
Operating time-delay setting of the V/Hz first stage trip element.				
V/Hz>1 tReset	0 s	0 s	6000 s	0.1 s
Setting to determine the reset or release definite time for the first stage overfluxing element W1				
V/Hz>2 Status	Enable	Enabled or Disabled		
Enables or disables the V/Hz second stage trip element.				
V/Hz>2 Trip Set	2.64 V/Hz	1.5 V/Hz	3.5 V/Hz	0.01 V/Hz
Pick-up setting for the V/Hz second stage trip element.				
V/Hz>2 Delay	3 s	0 s	6000 s	0.1 s
Operating time delay setting of the V/Hz alarm element.				
V/Hz>3 Status	Enable	Enabled or Disabled		
Enables or disables the V/Hz third stage trip element.				
V/Hz>3 Trip Set	2.86 V/Hz	1.5 V/Hz	3.5 V/Hz	0.01 V/Hz
Pick-up setting for the V/Hz third stage trip element.				
V/Hz>3 Delay	2.00 s	0 s	6000 s	0.1 s
Operating time delay setting of the V/Hz alarm element.				
V/Hz>4 Status	Enable	Enabled or Disabled		
Enables or disables the V/Hz fourth stage trip element.				
V/Hz>4 Trip Set	3.08 V/Hz	1.5 V/Hz	3.5 V/Hz	0.01 V/Hz
Pick-up setting for the V/Hz fourth stage trip element.				
V/Hz>4 Delay	1.00 s	0 s	6000 s	0.1 s
Operating time delay setting of the V/Hz alarm element.				
TPre-trip Alarm	200 s	1 s	6000 s	0.1 s
Pre-trip alarm time delay.				
Volts/Hz Overfluxing element W2. P642, P643 and P645				
V/HZ Alm Status	Enable	Enabled or Disabled		
Enables or disables the V/Hz alarm element.				
V/HZ Alm Set	2.31 V/Hz	1.5 V/Hz	3.5 V/Hz	0.01 V/Hz
Pick-up setting for the V/Hz element.				
V/Hz Alarm Delay	10 s	0 s	6000 s	0.1 s
Operating time delay setting of the V/Hz alarm element.				
V/Hz>1 Status	Enable	Enabled or Disabled		
Enables or disables the V/Hz first stage trip element.				
V/Hz>1 Function	DT	DT or IDMT		

Menu text	Default setting	Setting range		Step size
		Min	Max	
GROUP 1: OVERFLUXING				
Tripping characteristic setting of the V/Hz first stage trip element.				
V/Hz>1 Trip Set	2.42 V/Hz	1.5 V/Hz	3.5 V/Hz	0.01 V/Hz
Pick-up setting for the V/Hz first stage trip element.				
V/Hz>1 Trip TMS	0.1	0.01	12	0.01
Setting for the time multiplier setting to adjust the operating time of the IDMT characteristic.				
V/Hz>1 Delay	60 s	0 s	6000 s	0.1 s
Operating time delay setting of the V/Hz alarm element.				
V/Hz>1 tReset	0 s	0 s	6000 s	0.1 s
Setting to determine the reset or release definite time for the first stage overfluxing element W2				
V/Hz>2 Status	Enable	Enabled or Disabled		
Enables or disables the V/Hz second stage trip element.				
V/Hz>2 Trip Set	2.64 V/Hz	1.5 V/Hz	3.5 V/Hz	0.01 V/Hz
Pick-up setting for the V/Hz second stage trip element.				
V/Hz>2 Delay	3 s	0 s	6000 s	0.1 s
Operating time delay setting of the V/Hz alarm element.				
V/Hz>3 Status	Enable	Enabled or Disabled		
Enables or disables the V/Hz third stage trip element.				
V/Hz>3 Trip Set	2.86 V/Hz	1.5 V/Hz	3.5 V/Hz	0.01 V/Hz
Pick-up setting for the V/Hz third stage trip element.				
V/Hz>3 Delay	2.00 s	0 s	6000 s	0.1 s
Operating time delay setting of the V/Hz alarm element.				
V/Hz>4 Status	Enable	Enabled or Disabled		
Enables or disables the V/Hz fourth stage trip element.				
V/Hz>4 Trip Set	3.08 V/Hz	1.5 V/Hz	3.5 V/Hz	0.01 V/Hz
Pick-up setting for the V/Hz fourth stage trip element.				
V/Hz>4 Delay	1.0 s	0 s	6000 s	0.1 s
Operating time delay setting of the V/Hz alarm element.				
TPre-trip alarm	200 s	1 s	6000 s	0.1 s
Pre-trip alarm time delay.				

Table 11 - Group 1 overfluxing settings

4.10 Voltage Protection

One two-stage undervoltage and one two-stage overvoltage functions are available in the P643 and P645. These can be configured to measure either phase-to-phase or phase-to-neutral voltages. Stage 1 has inverse time-delayed characteristics and can be selected as IDMT, DT or Disabled. Stage 2 is DT only and is enabled or disabled in the **V<2 status** cell. The undervoltage stages can be blocked by a Poledead Inh setting.

One single stage negative phase sequence overvoltage function is available in the P642, P643 and P645.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: VOLTAGE PROTECTION. P643 and P645 only if the optional three-phase VT input is available.				
Undervoltage				
V< Measur't Mode	Phase-Neutral	Phase-phase or Phase-neutral		
Sets the measured input voltage used for the undervoltage elements.				
V< Operate Mode	Any Phase	Any phase or Three-phase		
Determines whether any phase or all three phases must satisfy the undervoltage criteria before a decision is made.				
V<1 Function	DT	IDMT, DT or Disabled		
Tripping characteristic for the first stage undervoltage function. The IDMT characteristic available on the first stage is defined by the following formula: t = K / (1 - M) Where: K = Time multiplier setting t = Operating time in seconds M = Measured voltage/relay setting voltage (V< Voltage Set)				
V<1 Voltage Set	50 V1	10 V1	120 V1	1 V1
Sets the pick-up setting for the first stage undervoltage element.				
V<1 Time Delay	10 s	0 s	100 s	0.01 s
Sets the operating time-delay for the first stage definite time undervoltage element.				
V<1 TMS	1	0.05	100	0.05
Sets the time multiplier setting to adjust the operating time of the IEC IDMT characteristic.				
V<1 Poledead Inh	Enabled	Enabled or Disabled		
If the setting is enabled, the relevant stage is inhibited by the pole dead logic. This logic produces an output when it detects either an open circuit breaker through auxiliary contacts feeding the relay opto inputs, or it detects a combination of both undercurrent and undervoltage on any one phase. It allows the undervoltage protection to reset when the circuit breaker opens to cater for line or bus side VT applications.				
V<2 Status	Disabled	Enabled or Disabled		
Enables or disables the second stage undervoltage element.				
V<2 Voltage Set	38 V1	10 V1	120 V1	1 V1
Sets the pick-up setting for the second stage undervoltage element.				
V<2 Time Delay	5 s	0 s	100 s	0.01 s
Sets the operating time-delay for the second stage definite time undervoltage element.				
V<2 Poledead Inh	Enabled	Disabled/Enabled		
Overvoltage				
V> Measur't Mode	Phase-Phase	Phase-phase or Phase-neutral		
Sets the measured input voltage used for the overvoltage elements.				
V> Operate Mode	Any Phase	Any phase or Three-phase		
Determines whether any phase or all three phases must satisfy the overvoltage criteria before a decision is made.				
V>1 Function	DT	IDMT, DT or Disabled		

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: VOLTAGE PROTECTION. P643 and P645 only if the optional three-phase VT input is available.				
Tripping characteristic for the first stage overvoltage element. The IDMT characteristic available on the first stage is defined by the following formula: t = K / (M - 1) Where: K = Time multiplier setting t = Operating time in seconds M = Measured voltage/relay setting voltage (V<> Voltage Set)				
V>1 Voltage Set	130 V1	60 V1	185 V1	1 V1
Sets the pick-up setting for the first stage overvoltage element.				
V>1 Time Delay	10 s	0 s	100 s	0.01 s
Sets the operating time-delay for the first stage definite time overvoltage element.				
V>1 TMS	1	0.05	100	0.05
Sets the time multiplier to adjust the operating time of the IEC IDMT characteristic.				
V>2 Status	Disabled	Enabled or Disabled		
Enables or disables the second stage overvoltage element.				
V>2 Voltage Set	150 V1	60 V1	185 V1	1 V1
Sets the pick-up setting for the second stage overvoltage element.				
V>2 Time Delay	0.5 s	0 s	100 s	0.01 s
Sets the operating time-delay for the second stage definite time overvoltage element.				
Negative phase sequence overvoltage				
V2>1 Status	Disabled	Enabled or Disabled		
Enables or disables the negative phase sequence overvoltage element				
V2>1 Voltage Set	15 V	1 V	110 V	1 V
Sets the pick-up setting for the negative phase sequence overvoltage element				
V2>1 Time Delay	5 s	0 s	100 s	0.01 s
Sets the operating time-delay for the negative phase sequence overvoltage element				

Table 12 - Group 1 voltage protection settings

4.11 Frequency Protection

The relay includes 4 stages of underfrequency and 2 stages of overfrequency protection to help load shedding and subsequent restoration. The frequency can be obtained from any analog signal having the voltage priority over the current.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: FREQ PROTECTION				
UNDER FREQUENCY				
F<1 Status	Enabled	Enabled or Disabled		
Enables or disables the first stage underfrequency element.				
F<1 Setting	49.5 Hz	46 Hz	65 Hz	0.01 Hz
Determines the pick-up threshold for the first stage underfrequency element.				
F<1 Time Delay	4 s	0 s	100 s	0.01 s

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: FREQ PROTECTION				
Determines the minimum operating time-delay for the first stage underfrequency element.				
F<2 Status	Disabled	Enabled or Disabled		
Enables or disables the second stage underfrequency element.				
F<2 Setting	49 Hz	46 Hz	65 Hz	0.01 Hz
Determines the pick-up threshold for the second stage underfrequency element.				
F<2 Time Delay	3 s	0 s	100 s	0.01 s
Determines the minimum operating time-delay for the second stage underfrequency element.				
F<3 Status	Disabled	Enabled or Disabled		
Enables or disables the third stage underfrequency element.				
F<3 Setting	48.5 Hz	46 Hz	65 Hz	0.01 Hz
Determines the pick-up threshold for the third stage underfrequency element.				
F<3 Time Delay	2 s	0 s	100 s	0.01 s
Determines the minimum operating time-delay for the third stage underfrequency element.				
F<4 Status	Disabled	Enabled or Disabled		
Determines the pick-up threshold for the fourth stage underfrequency element.				
F<4 Setting	48 Hz	46 Hz	65 Hz	0.01 Hz
Enables or disables the fourth stage underfrequency element.				
F<4 Time Delay	1 s	0 s	100 s	0.01 s
Determines the minimum operating time-delay for the fourth stage underfrequency element.				
OVER FREQUENCY				
F>1 Status	Enabled	Enabled or Disabled		
Enables or disables the first stage overfrequency element.				
F>1 Setting	50.5 Hz	46 Hz	65 Hz	0.01 Hz
Determines the pick-up threshold for the first stage overfrequency element.				
F>1 Time Delay	2 s	0 s	100 s	0.01 s
Determines the minimum operating time-delay for the first stage overfrequency element.				
F>2 Status	Disabled	Enabled or Disabled		
Enables or disables the second stage overfrequency element.				
F>2 Setting	51 Hz	46 Hz	65 Hz	0.01 Hz
Determines the pick-up threshold for the second stage overfrequency element.				
F>2 Time Delay	1 s	0 s	100 s	0.01 s
Determines the minimum operating time-delay for the second stage overfrequency element.				

Table 13 - Group 1 FREQ protection settings

4.12 Resistor Temperature Device (RTD) Protection

The P642/P643/P645 relays provide temperature protection from 10 PT100 Resistor Temperature Devices (RTD). Each RTD has a definite time trip and alarm stage.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: RTD PROTECTION				
Select RTD	0000000000	Bit 0 - Select RTD 1 Bit 1 - Select RTD 2 Bit 2 - Select RTD 3 Bit 3 - Select RTD 4 Bit 4 - Select RTD 5 Bit 5 - Select RTD 6 Bit 6 - Select RTD 7 Bit 7 - Select RTD 8 Bit 8 - Select RTD 9 Bit 9 - Select RTD 10		N/A
10-bit setting to enable or disable the 10 RTDs. For each bit 1 = Enabled, 0 = Disabled.				
RTD 1 Alarm Set	80°C	0°C	200°C	1°C
Temperature setting for the RTD 1 alarm element.				
RTD 1 Alarm Dly	10 s	0 s	100 s	1 s
Operating time delay setting for the RTD 1 alarm element.				
RTD 1 Trip Set	85°C	0°C	200°C	1°C
Temperature setting for the RTD 1 trip element.				
RTD 1 Trip Dly	1 s	0 s	100 s	1 s
Operating time delay setting for the RTD 1 alarm element.				
RTD 2-10 Alarm and Trip Settings are the same as RTD1.				

Table 14 - Group 1 RTD protection settings

4.13 Circuit Breaker Failure

Current-based protection: the reset condition depends on undercurrent to determine whether the CB has opened.

Non current-based protection: the reset criteria can be selected from a setting to determine a CB Failure.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: CB FAIL				
T1 CBF Status	Enabled	Enabled or disabled		
Enables or disables circuit breaker failure 1. It is associated to T1 CT current input.				
I< Current Set	10%	5%	400%	1%
Sets the pick-up for the phase undercurrent element of circuit breaker failure 1				
In< Status	Disabled	Enabled or disabled		
Enables or disables the ground undercurrent element of circuit breaker failure 1.				
In< Inputs	Measured	Measured or derived		
Sets the ground undercurrent element as measured or derived				
In< Terminal	TN1	TN1, TN2, TN3		
Sets the single phase CT related to circuit breaker failure 1				
In< Current Set	10%	5%	400%	1%
Sets the pick-up for the ground undercurrent element of circuit breaker failure 1.				
CB Fail 1 Status	Disabled	Enabled or disabled		

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: CB FAIL				
Enables or disables the re-trip stage of circuit breaker failure 1.				
CB1 Fail Timer	0.05 s	0 s	10 s	0.001 s
Sets circuit breaker failure 1 re-trip timer				
CB Fail 2 Status	Enabled	Enabled or disabled		
Enables or disables the back-trip stage of the circuit breaker failure 1.				
CB2 Fail Timer	0.2 s	0 s	10 s	0.001 s
Sets circuit breaker failure 1 back-up timer				
CBF Non I Reset	CB Open & I<	I< Only, CB Open & I<, Prot Reset & I<		
Setting which determines the elements that reset circuit breaker failure 1 for non current-based protection functions (such as voltage and frequency) initiating circuit breaker fail conditions.				
CBF Ext Reset	CB Open & I<	I< Only, CB Open & I<, Prot Reset & I<		
Setting which determines the elements that reset the circuit breaker failure 1 for external protection functions initiating circuit breaker failure conditions.				
T2 CBF Status	Disabled	Enabled or disabled		
Enables or disables circuit breaker failure 2. It is associated to T2 CT current input.				
I< Current Set	10%	5%	400%	1%
Sets the pick-up for the phase undercurrent element of circuit breaker failure 2				
In< Status	Disabled	Enabled or disabled		
Enables or disables the ground undercurrent element of circuit breaker failure 2.				
In< Inputs	Measured	Measured or derived		
Sets the ground undercurrent element as measured or derived				
In< Terminal	TN1	TN1, TN2, TN3		
Sets the single phase CT related to circuit breaker failure 2				
In< Current Set	10%	5%	400%	1%
Sets the pick-up for the ground undercurrent element of circuit breaker failure 2.				
CB Fail 1 Status	Disabled	Enabled or disabled		
Enables or disables the re-trip stage of circuit breaker failure 2.				
CB1 Fail Timer	0.05 s	0 s	10 s	0.001 s
Sets circuit breaker failure 2 re-trip timer				
CB Fail 2 Status	Enabled	Enabled or disabled		
Enables or disables the back-trip stage of the circuit breaker failure 2.				
CB2 Fail Timer	0.2 s	0 s	10 s	0.001 s
Sets circuit breaker failure 2 back-up timer				
CBF Non I Reset	CB Open & I<	I< Only, CB Open & I<, Prot Reset & I<		
Setting which determines the elements that reset circuit breaker failure 2 for non current-based protection functions (such as voltage and frequency) initiating circuit breaker fail conditions.				
CBF Ext Reset	CB Open & I<	I< Only, CB Open & I<, Prot Reset & I<		
Setting which determines the elements that reset the circuit breaker failure 2 for external protection functions initiating circuit breaker failure conditions.				
T3 CBF Status Only P643 and P645	Enabled	Enabled or disabled		
Enables or disables circuit breaker failure 3. It is associated to T3 CT current input.				
I< Current Set	10%	5%	400%	1%

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: CB FAIL				
Sets the pick-up for the phase undercurrent element of circuit breaker failure 3				
In< Status	Disabled	Enabled or disabled		
Enables or disables the ground undercurrent element of circuit breaker failure 3.				
In< Inputs	Measured	Measured or derived		
Sets the ground undercurrent element as measured or derived				
In< Terminal	TN3	TN1, TN2, TN3		
Sets the single phase CT related to circuit breaker failure 3				
In< Current Set	10%	5%	400%	1%
Sets the pick-up for the ground undercurrent element of circuit breaker failure 3.				
CB Fail 1 Status	Disabled	Enabled or disabled		
Enables or disables the re-trip stage of circuit breaker failure 3.				
CB1 Fail Timer	0.05 s	0 s	10 s	0.001 s
Sets circuit breaker failure 3 re-trip timer				
CB Fail 2 Status	Enabled	Enabled or disabled		
Enables or disables the back-trip stage of the circuit breaker failure 3.				
CB2 Fail Timer	0.2 s	0 s	10 s	0.001 s
Sets circuit breaker failure 3 back-up timer				
CBF Non I Reset	CB Open & I<	I< Only, CB Open & I<, Prot Reset & I<		
Setting which determines the elements that reset circuit breaker failure 3 for non current-based protection functions (such as voltage and frequency) initiating circuit breaker fail conditions.				
CBF Ext Reset	CB Open & I<	I< Only, CB Open & I<, Prot Reset & I<		
Setting which determines the elements that reset the circuit breaker failure 3 for external protection functions initiating circuit breaker failure conditions.				
T4 CBF Status Only P643 and P645	Enabled	Enabled or disabled		
Enables or disables circuit breaker failure 4. It is associated to T4 CT current input.				
I< Current Set	10%	5%	400%	1%
Sets the pick-up for the phase undercurrent element of circuit breaker failure 4				
In< Status	Disabled	Enabled or disabled		
Enables or disables the ground undercurrent element of circuit breaker failure 4.				
In< Inputs	Measured	Measured or derived		
Sets the ground undercurrent element as measured or derived				
In< Terminal	TN2	TN1, TN2, TN3		
Sets the single phase CT related to circuit breaker failure 4				
In< Current Set	10%	5%	400%	1%
Sets the pick-up for the ground undercurrent element of circuit breaker failure 4.				
CB Fail 1 Status	Disabled	Enabled or disabled		
Enables or disables the re-trip stage of circuit breaker failure 4.				
CB1 Fail Timer	0.05 s	0 s	10 s	0.001 s
Sets circuit breaker failure 4 re-trip timer				
CB Fail 2 Status	Enabled	Enabled or disabled		
Enables or disables the back-trip stage of the circuit breaker failure 4.				

<table>
<tr><th rowspan="2">Menu text</th><th rowspan="2">Default setting</th><th colspan="2">Setting range</th><th rowspan="2">Step size</th></tr>
<tr><th>Min.</th><th>Max.</th></tr>
<tr><td colspan="5">GROUP 1: CB FAIL</td></tr>
<tr><td>CB2 Fail Timer</td><td>0.2 s</td><td>0 s</td><td>10 s</td><td>0.001 s</td></tr>
<tr><td colspan="5">Sets circuit breaker failure 4 back-up timer</td></tr>
<tr><td>CBF Non I Reset</td><td>CB Open & I<</td><td colspan="3">I< Only, CB Open & I<, Prot Reset & I<</td></tr>
<tr><td colspan="5">Setting which determines the elements that reset circuit breaker failure 4 for non current-based protection functions (such as voltage and frequency) initiating circuit breaker fail conditions.</td></tr>
<tr><td>CBF Ext Reset</td><td>CB Open & I<</td><td colspan="3">I< Only, CB Open & I<, Prot Reset & I<</td></tr>
<tr><td colspan="5">Setting which determines the elements that reset the circuit breaker failure 4 for external protection functions initiating circuit breaker failure conditions.</td></tr>
<tr><td>T5 CBF Status
Only P643 and P645</td><td>Disabled</td><td colspan="3">Enabled or disabled</td></tr>
<tr><td colspan="5">Enables or disables circuit breaker failure 5. It is associated to T5 CT current input.</td></tr>
<tr><td>I< Current Set</td><td>10%</td><td>5%</td><td>400%</td><td>1%</td></tr>
<tr><td colspan="5">Sets the pick-up for the phase undercurrent element of circuit breaker failure 5</td></tr>
<tr><td>In< Status</td><td>Disabled</td><td colspan="3">Enabled or disabled</td></tr>
<tr><td colspan="5">Enables or disables the ground undercurrent element of circuit breaker failure 5.</td></tr>
<tr><td>In< Inputs</td><td>Measured</td><td colspan="3">Measured or derived</td></tr>
<tr><td colspan="5">Sets the ground undercurrent element as measured or derived</td></tr>
<tr><td>In< Terminal</td><td>TN2</td><td colspan="3">TN1, TN2, TN3</td></tr>
<tr><td colspan="5">Sets the single phase CT related to circuit breaker failure 5</td></tr>
<tr><td>In< Current Set</td><td>10%</td><td>5%</td><td>400%</td><td>1%</td></tr>
<tr><td colspan="5">Sets the pick-up for the ground undercurrent element of circuit breaker failure 5.</td></tr>
<tr><td>CB Fail 1 Status</td><td>Disabled</td><td colspan="3">Enabled or disabled</td></tr>
<tr><td colspan="5">Enables or disables the re-trip stage of circuit breaker failure 5.</td></tr>
<tr><td>CB1 Fail Timer</td><td>0.05 s</td><td>0 s</td><td>10 s</td><td>0.001 s</td></tr>
<tr><td colspan="5">Sets circuit breaker failure 5 re-trip timer</td></tr>
<tr><td>CB Fail 2 Status</td><td>Enabled</td><td colspan="3">Enabled or disabled</td></tr>
<tr><td colspan="5">Enables or disables the back-trip stage of the circuit breaker failure 5.</td></tr>
<tr><td>CB2 Fail Timer</td><td>0.2 s</td><td>0 s</td><td>10 s</td><td>0.001 s</td></tr>
<tr><td colspan="5">Sets circuit breaker failure 5 back-up timer</td></tr>
<tr><td>CBF Non I Reset</td><td>CB Open & I<</td><td colspan="3">I< Only, CB Open & I<, Prot Reset & I<</td></tr>
<tr><td colspan="5">Setting which determines the elements that reset circuit breaker failure 5 for non current-based protection functions (such as voltage and frequency) initiating circuit breaker fail conditions.</td></tr>
<tr><td>CBF Ext Reset</td><td>CB Open & I<</td><td colspan="3">I< Only, CB Open & I<, Prot Reset & I<</td></tr>
<tr><td colspan="5">Setting which determines the elements that reset the circuit breaker failure 5 for external protection functions initiating circuit breaker failure conditions.</td></tr>
</table>

Table 15 - Group 1 CB fail settings

4.14 VT and CT Supervision

The VTS feature in the relay operates when it detects a negative phase sequence (NPS) voltage when there is no negative phase sequence current. This gives operation, for the loss of one or two-phase voltages. Stability of the VTS function is assured during system fault conditions by the presence of the NPS current. The use of negative sequence quantities ensures correct operation even where three-limb or V-connected VTs are used.

If all three-phase voltages to the relay are lost, there are no negative phase sequence quantities to operate the VTS function, and the three-phase voltages collapse. If this is detected without a corresponding change in any of the phase current signals (which would indicate a fault), a VTS condition is raised. In practice, the relay detects superimposed current signals, which are changes in the current applied to the relay.

If a VT is inadvertently left isolated before line energization, voltage-dependent elements may operate incorrectly. The previous VTS element detected 3-phase VT failure due to the absence of all three phase voltages with no corresponding change in current. However, on line energization there is a change in current, for example, due to load or line charging current. An alternative method of detecting 3-phase VT failure is therefore required on line energization.

The absence of measured voltage on all three phases on line energization can be as a result of two conditions. The first is a 3-phase VT failure and the second is a close-up 3-phase fault. The first condition would require blocking of the voltage dependent function and the second would require tripping. To differentiate between these two conditions an overcurrent level detector (VTS I> Inhibit) is used to prevent a VTS block from being issued if it operates. This element should be set in excess of any non-fault based currents on line energization (load, line charging current, transformer inrush current if applicable) but below the level of current produced by a close-up 3-phase fault. If the line is closed where a 3-phase VT failure is present, the overcurrent detector does not operate and a VTS block is applied. Closing onto a 3-phase fault results in operation of the overcurrent detector and prevents a VTS block from being applied.

This logic is only enabled during a live line condition to prevent operation under dead system conditions. A live line condition is indicated by the relay's pole dead logic. Dead system conditions are where no voltage is present and the VTS I> Inhibit overcurrent element is not picked up.

Differential CTS is based on measurement of the ratio of I2 and I1 at all ends. When this ratio is not zero, either the system has an unbalanced fault or there is a 1 or 2 phase CT problem. In both cases, both I2 and I1 are non-zero.

If the ratio of I2 and I1 is detected at all ends, it is almost certainly a genuine fault condition and CTS is prevented from operating. If this ratio is detected at only one end, it could be either a CT problem or a single end-fed fault condition. I1 is therefore detected to determine whether it is a CT problem or not.

If I1 is detected at all ends, it must be CT problem and CTS is allowed to operate. If I1 is detected at only one end, it is either an inrush condition or a single end-fed internal fault, therefore the CTS operation is blocked.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1: SUPERVISION				
VT supervision. P642 when the two phase VT inputs are available. P643 and P645 when the optional three-phase VT input is available.				
VTS Status	Blocking	Blocking, Indication, Disabled		
This setting determines whether the following operations occur on detection of VTS. VTS logic disabled, when set to disabled. VTS set to provide alarm indication only, when set to indication. Optional blocking of voltage-dependent protection elements, when set to blocking. Optional conversion of directional overcurrent elements to non-directional protection (available when set to blocking mode only). These settings are in the function links cell of the relevant protection element columns in the menu.				
VTS Reset Mode	Manual	Manual, Auto		

Menu text	Default setting	Setting range		Step size
		Min.	**Max.**	
GROUP 1: SUPERVISION				
The VTS block is latched after the user-settable VTS Time Delay. Once the signal has latched, two methods of resetting are available. The first is manually using the front panel interface (or remote communications). The second is in **Auto** mode, provided the VTS condition has been removed and the 3-phase voltages have been restored above the phase level detector settings for more than 240 ms.				
VTS Time Delay	5 s	1 s	10 s	0.1 s
Operating time delay setting of the VTS element on detection of a voltage supervision condition.				
VTS I> Inhibit	10 pu	0.08 pu	32 pu	0.01 pu
This overcurrent setting inhibits the voltage transformer supervision if all three phase voltages are lost, caused by a close-up 3-phase fault on the system after the CB is closed to energize the line. In a P642, this setting is referred to CT1 if the VT is located on the HV winding and to CT2 if the Ct is located on the LV winding. In a P643, this setting is always referred to CT1, CT2 or CT3 if the VT is located in the HV, TV or LV windings respectively. In a P645, this setting is always referred to CT1, CT3 or CT5 if the VT is located in the HV, TV or LV windings respectively.				
VTS I2> Inhibit	0.05 pu	0.05 pu	0.5 pu	0.01 pu
This NPS overcurrent setting inhibits the voltage transformer supervision if a fault occurs on the system with negative sequence current above this setting. In a P642, this setting is referred to CT1 if the VT is located on the HV winding and to CT2 if the Ct is located on the LV winding. In a P643, this setting is always referred to CT1, CT2 or CT3 if the VT is located in the HV, TV or LV windings respectively. In a P645, this setting is always referred to CT1, CT3 or CT5 if the VT is located in the HV, TV or LV windings respectively.				
CT supervision. P642, 3, 5.				
Diff CTS	Enable	Enable, Disable		
Enables or disables the CTS function.				
CTS Status	Restrain	Indication, Restrain		
In Indication mode, a CTS alarm is issued after CTS time delay timer expires. In restraint mode, the differential protection is desensitised to the Is-CTS setting.				
CTS Time delay	2 s	0 s	10 s	0.1 s
Sets the pick-up time delay for the CT Fail Alarm assertion.				
CTS I1	10%	5%	100%	1%
Load current threshold setting				
CTS I2/I1>1	5%	5%	100%	1%
Low set ratio of negative to positive sequence current.				
CTS I2/I1>2	40%	5%	100%	1%
High set ratio of negative to positive sequence current.				

Table 16 - Group 1 supervision settings

4.15 Input Labels

Menu text	Default setting	Setting range	Step size
GROUP 1: INPUT LABELS			
Opto Input 1 to 12	Input L1	16 character text	
P642, P643 and P645. Text label to describe each individual opto input. This text is displayed in the programmable scheme logic and event record description of the opto input.			
Opto Input 13 to 24	Input L13 to L24	16 Character Text	
P643 and P645. Text label to describe each individual opto input. This text is displayed in the programmable scheme logic and event record description of the opto input.			

Table 17 - Input label settings

4.16 Output Labels

Menu text	Default setting	Setting range	Step size
GROUP 1: OUTPUT LABELS			
Relay 1	Output R1	16 Character Text	
P642, 643 and 645. Text label to describe each individual relay output contact. This text is displayed in the programmable scheme logic and event record description of the relay output contact.			
Relay 13 to 24	Output R13 to R24	16 Character Text	
P643 and P645. Text label to describe each individual relay output contact. This text is displayed in the programmable scheme logic and event record description of the relay output contact.			

Table 18 - Output label settings

4.17 RTD Labels

Menu text	Default setting	Setting range	Step size
GROUP 1: RTD LABELS			
RTD 1 to 10	RTD 1 to 10	16 Character Text	
Text label to describe each individual RTD. This text is displayed in the Measurements 3 menu and fault records for the description of the RTDs.			

Table 19 - RTD label settings

4.18 Current Loop Inputs and Outputs (CLIO) Protection

Four analog or current loop inputs are provided for transducers with ranges of 0 to 1 mA, 0 to 10 mA, 0 to 20 mA or 4 to 20 mA. The analog inputs can be used for various transducers such as vibration monitors, tachometers, pressure and temperature transducers. Associated with each input there are two protection stages, one for alarm and one for trip. Each stage can be individually enabled or disabled, and each stage has a Definite Time delay setting. The Alarm and Trip stages can be set for operation when the input value falls below the Alarm/Trip threshold **Under** or when the input current is above the input value **Over**. The 4 to 20 mA input has an undercurrent alarm element which can be used to indicate a fault with the transducer or wiring.

There are four analog current outputs with ranges of 0 to 1 mA, 0 to 10 mA, 0 to 20 mA or 4 to 20 mA, which can reduce the need for separate transducers. These outputs can be fed to standard moving coil ammeters for analog measurements or to a SCADA system using an existing analog RTU.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1:CLIO PROTECTION				
CLIO Input 1	Enabled	Enabled or Disabled		
Enables or disables the current loop (transducer) input 1 element.				
CLI1 Input Type	4 to 20 mA	0 to 1 mA, 0 to 10 mA, 0 to 20 mA, 4 to 20 mA		
Current loop 1 input type.				
CLI1 Input Label	CLIO Input 1	16 characters		

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1:CLIO PROTECTION				
Current loop 1 input description. The minimum and maximum settings define the range but they have no units. The user can use the label to enter the transducer function and unit of measurement.				
CLI1 Minimum	0	-9999	9999	0.1
Current loop input 1 minimum setting. Defines the lower range of the physical or electrical quantity measured by the transducer.				
CLI1 Maximum	100	-9999	9999	0.1
Current loop input 1 maximum setting. Defines the upper range of the physical or electrical quantity measured by the transducer.				
CLI1 Alarm	Disabled	Enabled or Disabled		
Enables or disables the current loop input 1 alarm element.				
CLI1 Alarm Fn	Over	Over or Under		
Operating mode of the current loop input 1 alarm element.				
CLI1 Alarm Set	50	0	100	0.1
Pick-up setting for the current loop input 1 alarm element.				
CLI1 Alarm Delay	1 s	0 s	100 s	0.1 s
Operating time-delay setting of current loop input 1 alarm element.				
CLI1 Trip	Disabled	Enabled or Disabled		
Pick-up setting for the current loop input 1 trip element.				
CLI1 Trip Fn	Over	Over or Under		
Operating mode of the current loop input 1 alarm element.				
CLI1 Trip Set	60	0	100	0.1
Pick-up setting for the current loop input 1 trip element.				
CLI1 Trip Delay	0 s	0 s	100 s	0.1 s
Operating mode of the current loop input 1 trip element.				
CLI1 I< Alarm	Disabled	Enabled or Disabled		
Enables or disables the current loop input 1 undercurrent element used to supervise the 4-20 mA input only.				
CLI1 I< Alm Set	3.5 mA	0 mA	4 mA	0.1 mA
Pick-up setting for the current loop input 1 undercurrent element. (4 - 20 mA input only).				
CLI2/3/4 settings are the same as CLI1				
CLIO Output 1	Disabled	Enabled or Disabled		
Enable or disables the current loop (transducer) output 1 element.				
CLO1 Output Type	4 to 20 mA	0 to 1 mA, 0 to 10 mA, 0 to 20 mA, 4 to 20 mA		
Current loop 1 output type				
CLO1 Set Values	Primary	Primary or Secondary		
This setting controls if the measured values from current loop output 1 are Primary or Secondary values.				
CLO1 Parameter	IA-1 Magnitude	A list of parameters are shown in the following table		
This setting defines the measured quantity assigned to current loop output 1.				
CLO1 Minimum	See following table	Range, step size and unit corresponds to the selected parameter in the following table		
Current loop output 1 minimum setting. Defines the lower range of the measurement.				
CLO1 Maximum	See following table	Range, step size and unit corresponds to the selected parameter in the following table		

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
GROUP 1:CLIO PROTECTION				
Current loop output 1 maximum setting. Defines the upper range of the measurement.				
CLO2/3/4 settings are the same as CLO1				

Table 20 - Group 1 CLIO Protection Settings

The CLIO output measurements are updated using a software timer every 50 ms. The CLIO protection is called every cycle (20 ms).

Current loop output parameters are shown in the following table:

Current loop output measurement	Unit	Min.	Max.	Step	Default min.	Default max.
IA-1 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IB-1 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IC-1 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IA-2 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IB-2 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IC-2 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IA-3 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IB-3 Magnitude	A	0	16 In	0.01 In	0	1.2 In
IC-3 Magnitude	A	0	16In	0.01 In	0	1.2 In
IA-4 Magnitude	A	0	16In	0.01 In	0	1.2 In
IB-4 Magnitude	A	0	16In	0.01 In	0	1.2 In
IC-4 Magnitude	A	0	16In	0.01 In	0	1.2 In
IA-5 Magnitude	A	0	16In	0.01 In	0	1.2 In
IB-5 Magnitude	A	0	16In	0.01 In	0	1.2 In
IC-5 Magnitude	A	0	16In	0.01 In	0	1.2 In
I1-1 Magnitude	A	0	16In	0.01 In	0	1.2 In
I2-1 Magnitude	A	0	16In	0.01 In	0	1.2 In
I0-1 Magnitude	A	0	16In	0.01 In	0	1.2 In
I1-2 Magnitude	A	0	16 In	0.01 In	0	1.2 In
I2-2 Magnitude	A	0	16 In	0.01 In	0	1.2 In
I0-2 Magnitude	A	0	16In	0.01 In	0	1.2 In
I1-3 Magnitude	A	0	16In	0.01 In	0	1.2 In
I2-3 Magnitude	A	0	16In	0.01 In	0	1.2 In
I0-3 Magnitude	A	0	16In	0.01 In	0	1.2 In
I1-4 Magnitude	A	0	16In	0.01 In	0	1.2 In
I2-4 Magnitude	A	0	16In	0.01 In	0	1.2 In
I0-4 Magnitude	A	0	16In	0.01 In	0	1.2 In
I1-5 Magnitude	A	0	16In	0.01 In	0	1.2 In
I2-5 Magnitude	A	0	16In	0.01 In	0	1.2 In
I0-5 Magnitude	A	0	16In	0.01 In	0	1.2 In
IA HV Magnitude	A	0	16In	0.01 In	0	1.2 In
IB HV Magnitude	A	0	16In	0.01 In	0	1.2 In

Current loop output measurement	Unit	Min.	Max.	Step	Default min.	Default max.
IC HV Magnitude	A	0	16In	0.01 In	0	1.2 In
IN HV Measured Mag	A	0	16In	0.01 In	0	1.2 In
IN HV Derived Mag	A	0	16In	0.01 In	0	1.2 In
IA LV Magnitude	A	0	16In	0.01 In	0	1.2 In
IB LV Magnitude	A	0	16In	0.01 In	0	1.2 In
IC LV Magnitude	A	0	16In	0.01 In	0	1.2 In
IN LV Measured Mag	A	0	16In	0.01 In	0	1.2 In
IN LV Derived Mag	A	0	16In	0.01 In	0	1.2 In
IA TV Magnitude	A	0	16In	0.01 In	0	1.2 In
IB TV Magnitude	A	0	16In	0.01 In	0	1.2 In
IC TV Magnitude	A	0	16In	0.01 In	0	1.2 In
IN TV Measured Mag	A	0	16In	0.01 In	0	1.2 In
IN TV Derived Mag	A	0	16In	0.01 In	0	1.2 In
VAB Magnitude	V	0	200 Vn	0.1 Vn	0	140 Vn
VBC Magnitude	V	0	200 Vn	0.1 Vn	0	140 Vn
VCA Magnitude	V	0	200 Vn	0.1 Vn	0	140 Vn
VAN Magnitude	V	0	200 Vn	0.1 Vn	0	80 Vn
VBN Magnitude	V	0	200 Vn	0.1 Vn	0	80 Vn
VCN Magnitude	V	0	200 Vn	0.1 Vn	0	80 Vn
Vx Magnitude	V	0	200 Vn	0.1 Vn	0	80 Vn
VN Derived Mag	V	0	200 Vn	0.1 Vn	0	80 Vn
V1 Magnitude	V	0	200 Vn	0.1 Vn	0	80 Vn
V2 Magnitude	V	0	200 Vn	0.1 Vn	0	80 Vn
V0 Magnitude	V	0	200 Vn	0.1 Vn	0	80 Vn
VAN RMS	V	0	200 Vn	0.1 Vn	0	80 Vn
VBN RMS	V	0	200 Vn	0.1 Vn	0	80 Vn
VCN RMS	V	0	200 Vn	0.1 Vn	0	80 Vn
Frequency	Hz	0	70	0.01	45	65
RTD 1	°C	-40	300	0.1	0	200
RTD 2	°C	-40	300	0.1	0	200
RTD 3	°C	-40	300	0.1	0	200
RTD 4	°C	-40	300	0.1	0	200
RTD 5	°C	-40	300	0.1	0	200
RTD 6	°C	-40	300	0.1	0	200
RTD 7	°C	-40	300	0.1	0	200
RTD 8	°C	-40	300	0.1	0	200
RTD 9	°C	-40	300	0.1	0	200
RTD 10	°C	-40	300	0.1	0	200
CL Input 1		-9999	9999	0.1	0	9999
CL Input 2		-9999	9999	0.1	0	9999
CL Input 3		-9999	9999	0.1	0	9999
CL Input 4		-9999	9999	0.1	0	9999
Volts/Hz W1	V/Hz	0	20	0.01	0	4

Current loop output measurement	Unit	Min.	Max.	Step	Default min.	Default max.
V/Hz W1 Thermal	%	0	200	0.01	0	120
Volts/Hz W2	V/Hz	0	20	0.01	0	4
V/Hz W2 Thermal	%	0	200	0.01	0	120
Hot Spot T	°C	-40	300	0.1	0	200
Top Oil T	°C	-40	300	0.1	0	200
Ambient T	°C	-40	300	0.1	0	200
LOL Status	Hr	1	300000	1	1	300000
Note These settings are for nominal 1A and 100/120 V versions only. For other nominal versions they need to be multiplied accordingly.						

Table 21 - Current loop output measurements

5 CONTROL AND SUPPORT SETTINGS

The control and support settings are part of the main menu and are used to configure the relay's global configuration. It includes the following submenu settings.

- Relay function configuration settings
- Open/close circuit breaker
- CT & VT ratio settings
- Reset LEDs
- Active protection setting group
- Password & language settings
- Circuit breaker control & monitoring settings
- Communications settings
- Measurement settings
- Event & fault record settings
- User interface settings
- Commissioning settings

5.1 System Data

This menu provides information for the device and general status of the relay.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
SYSTEM DATA				
Language	English	English, Francais, Deutsch, Español		
The default language used by the device. Selectable as English, French, German, Spanish, Chinese, Russian.				
Password	****			
Device default password.				
Sys. Fn. Links	0			1
Setting to allow the fixed function trip LED to be self resetting, **1**= self reset, **0** = latched.				
Description	MiCOM P643			
16 character relay description. Can be edited.				
Plant Reference	MiCOM			
Plant description. Can be edited.				
Model Number	P643?11???0010K			
Relay model number.				
Serial Number	149188B			
Relay serial number.				
Frequency	50 Hz	50 Hz	60 Hz	10Hz
Relay set frequency. Settable as 50 or 60Hz.				
Comms. Level				
Displays the conformance of the relay to the Courier Level 2 comms.				
Relay Address				
Sets the first rear port relay address.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
SYSTEM DATA				
Plant Status	0000000000000000			
Displays the circuit breaker plant status for up to 8 circuit breakers.				
Control Status	0000000000000000			
Not used.				
Active Group	1			
Displays the active settings group.				
Software Ref. 1	P643____1__040_B			
Software Ref. 2	P643____1__040_B			
Displays the relay software version including the protocol and relay model. Software Ref. 2 is displayed for relays with IEC 61850 protocol only and displays the software version of the Ethernet card.				
Opto I/P Status	0000000000000000			
Displays the status of the relay’s opto-isolated inputs as a binary string. **1** indicates an energized opto-isolated input and **0** a de-energized one.				
Relay O/P Status	0000001000000000			
Displays the status of the relay’s output contacts as a binary string. **1** indicates an operated state and **0** a non-operated state.				
Alarm Status 1	00000000000000000000000000000000			
This menu cell displays the status of the first 32 alarms as a binary string. **1** indicates an ON state and **0** an OFF state. Includes fixed and user settable alarms. See Data Type G96 in the Menu Database document, P64x/EN/MD for details.				
Alarm Status 2	00000000000000000000000000000000			
This menu cell displays the status of the second 32 alarms as a binary string. **1** indicates an ON state and **0** an OFF state. See Data Type G128 in the Menu Database document, P64x/EN/MD for details.				
Alarm Status 3	00000000000000000000000000000000			
This menu cell displays the status of the third 32 alarms as a binary string. **1** indicates an ON state and **0** an OFF state. Assigned specifically for platform alarms. See Data Type G228 in the Menu Database document, P64x/EN/MD for details.				
Usr Alarm Status 3	00000000000000000000000000000000			
This menu cell displays the status of the third 32 alarms as a binary string. **1** indicates an ON state and **0** an OFF state. Assigned specifically for user alarms. See Data Type G40 in the Menu Database document, P64x/EN/MD for details.				
Access Level	2			
Access Level. Read only. The table below describes the password control.				

Set the **Password Control** cell to	The **Access Level** cell displays	Operations	Type of Password required
0	0	**Read** access to all settings, alarms, event records and fault records	None
		Execute Control Commands, such as circuit breaker open/close. Reset of fault and alarm conditions. Reset LEDs. Clearing of event and fault records.	Level 1 Password
		Edit all other settings	Level 2 Password
1	1	**Read** access to all settings, alarms, event records and fault records	None
		Execute Control Commands, such as circuit breaker open/close. Reset of fault and alarm conditions. Reset LEDs. Clearing of event and fault records.	None
		Edit all other settings	Level 2 Password

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
SYSTEM DATA				
2 (Default)	2(Default)	**Read** access to all settings, alarms, event records and fault records	None	
		Execute Control Commands, such as circuit breaker open/close. Reset of fault and alarm conditions. Reset LEDs. Clearing of event and fault records.	None	
		Edit all other settings	None	
Password Control	2	0	2	1
Sets the menu access level for the relay. This setting can only be changed when level 2 access is enabled.				
Password Level 1	****			
Password level 1 setting (4 characters).				
Password Level 2	****			
Password level 2 setting (4 characters).				

Table 22 - System data settings

5.2 View Records

This menu provides information on fault and maintenance records. The relay records the last five fault records and the last ten maintenance records.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
VIEW RECORDS				
Select Event	0	0	511	
Setting range from 0 to 511. This selects the required event record from the possible 512 that can be stored. A value of 0 corresponds to the latest event.				
Menu Cell Ref	(From record)	Latched alarm active, Latched alarm inactive, Self reset alarm active, Self reset alarm inactive, Relay contact event, Opto-isolated input event, Protection event, General event, Fault record event, Maintenance record event		
Indicates the type of event.				
Time and Date	(From record)			
Time & Date Stamp for the event given by the internal Real Time Clock.				
Event text	Data.			
Up to 32 Character description of the Event. See the event sheet in the Measurements and Recording chapter, P64x/EN MR or the Menu Database document, P64x/EN/MD for details.				
Event Value	Data.			
32-bit binary string indicating ON (1) or OFF (0) status of relay contact or opto input or alarm or protection event depending on event type. Unsigned integer is used for maintenance records. See the event sheet in the Measurements and Recording chapter, P64x/EN MR or the Menu Database document, P64x/EN/MD for details.				
Select Fault	0	0	19	1
Setting range from 0 to 19. This selects the required fault record from the possible 20 that can be stored. A value of 0 corresponds to the latest fault.				
Faulted Phase	00000000			
Displays the faulted phase as a binary string, bits 0 – 8 = Start A/B/C/N Trip A/B/C/N.				
Start elements 1	00000000000000000000000000000000			

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
VIEW RECORDS				
32-bit binary string gives status of first 32 start signals. See Data Type G84 in the Menu Database document, P64x/EN/MD for details.				
Start elements 2	00000000000000000000000000000000			
32-bit binary string gives status of second 32 start signals. See Data Type G107 in the Menu Database document, P64x/EN/MD for details.				
Start elements 3	00000000000000000000000000000000			
32-bit binary string gives status of third 32 start signals. See Data Type G129 in the Menu Database document, P64x/EN/MD for details.				
Trip elements 1	00000000000000000000000000000000			
32-bit binary string gives status of first 32 trip signals. See Data Type G85 in the Menu Database document, P64x/EN/MD for details.				
Trip elements 2	00000000000000000000000000000000			
32-bit binary string gives status of second 32 trip signals. See Data Type G86 in the Menu Database document, P64x/EN/MD for details.				
Trip elements 3	00000000000000000000000000000000			
32-bit binary string gives status of third 32 trip signals. See Data Type G130 in the Menu Database document, P64x/EN/MD for details.				
Fault Alarms	0000001000000000			
32-bit binary string gives status of fault alarm signals. See Data Type G87 in the Menu Database document, P64x/EN/MD for details.				
Fault Time	(From record)			
Fault time and date.				
Fault type	Internal or external			
Internal or external fault type. See Data Type G193 in the Menu Database document, P64x/EN/MD for details.				
Active Group	Data			
Active setting group 1-4.				
System Frequency	Data			
System frequency.				
Fault Duration				
Fault duration. Time from the start until the undercurrent elements indicate the CB is open.				
CB Operate Time	Data.			
CB operating time. Time from protection trip to undercurrent elements indicating the CB is open.				
Relay Trip Time	Data.			
Relay trip time. Time from protection start to protection trip.				
The following cells provide measurement information of the fault : IA-1 to 5, IB-1 to 5, IC-1 to 5, IA to C-HV, IB-HV, IC-HV, IA-LV, IB-LV, IC-LV, IA-TV, IB-TV, IC-TV, I2-HV, I2-LV, I2-TV, IN-HV Mea Mag, IN-LV Mea Mag, IN-TV Mea Mag, VAN, VBN, VCN, Vx, V1, V2, VN Derived Mag, VAB, VBC, VCA, IA Diff, IB Diff, IC Diff, IA Bias, IB Bias, IC Bias, IREF HV LoZ Diff, IREF HV LoZ Bias, IREF LV LoZ Diff, IREF LV LoZ Bias, IREF TV LoZ Diff, IREF TV LoZ Bias, IREF Auto LoZ Diff, IREF Auto LoZ Bias, IREF HV HighZ Op, IREF LV HighZ Op, IREF TV HighZ Op, IREF Auto HighZ Op, IA Peak Mag, IB Peak Mag, IC Peak Mag, I2t Phase A, I2t Phase B, I2t Phase C, RTD 1 to 10, CLIO Input 1 to 4.				
Reset Indication	No	No, Yes		
Resets latched LEDs and latched relay contacts provided the relevant protection element has reset.				

Table 23 - View records settings

5.3 Measurements 1

This menu provides measurement information.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
MEASUREMENTS 1				
IA-1, 2 Magnitude	Data.			
IA-1, 2 Phase Angle	Data			
IB-1, 2 Magnitude	Data			
IB-1, 2 Phase Angle	Data			
IC-1, 2 Magnitude	Data			
IC-1, 2 Phase Angle	Data			
IA-3 Magnitude	Data. P643, P645			
IA-3 Phase Angle	Data. P643, P645			
IB-3 Magnitude	Data. P643, P645			
IB-3 Phase Angle	Data. P643, P645			
IC-3 Magnitude	Data. P643, P645			
IC-3 Phase Angle	Data. P643, P645			
IA-4, 5 Magnitude	Data. P645 only			
IA-4, 5 Phase Angle	Data. P645 only			
IB-4, 5 Magnitude	Data. P645 only			
IB-4, 5 Phase Angle	Data. P645 only			
IC-4, 5 Magnitude	Data. P645 only			
IC-4, 5 Phase Angle	Data. P645 only			
IA-HV, LV Magnitude	Data			
IA-HV, LV Phase Angle	Data			
IB-HV, LV Magnitude	Data			
IB-HV, LV Phase Angle	Data			
IC-HV, LV Magnitude	Data			
IC-HV, LV Phase Angle	Data			
IA-TV Magnitude	Data. P643, P645			
IA-TV Phase Angle	Data. P643, P645			
IB-TV Magnitude	Data. P643, P645			
IB-TV Phase Angle	Data. P643, P645			
IC-TV Magnitude	Data. P643, P645			
IC-TV Phase Angle	Data. P643, P645			
I0-1 Magnitude	Data. Zero sequence current of T1 CT			
I1-1 Magnitude	Data. Positive sequence current of T1 CT			
I2-1 Magnitude	Data. Negative sequence current of T1 CT			
IN-HV Measured Mag	Data.			
IN-HV Measured Angle	Data.			
IN-HV Derived Mag	Data.			
IN-HV Derived Angle	Data.			
I0-2 Magnitude	Data. Zero sequence current of T2 CT			
I1-2 Magnitude	Data. Positive sequence current of T2 CT			

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
MEASUREMENTS 1				
I2-2 Magnitude	Data. Negative sequence current of T2 CT			
IN-LV Mea Mag	Data.			
IN-LV Mea Ang	Data.			
IN-LV Deriv Mag	Data.			
IN-LV Deriv Ang	Data.			
I0-3 Magnitude	Data. Zero sequence current of T3 CT. P643, P645 only.			
I1-3 Magnitude	Data. Positive sequence current of T3 CT. P643, P645 only.			
I2-3 Magnitude	Data. Negative sequence current of T3 CT. P643, P645 only.			
IN-TV Mea Mag	Data. P643, P645 only.			
IN-TV Mea Ang	Data. P643, P645 only.			
IN-TV Deriv Mag	Data. P643, P645 only.			
IN-TV Deriv Ang	Data. P643, P645 only.			
I0-4 Magnitude	Data. Zero sequence current of T4 CT. P645 only.			
I1-4 Magnitude	Data. Positive sequence current of T4 CT. P645 only.			
I2-4 Magnitude	Data. Negative sequence current of T4 CT. P645 only.			
I0-5 Magnitude	Data. Zero sequence current of T5 CT. P645 only.			
I1-5 Magnitude	Data. Positive sequence current of T5 CT. P645 only.			
I2-5 Magnitude	Data. Negative sequence current of T5 CT. P645 only.			
IA-HV RMS	Data.			
IB-HV RMS	Data.			
IC-HV RMS	Data.			
IA-LV RMS	Data.			
IB-LV RMS	Data.			
IC-LV RMS	Data.			
IA-TV RMS	Data. P643, P645 only.			
IB-TV RMS	Data. P643, P645 only.			
IC-TV RMS	Data. P643, P645 only.			
VAN Magnitude	Data. P643, P645 only when optional three-phase VT is available.			
VAN Phase Angle	Data. P643, P645 only when optional three-phase VT is available.			
VBN Magnitude	Data. P643, P645 only when optional three-phase VT is available.			
VBN Phase Angle	Data. P643, P645 only when optional three-phase VT is available.			
VCN Magnitude	Data. P643, P645 only when optional three-phase VT is available.			
VCN Phase Angle	Data. P643, P645 only when optional three-phase VT is available.			
Vx Magnitude	Data.			
Vx Phase Angle	Data.			
V1 Magnitude	Data. Positive sequence voltage. P642 when two single phase VTs are available. P643, P645 when optional three-phase VT is available.			
V2 Magnitude	Data. Negative sequence voltage. P642 when two single phase VTs are available. P643, P645 when optional three-phase VT is available.			
V0 Magnitude	Data. Zero sequence voltage. P643, P645 only when optional three-phase VT is available.			
VN Derived Mag	Data. P643, P645 only when optional three-phase VT is available.			
VN Derived Angle	Data. P643, P645 only when optional three-phase VT is available.			

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
MEASUREMENTS 1				
VAB Magnitude	Data. P642 when two single phase VTs are available. P643, P645 when optional three-phase VT is available.			
VAB Phase Angle	Data. P642 when two single phase VTs are available. P643, P645 when optional three-phase VT is available.			
VBC Magnitude	Data. P642 when two single phase VTs are available. P643, P645 when optional three-phase VT is available.			
VBC Phase Angle	Data. P642 when two single phase VTs are available. P643, P645 when optional three-phase VT is available.			
VCA Magnitude	Data. P643, P645 when optional three-phase VT is available.			
VCA Phase Angle	Data. P642 when two single phase VTs are available. P643, P645 when optional three-phase VT is available.			
VAN RMS	Data. P643, P645 only when optional three-phase VT is available.			
VBN RMS	Data. P643, P645 only when optional three-phase VT is available.			
VCN RMS	Data. P643, P645 only when optional three-phase VT is available.			
Frequency	Data. P643, P645 only when optional three-phase VT is available.			

Table 24 - Measurements 1 settings

5.4 Measurements 2

This menu provides measurement information.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
MEASUREMENTS 2				
A Phase Watts	Data. P643, P645 only when optional three-phase VT is available.			
B Phase Watts	Data. P643, P645 only when optional three-phase VT is available.			
C Phase Watts	Data. P643, P645 only when optional three-phase VT is available.			
A Phase VARs	Data. P643, P645 only when optional three-phase VT is available.			
B Phase VARs	Data. P643, P645 only when optional three-phase VT is available.			
C Phase VARs	Data. P643, P645 only when optional three-phase VT is available.			
A Phase VA	Data. P643, P645 only when optional three-phase VT is available.			
B Phase VA	Data. P643, P645 only when optional three-phase VT is available.			
C Phase VA	Data. P643, P645 only when optional three-phase VT is available.			
3 Phase Watts	Data. P643, P645 only when optional three-phase VT is available.			
3 Phase VARs	Data. P643, P645 only when optional three-phase VT is available.			
3 Phase VA	Data. P643, P645 only when optional three-phase VT is available.			
3Ph Power Factor	Data. P643, P645 only when optional three-phase VT is available.			
APh Power Factor	Data. P643, P645 only when optional three-phase VT is available.			
BPh Power Factor	Data. P643, P645 only when optional three-phase VT is available.			
CPh Power Factor	Data. P643, P645 only when optional three-phase VT is available.			
3Ph WHours Fwd	Data. P643, P645 only when optional three-phase VT is available.			
3Ph WHours Rev	Data. P643, P645 only when optional three-phase VT is available.			
3Ph VArHours Fwd	Data. P643, P645 only when optional three-phase VT is available.			

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
MEASUREMENTS 2				
3Ph VArHours Rev	Data. P643, P645 only when optional three-phase VT is available.			
3Ph W Fix Demand	Data. P643, P645 only when optional three-phase VT is available.			
3Ph VAr Fix Demand	Data. P643, P645 only when optional three-phase VT is available.			
3Ph W Roll Demand	Data. P643, P645 only when optional three-phase VT is available.			
3Ph VAr Roll Demand	Data. P643, P645 only when optional three-phase VT is available.			
3Ph W Peak Demand	Data. P643, P645 only when optional three-phase VT is available.			
3Ph VAr Peak Demand	Data. P643, P645 only when optional three-phase VT is available.			
Reset Demand	No	No, Yes		
Reset demand measurements command. Can be used to reset the fixed, rolling and peak demand value measurements to 0.				

Table 25 - Measurements 2 settings

5.5 Measurements 3

This menu provides measurement information.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
MEASUREMENTS 3				
IA Differential	Data.			
IB Differential	Data.			
IC Differential	Data.			
IA Bias	Data.			
IB Bias	Data.			
IC Bias	Data.			
IA Diff 2H	Data.			
IB Diff 2H	Data.			
IC Diff 2H	Data.			
IA Diff 5H	Data.			
IB Diff 5H	Data.			
IC Diff 5H	Data.			
IREF HV LoZ Diff	Data.			
IREF HV LoZ Bias	Data.			
IREF LV LoZ Diff	Data.			
IREF LV LoZ Bias	Data.			
IREF TV LoZ Diff	Data. P643, P645 only.			
IREF TV LoZ Bias	Data. P643, P645 only.			
IREF Auto LoZ Diff	Data.			
IREF Auto LoZ Bias	Data.			
IREF HV HighZ Op	Data.			
IREF LV HighZ Op	Data.			
IREF LV HighZ Op	Data.			
IREF Auto HighZ Op	Data.			

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
MEASUREMENTS 3				
Thermal overload				
Hot Spot T	Data.			
Top Oil T	Data.			
Reset Thermal	No	Yes or No		
Reset thermal overload command. Resets thermal state to 0.				
Ambient T	Data.			
TOL Pretrip left	Data. Thermal overload pre-trip time left			
LOL status	Data. Accumulated loss of life			
Reset LOL	No	Yes or No		
Reset loss of life command. Resets life loss to Reset Life Hours setting.				
Rate of LOL	Data. (ROLOL)			
LOL Aging Factor	Data. Aging acceleration factor (FAA)			
Lres at designed	Data. Residual life hours at design temperature ΘH,r			
FAA,m	Data. Mean aging acceleration factor (FAA,m)			
Lres at FAA,m	Data. Residual life hours at FAA,m (Lres(FAA,m))			
Volts/Hz				
Volts/Hz W1	Data. P643 and P645 only when optional three-phase VT is available.			
V/Hz W1 tPretrip	Data. P643 and P645 only when optional three-phase VT is available.			
V/Hz W1 Thermal	Data. P643 and P645 only when optional three-phase VT is available.			
Reset V/Hz W1	No	Yes or No. P643 and P645 only when optional three-phase VT is available.		
Volts/Hz W2	Data.			
V/Hz W2 tPretrip	Data.			
V/Hz W2 Thermal	Data.			
Reset V/Hz W2	No	Yes or No		
RTD 1 to 10 label	Data.			
RTD Open Cct	00000000			
Displays the status of the eight RTDs as a binary string. 0 = No Open Circuit, 1 = Open Circuit. The Open Cct alarms are latched.				
RTD Short Cct	00000000			
Displays the status of the eight RTDs as a binary string. 0 = No Short Circuit, 1 = Short Circuit. The Short Cct alarms are latched.				
RTD Data Error	00000000			
Displays the status of the eight RTDs as a binary string. 0 = No Data Error, 1 = Data Error. The Data Error alarms are latched.				
Reset RTD Flags	No	Yes or No		
Reset RTD alarms command. Resets latched RTD Open Cct, Short Cct, Data Error alarms.				
CLIO Input 1	Data. Current loop (transducer) input 1.			
CLIO Input 2	Data. Current loop (transducer) input 2.			
CLIO Input 3	Data. Current loop (transducer) input 3.			
CLIO Input 4	Data. Current loop (transducer) input 4.			

Table 26 - Measurements 3 settings

5.6 Date and Time

Displays the date and time as well as the battery condition.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
DATE AND TIME				
Date/Time	Data			
Displays the relay's date and time.				
IRIG-B Sync.	Disabled	Disabled or Enabled		
Enables or disables the IRIG-B time synchronization.				
IRIG-B Status	Data	Card not fitted/Card failed/Signal healthy/No signal		
Displays the status of IRIG-B.				
Battery Status	Dead or Healthy			
Displays whether the battery is healthy or not.				
Battery Alarm	Enabled	Disabled or Enabled		
Enables or disables battery alarm. The battery alarm needs to be disabled when a battery is removed or not used.				
SNTP Status	Data	Disabled/Trying Server1/ Trying Server 2/Server 1 OK/Server 2 OK/No response/No Valid Clock		
Displays information about the SNTP time synchronization status				
Local Time Enable	Fixed	Disable/Fixed/Flexible		
Setting to turn on/off local time adjustments. **Disabled** - No local time zone is maintained. Time synchronization from any interface is used to directly set the master clock. All displayed (or read) times on all interfaces are based on the master clock with no adjustment. **Fixed** - A local time zone adjustment can be defined using the Local Time offset setting. All interfaces then use local time except SNTP time synchronization and IEC61850 timestamps. **Flexible** - A local time zone adjustment can be defined using the Local Time offset setting. Each interface can then be assigned to the UTC zone or local time zone with the exception of the local interfaces which are always in the local time zone and IEC61850/SNTP which is always in the UTC zone.				
LocalTime Offset	0 min	-720 min	720 min	1 min
Setting to specify an offset of -12 to +12 hrs in 15 minute intervals for the local time zone. This adjustment is applied to the time, based on the master clock which is UTC/GMT				
DST Enable	Enabled	Disabled or Enabled		
Setting to turn on/off daylight saving time adjustment to local time.				
DST Offset	60 min	30 min	60 min	30 min
Setting to specify the daylight saving offset, used for the time adjustment to local time.				
DST Start	Last	First/Second/Third/Fourth/Last		
Setting to specify the week of the month in which daylight saving time adjustment starts				
DST Start Day	Sunday	Sunday/Monday/Tuesday/Wednesday/ Thursday/Friday/Saturday		
Setting to specify the day of the week in which daylight saving time adjustment starts				
DST Start Month	March	January/February/March/ April/May/June/July/August/September/ November/ December		
Setting to specify the month in which daylight saving time adjustment starts				
DST Start Mins	60 min	0 min	1425 min	15 min
Setting to specify the time of day in which daylight saving time adjustment starts. This is set relative to 00:00 hrs on the selected day when the time adjustment is to start.				
DST End	Last	First/Second/Third/Fourth/Last		
Setting to specify the week of the month in which daylight saving time adjustment ends.				
DST End Day	Sunday	Sunday/Monday/Tuesday/Wednesday/ Thursday/Friday/Saturday		

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
DATE AND TIME				
Setting to specify the day of the week in which daylight saving time adjustment ends				
DST End Month	October	January/February/March/ April/May/June/July/August/September/ November/ December		
Setting to specify the month in which daylight saving time adjustment ends				
DST End Mins	60 min	0 min	1425 min	15 min
Setting to specify the time of day in which daylight saving time adjustment ends. This is set relative to 00:00 hrs on the selected day when time adjustment is to end.				
RP1 Time Zone	Local	UTC/Local		
Setting for the rear port 1 interface to specify if the time synchronization received is local or universal time coordinated.				
RP2 Time Zone	Local	UTC/Local		
Setting for the rear port 2 interface to specify if the time synchronization received is local or universal time coordinated.				
DNPOE Time Zone	Local	UTC/Local		
Setting to specify if the time synchronization received is the local or universal time coordinate when using DNP3.0 over Ethernet				
Tunnel Time Zone	Local	UTC/Local		
Setting to specify if the time synchronization received is the local or universal time coordinate when 'tunnelling' the courier protocol over Ethernet.				

Table 27 - Date and time settings

5.7 CT and VT Ratios

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
CT AND VT RATIOS				
Main VT location	HV	HV, LV, TV.		
Sets main VT location in P643 and P645.				
Aux' VT Location	HV	HV, LV		
Sets auxiliary VT location in the P642.				
Main VT Primary	110.0 V	100 V	1 MV	1 V
Main voltage transformer input, primary voltage setting. P643 and P645 only.				
Main VT Sec'y	110.0 V	80 V	140 V	1 V
Main transformer input, secondary voltage setting. P643 and P645 only.				
Aux' VT Primary	110.0 V	100 V	1 MV	1 V
In the P643 and P645 is the single phase VT primary voltage used for W2 overfluxing. In the P642, it is the single phase VTs primary voltage.				
Aux' VT Sec'y	110.0 V	80 V	140 V	1 V
In the P643 and P645 is the single phase VT secondary voltage used for W2 overfluxing. . In the P642, it is the single phase VTs secondary.				
T1 CT				
Polarity	Standard	Standard or Inverted		
Current transformer 1 polarity with respect to the protected object				
Primary	300 A	1 A	30000 A	1 A
Current transformer 1 primary nominal current				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
CT AND VT RATIOS				
Secondary	1 A	1 A	5 A	4 A
Current transformer 1 secondary nominal current				
T2 CT				
Polarity	Standard	Standard or Inverted		
Current transformer 2 polarity with respect to the protected object				
Primary	300 A	1 A	30000 A	1 A
Current transformer 2 primary nominal current				
Secondary	1 A	1 A	5 A	4 A
Current transformer 2 secondary nominal current				
T3 CT (P643/P645)				
Polarity	Standard	Standard or Inverted		
Current transformer 3 polarity with respect to the protected object				
Primary	300 A	1 A	30000 A	1 A
Current transformer 3 primary nominal current				
Secondary	1 A	1 A	5 A	4 A
Current transformer 3 secondary nominal current				
T4 CT (P643/P645)				
Polarity	Standard	Standard or Inverted		
Current transformer 4 polarity with respect to the protected object				
Primary	300 A	1 A	30000 A	1 A
Current transformer 4 primary nominal current				
Secondary	1 A	1 A	5 A	4 A
Current transformer 4 secondary nominal current				
T5 CT (P643/P645)				
Polarity	Standard	Standard or Inverted		
Current transformer 5 polarity with respect to the protected object				
Primary	300 A	1 A	30000 A	1 A
Current transformer 5 primary nominal current				
Secondary	1 A	1 A	5 A	4 A
Current transformer 5 secondary nominal current				
TN1 CT				
Polarity	Standard	Standard or Inverted		
Single phase current transformer 1 polarity with respect to the protected object				
Primary	300 A	1 A	30000 A	1 A
Single phase current transformer 1 primary nominal current				
Secondary	1 A	1 A	5 A	4 A
Single phase current transformer 1 secondary nominal current				
TN2 CT				
Polarity	Standard	Standard or Inverted		
Single phase current transformer 2 polarity with respect to the protected object				
Primary	300 A	1 A	30000 A	1 A
Single phase current transformer 2 primary nominal current				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
CT AND VT RATIOS				
Secondary	1 A	1 A	5 A	4 A
Single phase current transformer 2 secondary nominal current				
TN3 CT (P643/P645)				
Polarity	Standard	Standard or Inverted		
Single phase current transformer 3 polarity with respect to the protected object				
Primary	300 A	1 A	30000 A	1 A
Single phase current transformer 3 primary nominal current				
Secondary	1 A	1 A	5 A	4 A
Single phase current transformer 3 secondary nominal current				

Table 28 - CT and VT ratio settings

5.8 Record Control

It is possible to disable the reporting of events from all interfaces that support setting changes. The settings that control the reporting of various types of events are in the Record Control column. The effect of setting each to disabled is as follows:

Menu text	Default setting	Available settings
RECORD CONTROL		
Clear Events	No	No or Yes
Selecting **Yes** clears the existing event log and generates an event which shows the events have been erased.		
Clear Faults	No	No or Yes
Selecting **Yes** erases the existing fault records from the relay.		
Clear Maint.	No	No or Yes
Selecting **Yes** erases the existing maintenance records from the relay.		
Alarm Event	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for all alarms.		
Relay O/P Event	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any change in relay output contact state.		
Opto Input Event	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any change in logic input state.		
General Event	Enabled	Enabled or Disabled
Disabling this setting means that no General Events is generated. See the event record sheet in the menu database chapter, P64x/EN MD for a list of general events.		
Fault Rec Event	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any fault that produces a fault record.		
Maint. Rec Event	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any maintenance records.		
Protection Event	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any operation of the protection elements.		
Clear Dist Recs	No	No or Yes
Selecting Yes clears the existing disturbance records from the relay.		

Menu text	Default setting	Available settings
RECORD CONTROL		
DDB 31 - 0	11111111111111111111111111111111	
32-bit setting to enable or disable the event recording for DDBs 0-31. For each bit **1** = event recording Enabled, **0** = event recording Disabled.		
DDB 2047 - 2016	11111111111111111111111111111111	
32-bit setting to enable or disable the event recording for DDBs 2047 – 2016. For each bit **1** = event recording Enabled, **0** = event recording Disabled. There are similar cells showing 32-bit binary strings for all DDBs from 0 – 2016. The first and last 32-bit binary strings only are shown here.		

Table 29 - Record control settings

5.9 Disturbance Recorder Settings

The disturbance recorder settings include the record duration and trigger position, selection of analog and digital signals to record, and the signal sources that trigger the recording.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
DISTURB RECORDER				
Duration	1.5 s	0.1 s	10.5 s	0.01 s
Overall recording time setting.				
Trigger Position	33.3%	0%	100%	0.1%
Trigger point setting as a percentage of the duration. For example, the default settings show the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1 s post fault recording times.				
Trigger Mode	Single	Single or Extended		
If set to single mode, and if a further trigger occurs while a recording is taking place, the recorder ignores the trigger. However, if this is set to **Extended**, the post trigger timer is reset to zero, extending the recording time.				
P642	P643	P645	Default Setting	
Analog. Channel 1	Analog. Channel 1	Analog. Channel 1	IA-1	
Selects any available analog input to be assigned to this channel. The options are Unused, VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IADIFF, IBDIFF, ICDIFF, IABIAS, IBBIAS, ICBIAS, REFHVDIFF, REFHVBIAS, REFLVDIFF, REFLVBIAS, REFTVDIFF, REFTVBIAS, REFAUTODIFF, REFAUTOBIAS, REFHVOP, REFLVOP, REFTVOP, REFAUTOOP, Frequency, VAB or VBC depending on the model.				
Analog. Channel 2	Analog. Channel 2	Analog. Channel 2	IB-1	
Analog. Channel 3	Analog. Channel 3	Analog. Channel 3	IC-1	
Analog. Channel 4	Analog. Channel 4	Analog. Channel 4	IN-1	
Analog. Channel 5	Analog. Channel 5	Analog. Channel 5	IA-2	
Analog. Channel 6	Analog. Channel 6	Analog. Channel 6	IB-2	
Analog. Channel 7	Analog. Channel 7	Analog. Channel 7	IC-2	
Analog. Channel 8	Analog. Channel 8	Analog. Channel 8	IN-2	
	Analog. Channel 9	Analog. Channel 9	IA-3	
	Analog. Channel 10	Analog. Channel 10	IB-3	
	Analog. Channel 11	Analog. Channel 11	IC-3	
	Analog. Channel 12	Analog. Channel 12	IN-3	
		Analog. Channel 13	IA-4	
		Analog. Channel 14	IB-4	

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
DISTURB RECORDER				
		Analog. Channel 15	IC-4	
		Analog. Channel 16	IA-5	
		Analog. Channel 17	IB-5	
		Analog. Channel 18	IC-5	
Analog. Channel 9	Analog. Channel 13	Analog. Channel 19	IA-Diff	
Analog. Channel 10	Analog. Channel 14	Analog. Channel 20	IB-Diff	
Analog. Channel 11	Analog. Channel 15	Analog. Channel 21	IC-Diff	
Analog. Channel 12	Analog. Channel 16	Analog. Channel 22	IA-Bias	
Analog. Channel 13	Analog. Channel 17	Analog. Channel 23	IB-Bias	
Analog. Channel 14	Analog. Channel 18	Analog. Channel 24	IC-Bias	
Analog. Channel 15	Analog. Channel 19	Analog. Channel 25	LoZREF-HV-Diff	
Analog. Channel 16	Analog. Channel 20	Analog. Channel 26	LoZREF-HV-Bias	
Analog. Channel 17	Analog. Channel 21	Analog. Channel 27	LoZREF-LV-Diff	
Analog. Channel 18	Analog. Channel 22	Analog. Channel 28	LoZREF-LV Bias	
Analog. Channel 19	Analog. Channel 23	Analog. Channel 29	LoZREF-TV-Diff	
	Analog. Channel 24	Analog. Channel 30	LoZREF-TV-Bias	
Digital Inputs 1 to 32	Relays 1 to 12 and Optos 1 to 12	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals		
	Analog. Channel 25		Vx	
	Analog. Channel 26		Frequency	
The digital channels can be mapped to any of the opto isolated inputs or output contacts, in addition to several internal relay digital signals such as protection starts and LEDs.				
Inputs 1 to 32 Trigger	No Trigger except Dedicated Trip Relay O/Ps which are set to Trigger L/H	No Trigger, Trigger L/H, Trigger H/L		
Any of the digital channels can be selected to trigger the disturbance recorder on either a low-to-high (L/H) or a high-to-low (H/L) transition.				

Table 30 - Disturbance recorder settings

5.10 Measurement Setup

Menu text	Default settings	Available settings
MEASURE'T SETUP		
Default Display	Description	3Ph + N Current/3Ph Neutral Voltage/Power/Date and Time/Description/Plant Reference/Frequency/Access Level
Used to select the default display from a range of options. The options **3Ph Neutral Voltage** and **Power** are available on the P643 and P645 only. You can also view the other default displays from the default level using the ◁ □and ▷ keys. However once the 15 minute timeout elapses the default display reverts to that selected by this setting.		
Local Values	Primary	Primary/Secondary
This setting controls whether measured values from the front panel user interface and the front courier port are displayed as primary or secondary quantities.		
Remote Values	Primary	Primary/Secondary
Controls whether measured values from the rear communication port are displayed as primary or secondary quantities.		

Menu text	Default settings	Available settings
MEASURE'T SETUP		
Measurement Ref.	VX (P642) VA (P643,5)	Vx, VA, VB, VC (P643,5 only) VAB, VBC (P642 only) IA1, IB1, IC1, IA2, IB2, IC2 (P642,3,5) IA3, IB3, IC3 (P643,5 only) IA4, IB4, IC4, IA5, IB5, IC5 (P645 only)
Sets the phase reference for all angular measurements made by the relay.		
Measurement Mode	0	0 to 3 step 1
This setting is used to control the signing of the real and reactive power quantities; the signing convention used is defined in the Measurements and Recording section (P64x/EN MR)		

Table 31 - Measure't setup settings

5.11 Communications

The communications settings apply to the rear communications ports only and depend on the particular protocol being used. For further details see the *SCADA communications section (P64x/EN SC)*.

The Communications Settings have been divided into these sections:

- Section 5.11.1 - Communications Settings for Courier Protocol
- Section 5.11.2 - Communications Settings for MODBUS Protocol
- Section 5.11.3 - Communications Settings for IEC60870-5-103 Protocol
- Section 5.11.4 - Communications Settings for DNP3.0 Protocol
- Section 5.11.5 - Communications Settings for Ethernet Port
- Section 5.11.6 - Rear Port 2 Connection Settings

5.11.1 Communications Settings for Courier Protocol

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
COMMUNICATIONS				
RP1 Protocol	Courier			
Indicates the communications protocol used on the rear communications port.				
RP1 Address	255	0	255	1
This cell sets the unique address for the relay so that only one relay is accessed by master station software.				
RP1 Inactiv Timer	15 mins.	1 mins.	30 mins.	1 min.
This cell controls how long the relay waits without receiving any messages on the rear port before it reverts to its default state, including resetting any password access that was enabled.				
RP1 Baud Rate	19200 bits/s	9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. Both the relay and master station must be set to the same speed.				
RP1 Parity	None	Odd, Even or None		
Communications parity				
RP1 Meas Period	15 s	1 s	60 s	1 s

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
COMMUNICATIONS				
Defines the measurement period for the cyclic measurements of the Courier protocol.				
RP1 Physical Link	Copper	Copper, Fiber Optic or KBus		
This cell defines whether an electrical EIA(RS)485, fiber optic or KBus connection is being used for communication between the master station and relay. If **Fiber Optic** is selected, the optional fiber optic communications board is required.				
RP1 Card Status		K-Bus OK, EIA485 OK or Fiber Optic OK		
First Rear Port (RP1) Courier protocol status				
RP1 Port Config.	KBus	KBus or EIA(RS)485		
Defines whether KBus or EIA(RS)485 is being used for communication between the master station and relay on Rear Port 1.				
RP1 Comms Mode	IEC60870 FT1.2 Frame	IEC60870 FT1.2 Frame or 10-bit No Parity		
The choice is either IEC60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity.				
RP1 Baud Rate	19200 bits/s	9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. Both the relay and master station must be set to the same speed.				

Table 32 - Communications settings for Courier protocol

5.11.2 Communications Settings for MODBUS Protocol

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
COMMUNICATIONS				
RP1 Protocol	MODBUS			
Indicates the communications protocol used on the rear communications port.				
RP1 Address	1	1	247	1
This cell sets the unique address for the relay so that only one relay is accessed by master station software.				
RP1 Inactiv Timer	15 mins.	1 mins.	30 mins.	1 min.
This cell controls how long the relay waits without receiving any messages on the rear port before it reverts to its default state, including resetting any password access that was enabled.				
RP1 Baud Rate	19200 bits/s	9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. Both the relay and master station must be set to the same speed.				
RP1 Parity	None	Odd, Even or None		
This cell controls the parity format used in the data frames. Both the relay and master station must be set to the same parity.				
RP1 Physical Link	Copper	Copper or Fiber Optic		
This cell defines whether an electrical EIA(RS) 485 or fiber optic connection is being used for communication between the master station and relay. If **Fiber Optic** is selected, the optional fiber optic communications board is required.				
MODBUS IEC Time	Standard	Standard or Reverse		
When **Standard** is selected, the time format complies with IEC60870-5-4 requirements so that byte 1 of the information is transmitted first, followed by bytes 2 through to 7. If **Reverse** is selected the transmission of information is reversed.				

Table 33 - Communications settings for MODBUS protocol

5.11.3 Communications Settings for IEC60870-5-103 Protocol

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
COMMUNICATIONS				
RP1 Protocol	IEC60870-5-103			
Indicates the communications protocol used on the rear communications port.				
RP1 Address	1	0	255	1
This cell sets the unique address for the relay so that only one relay is accessed by master station software.				
RP1 Inactiv Timer	15 mins.	1 mins.	30 mins.	1 min.
This cell controls how long the relay waits without receiving any messages on the rear port before it reverts to its default state, including resetting any password access that was enabled.				
RP1 Baud Rate	19200 bits/s	9600 bits/s or 19200 bits/s		
This cell controls the communication speed between relay and master station. Both the relay and master station must be set to the same speed.				
RP1 Measure’t Period	15 s	1 s	60 s	1 s
Defines the measurement period for the cyclic measurements of the IEC60870-5-103 protocol.				
RP1 Physical Link	Copper	Copper or Fiber Optic		
This cell defines whether an electrical EIA(RS) 485 or fiber optic connection is being used for communication between the master station and relay. If Fiber Optic is selected, the optional fiber optic communications board is needed.				
RP1 CS103 Blocking	Disabled	Disabled, Monitor Blocking or Command Blocking		
There are three settings associated with this cell:				
Disabled	No blocking selected.			
Monitor Blocking	When the monitor blocking DDB Signal is active high, either by energizing an opto input or control input, reading of the status information and disturbance records is not permitted. When in this mode the relay returns a **termination of general interrogation** message to the master station.			
Command Blocking	When the command blocking DDB signal is active high, either by energizing an opto input or control input, all remote commands areignored, such as CB Trip/Close and change setting group. When in this mode the relay returns a **negative acknowledgement of command** message to the master station.			

Table 34 - Communications settings for IEC60870-5-103 protocol

5.11.4 Communications Settings for DNP3.0 Protocol

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
COMMUNICATIONS				
RP1 Protocol	DNP 3.0			
Indicates the communications protocol used on the rear communications port.				
RP1 Address	3	0	65534	1
This cell sets the unique address for the relay so that only one relay is accessed by master station software.				
RP1 Baud Rate	19200 bits/s	1200 bits/s, 2400 bits/s, 4800 bits/s, 9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. Both the relay and master station must be set to the same speed.				
RP1 Parity	None	Odd, Even or None		
This cell controls the parity format used in the data frames. Both the relay and master station must be set to the same parity.				
RP1 Physical Link	Copper	Copper or Fiber Optic		

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
COMMUNICATIONS				
This cell defines whether an electrical EIA(RS) 485 or fiber optic connection is being used for communication between the master station and relay. If **Fiber Optic** is selected, the optional fiber optic communications board is required.				
RP1 Time Sync.	Disabled	Disabled or Enabled		
If set to **Enabled** the DNP3.0 master station can be used to synchronize the time on the relay. If set to **Disabled** either the internal free running clock or IRIG-B input are used.				

Table 35 - Communications settings for DNP3.0 protocol

5.11.5 Communications Settings for Ethernet Port

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
COMMUNICATIONS				
NIC Protocol	IEC61850			
Indicates that IEC61850 is used on the rear Ethernet port.				
NIC MAC Address	Ethernet MAC Address			
Shows the MAC address of the rear Ethernet port.				
NIC Tunl Timeout	5 mins	1 min	30 mins	1 min
Time waited before an inactive tunnel to MiCOM S1 Studio is reset.				
NIC Link Report	Alarm	Alarm, Event, None		
Configures how a failed/unfitted network link (copper or fiber) is reported: Alarm - an alarm is raised for a failed link Event - an event is logged for a failed link None - nothing reported for a failed link				

Table 36 - Communications settings for Ethernet port

5.11.6 Rear Port 2 Connection Settings

The settings shown are those configurable for the second rear port which is only available with the Courier protocol.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
COMMUNICATIONS				
RP2 Protocol	Courier			
Shows the communications protocol used on the 2nd rear communications port.				
RP2 Card Status		Unsupported, Card not fitted, EIA232 OK, EIA485 OK, K-Bus OK.		
Second Rear Port (RP2) Courier protocol status				
RP2 Port Config.	RS232	EIA(RS)232, EIA(RS)485 or KBus		
This cell defines whether an electrical EIA(RS)232, EIA(RS)485 or KBus is being used for communication.				
RP2 Comms. Mode	IEC60870 FT1.2 Frame	IEC60870 FT1.2 Frame or 10-bit No Parity		
The choice is either IEC60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity.				
RP2 Address	255	0	255	1

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
COMMUNICATIONS				
This cell sets the unique address for the relay so that only one relay is accessed by master station software.				
RP2 Inactiv Timer	15 mins.	1 mins.	30 mins.	1 min.
This cell controls how long the relay waits without receiving any messages on the rear port before it reverts to its default state, including resetting any password access that was enabled.				
RP2 Baud Rate	19200 bits/s	9600 bits/s, 19200 bits/s or 38400 bits/s		
This cell controls the communication speed between relay and master station. It is important that both relay and master station are set to the same speed.				
DNP Need Time	10	1	30	1
The duration of time waited before requesting another time sync from the master.				
DNP App Fragment	2048	100	2048	1
The maximum message length (application fragment size) transmitted by the relay.				
DNP App Timeout	2	1	120	1
Duration of time waited, after sending a message fragment and awaiting a confirmation from the master.				
DNP SBO Timeout	10	1	10	1
Duration of time waited, after receiving a select command and awaiting an operate confirmation from the master.				

Table 37 - RP2 protocol

5.12 Commissioning Tests

There are menu cells which allow the status of the opto-isolated inputs, output relay contacts, internal digital data bus (DDB) signals and user-programmable LEDs to be monitored. Also there are cells used to test the operation of the output contacts and user-programmable LEDs.

Menu Text	Default Setting	Available Settings
COMMISSION TESTS		
Opto I/P Status	0000000000000000	
This menu cell displays the status of the relay’s opto-isolated inputs as a binary string. **1** indicates an energized opto-isolated input and **0** a de-energized one.		
Relay O/P Status	0000000000000000	
This menu cell displays the status of the relay’s output contacts as a binary string. **1** indicates an operated state and **0** a non-operated state. When the **Test Mode** cell is set to **Enabled** the **Relay O/P Status** cell does not show the current status of the output relays so it cannot be used to confirm operation of the output relays. Therefore it is necessary to monitor the state of each contact in turn.		
Test Port Status	00000000	
This menu cell displays the status of the eight digital data bus (DDB) signals that have been allocated in the **Monitor Bit** cells.		
LED Status	00000000	
This cell is an 8-bit binary string that indicates which of the LEDs are ON.		
Monitor Bit 1	64 (LED 1)	0 to 1407 See PSL section for details of digital data bus signals
The eight **Monitor Bit** cells allow the user to select the status of which digital data bus signals can be observed in the **Test Port Status** cell or from the monitor/download port.		
Monitor Bit 8	71 (LED 8)	0 to 1407

Menu Text	Default Setting	Available Settings
COMMISSION TESTS		
The eight **Monitor Bit** cells allow the user to select the status of which digital data bus signals can be observed in the **Test Port Status** cell or from the monitor/download port.		
Test Mode	Disabled	Disabled, Test Mode, Contacts Blocked
The Test Mode menu cell allows secondary injection testing to be performed on the relay without operating the trip contacts. It also enables a facility to test the output contacts directly by applying menu-controlled test signals. To select test mode, set the Test Mode menu cell to **Test Mode**. This takes the relay out of service and blocks the maintenance counters. In Test Mode an alarm condition is recorded, the yellow **Out of Service** LED goes ON, and an alarm message **Prot'n. Disabled** is given. This also freezes any information stored in the CB Condition column and in IEC60870-5-103 builds, Test Mode changes the Cause of Transmission, COT, to Test Mode. To enable testing of output contacts, set the **Test Mode** cell to **Contacts Blocked**. This blocks the protection from operating the contacts and enables the test pattern and contact test functions, which can be used to manually operate the output contacts. Once testing is complete, set the cell back to **Disabled** so the relay can return to service.		
Test Pattern	00000000000000000000000000000000	0 = Not Operated 1 = Operated
This cell is used to select the output relay contacts tested when the **Contact Test** cell is set to **Apply Test**.		
Contact Test	No Operation	No Operation, Apply Test, Remove Test
When the **Apply Test** command in this cell is issued the contacts set for operation (set to **1**) in the **Test Pattern** cell change state. After the test has been applied the command text on the LCD changes to **No Operation** and the contacts remain in the Test State until reset issuing the **Remove Test** command. The command text on the LCD again reverts to **No Operation** after the **Remove Test** command has been issued. Note: When the **Test Mode** cell is set to **Enabled** the **Relay O/P Status** cell does not show the current status of the output relays, so cannot be used to confirm operation of the output relays. Therefore it is necessary to monitor the state of each contact in turn.		
Test LEDs	No Operation	No Operation Apply Test
When the **Apply Test** command in this cell is issued, the 8 (P642/P643) or 18 (P645) user-programmable LEDs are ON for approximately 2 seconds. When they go OFF, the command text on the LCD reverts to **No Operation**.		
Red LED Status	000000000000000000	
This cell is an 18-bit binary string that indicates which of the user-programmable LEDs on the relay are ON. The Red LED input is active when accessing the relay from a remote location; **1** indicates that a particular LED is ON and **0** OFF. If both the Green and Red LED status bits are ON, it means the LED is yellow. This only applies to the P645 which has programmable tri-color LEDs – red/yellow/green.		
Green LED Status	000000000000000000	
This cell is an 18-bit binary string that indicates which of the user-programmable LEDs on the relay are ON. The Green LED input is active when accessing the relay from a remote location; **1** indicates that a particular LED is ON and **0** OFF. If both the Green and Red LED status bits are ON, it means the LED is yellow. This only applies to the P645 which has programmable tri-color LEDs – red/yellow/green.		
DDB 31 - 0	00000000000000000000001000000000	
Displays the status of DDB signals 0-31.		
DDB 2047 - 2016	00000000000000000000000000000000	
Displays the status of DDB signals 1407 – 1376. There are similar cells showing 32-bit binary strings for all DDBs from 0 – 1407. The first and last 32-bit words only are shown here.		

Table 38 - Commission tests

5.13 Opto Configuration

Menu text	Default setting	Setting range		Step size
		Min.	Max.	

OPTO CONFIG.		
Global Nominal V	48 - 54 V	24 - 27, 30 - 34, 48 - 54, 110 - 125, 220 - 250, Custom
Sets the nominal battery voltage for all opto inputs by selecting one of the five standard ratings in the Global Nominal V settings. If Custom is selected, each opto input can be set individually to a nominal voltage value.		
Opto Input 1	48 - 54 V	24 - 27, 30 - 34, 48 - 54, 110 - 125, 220 - 250
Each opto input can be set individually to a nominal voltage value if custom is selected for the global setting.		
Opto Input 2 - 40	48 - 54 V	24 - 27, 30 - 34, 48 - 54, 110 - 125, 220 - 250
Each opto input can be set individually to a nominal voltage value if custom is selected for the global setting.		
Opto Filter Cntl.	1111111111111111 11111111	0 = Disable Filtering 1 = Enable filtering
A binary string is used to represent the opto inputs available. A **1** or **0** is used to enable or disable for each input a pre-set filter of ½ cycle that renders the input immune to induced ac noise on the wiring.		
Characteristics	Standard 60% - 80%	Standard 60% - 80%, 50% - 70%
Selects the pick-up and drop-off characteristics of the optos. The standard setting means the optos nominally provide a Logic 1 or ON value for voltages ≥80% of the set lower nominal voltage, and a Logic 0 or OFF value for the voltages ≤60% of the set higher nominal voltage.		

Table 39 - Opto config

5.14 Control Input Configuration

The control inputs function as software switches that can be set or reset either locally or remotely. These inputs can be used to trigger any function they are connected to as part of the PSL.

Menu text	Default setting	Setting range	Step size
CTRL I/P CONFIG.			
Hotkey Enabled	11111111111111111111111111111111		
Setting to allow the control inputs to be individually assigned to the **Hotkey** menu by setting **1** in the appropriate bit in the **Hotkey Enabled** cell. The hotkey menu allows the control inputs to be set, reset or pulsed without the need to enter the **CONTROL INPUTS** column.			
Control Input 1	Latched	Latched, Pulsed	
Configures the control inputs as either **latched** or **pulsed**. A latched control input remains in the set state until a reset command is given, either by the menu or the serial communications. A pulsed control input stays energized for 10 ms after the set command is given, then resets automatically (no reset command is required).			
Ctrl Command 1	Set/Reset	Set/Reset, In/Out, Enabled/Disabled, On/Off	
Allows the SET / RESET text, displayed in the hotkey menu, to be changed to something more suitable for the application of an individual control input, such as **ON / OFF** or **IN / OUT**.			
Control Input 2 to 32	Latched	Latched, Pulsed	
Configures the control inputs as either **latched** or **pulsed**.			
Ctrl Command 2 to 32	Set/Reset	Set/Reset, In/Out, Enabled/Disabled, On/Off	
Allows the SET / RESET text, displayed in the hotkey menu, to be changed to something more suitable for the application of an individual control input, such as **ON / OFF** or **IN / OUT**.			

Table 40 - Control input config

5.15 Function Keys

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
FUNCTION KEYS				
Fn. Key Status	0000000000			
Displays the status of each function key.				
Fn. Key 1	Unlocked(Enabled)	Disable, Lock, Unlock(Enable)		
Setting to activate the function key. The **Lock** setting allows a function key output that is set to toggle mode to be locked in its current active state.				
Fn. Key 1 Mode	Toggle	Toggle, Normal		
Sets the function key to toggle or normal mode. In **Toggle** mode, the first keypress latches the function key DDB output signal ON and the next keypress resets the function key DDB output to OFF. This feature can be used to enable or disable relay functions. In **Normal** mode the function key DDB signal output goes ON (high) when the key is pressed and OFF when the key is released.				
Fn. Key 1 Label	Function Key 1			
Allows the text of the function key to be changed to something more suitable for the application.				
Fn. Key 2 to 10	Unlock(Enable)	Disable, Lock, Unlock(Enable)		
Setting to activate the function key. The **Lock** setting allows a function key output that is set to toggle mode to be locked in its current active position.				
Fn. Key 2 to 10 Mode	Toggle	Toggle, Normal		
Sets the function key to toggle or normal mode. In **Toggle** mode, the first keypress latches the function key DDB output signal ON and the next keypress resets the function key DDB output to OFF. This feature can be used to enable or disable relay functions. In **Normal** mode the function key DDB signal output goes ON (high) when the key is pressed and OFF when the key is released.				
Fn. Key 2 to 10 Label	Function Key 2 to 10			
Allows the text of the function key to be changed to something more suitable for the application.				

Table 41 - Function keys

5.16 IED Configurator (for IEC 61850 Configuration)

The contents of the IED CONFIGURATOR column are mostly data cells, displayed for information but not editable. To edit the configuration, use the IED Configurator tool in MiCOM S1 Studio.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
IED CONFIGURATOR				
Switch Conf.Bank	No Action	No Action, Switch Banks		
Setting which allows the user to switch between the current configuration, held in the Active Memory Bank, to the configuration sent to and held in the Inactive Memory Bank. The Active Memory Bank is partly displayed below.				
Restore MCL	No Action	No Action, Restore MCL		
Setting which allows the user to restore MCL or no action.				
Active Conf.Name	Data			
The name of the configuration in the Active Memory Bank, usually taken from the SCL file.				
Active Conf.Rev	Data			
Configuration Revision number of the configuration in the Active Memory Bank, usually taken from the SCL file.				
Inact.Conf.Name	Data			

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
IED CONFIGURATOR				
The name of the configuration in the Inactive Memory Bank, usually taken from the SCL file.				
Inact.Conf.Rev	Data			
Configuration Revision number of the configuration in the Inactive Memory Bank, usually taken from the SCL file.				
IP PARAMETERS				
IP Address	0.0.0.0			
Displays the unique network IP address that identifies the relay.				
Subnet Mask	0.0.0.0			
Displays the sub-network the relay is connected to.				
Gateway	0.0.0.0			
Displays the IP address of the gateway (proxy) the relay is connected to, if any.				
SNTP PARAMETERS				
SNTP Server 1	0.0.0.0			
Displays the IP address of the primary SNTP server.				
SNTP Server 2	0.0.0.0			
Displays the IP address of the secondary SNTP server.				
IEC 61850 SCL				
IED Name	Data			
8 character IED name, which is the unique name on the IEC 61850 network for the IED, usually taken from the SCL file.				
IEC 61850 GOOSE				
GoEna	0x00000000	0x00000000	0x11111111	1
Setting to enable GOOSE publisher settings.				
Test Mode	0x00000000	0x00000000	0x11111111	1
The Test Mode cell allows the test pattern to be sent in the GOOSE message, for example for testing or commissioning.				
Ignore Test Flag	No	No, Yes		
When set to **Yes**, the test flag in the subscribed GOOSE message is ignored, and the data treated as normal.				

Table 42 - IED configurator

5.17 User Alarms

Thirty two user alarms are available. Each one can be set as self-reset or manual reset.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
USER ALARMS				
Manual Reset	0x00000000	0x00000000	0x11111111	1
32 bits are used to set the user alarm as self-reset (1) or manual reset (0). The first bit corresponds to user alarm 1 and the last bit to user alarm 32.				
Labels				
Up to 32 user alarms labels are available.				
User Alarm 1	User Alarm 1			
User Alarm 1 label. The maximum label length is 16 characters including spaces.				
User Alarm 32	User Alarm 32			

User Alarm 1 label. The maximum label length is 16 characters including spaces.

Table 43 - User Alarms

5.18 Control Input Labels

Menu text	Default setting	Setting range	Step size
CTRL I/P LABELS			
Control Input 1	Control Input 1	16 Character Text	
Text label to describe each individual control input. This text is displayed when a control input is accessed by the hotkey menu. It is displayed in the programmable scheme logic description of the control input.			
Control Input 2 to 32	Control Input 2 to 32	16 Character Text	
Text label to describe each individual control input. This text is displayed when a control input is accessed by the hotkey menu and it is displayed in the programmable scheme logic description of the control input.			

Table 44 - Control I/P labels

Notes:

OPERATION

CHAPTER NO 5

Date:	12/2013
Hardware Suffix:	J (P642) K (P643/P645)
Software Version:	04
Connection Diagrams:	10P642xx (xx = 1 to 10) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9)

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Notes:

1 SIGNAL PROCESSING

The sampling rate of the P64x is 24 samples per cycle. The raw samples of each channel are buffered in a 2-cycle rotating buffer.

One-cycle Fourier filter is used to extract the fundamental sine and cosine components of each signal channel, and the second and fifth harmonic sine and cosine components of every phase differential current.

Magnitude and phase angle for each channel is calculated, as well as other derived quantities.

The protection functions require a combination of raw samples, Fourier components, magnitudes, phase, and other derived quantities as appropriate. These are specified in the analogue input section of each function.

Data acquisition is performed at a rate of 24 samples per cycle. The frequency tracking runs from the protection scheduler every 3rd sample. The differential protection task runs every 3 samples. The programmable scheme logic and the current differential run at a rate of 8 times per cycle. Table 1 shows the execution rate of other functions:

Function	Execution rate (times/cycle)
CTS, zero crossing detection algorithm used by the CBF function, CT saturation detection, no gap detection, internal/external fault detector.	8
High impedance REF , Low impedance REF, VTS, poledead, circuit breaker failure.	4
Phase overcurrent, negative phase overcurrent, standby overcurrent, under/overvoltage, residual overvoltage, voltage controlled overcurrent, negative sequence overvoltage.	2
CLIO, RTD, overflux, through fault monitoring, thermal overload.	1

Table 1 - Execution rates

The frequency tracking algorithm is used to determine the power system frequency and to adjust the sampling clock so that it will be in exact multiples of the power system frequency. The P64x frequency tracking range is 45 to 66 Hz. The relay will track fundamental frequency down to the following levels of voltage (10V ±5%) and current (50 mA). The frequency tracking channel order is VA, VB, VC, VX, IA1, IB1, IC1, IA2, IB2, IC2, IA3, IB3, IC3, IA4, IB4, IC4, IA5, IB5, IC5. VA, VB, VC are only available in P643/P645 when the three-phase VT option is selected. The voltage channels have the priority. Only if a voltage channel is not available, a current channel would be used. If a current channel is being used and a voltage channel becomes available, the frequency tracking will automatically switch to the voltage channel. However, if neither a voltage channel nor IA1 are on hand, IB1 would be used. If IA1 becomes available and not voltage channel is available, the frequency tracking algorithm will continue using IB1.

2 OPERATION OF INDIVIDUAL PROTECTION FUNCTIONS

2.1 Differential Protection (DIFF)

The P64x is designed for the protection of transformers as well as for the protection of motors and reactors and of other two-winding (P642, P643, P645), three-winding (P643, P645) or five biased inputs (P645) arrangements.

For application of the device as transformer differential protection, ratio correction is required. This is achieved simply by setting of the reference power generally to the nominal power of the transformer and of the primary nominal voltages for all windings of the transformer. To minimize unbalance due to tap changer operation, current inputs to the differential element should be matched for the mid-tap position and not the nominal voltage.

Vector group matching is achieved by input of the relevant vector group identification number. Zero-sequence current filtering is also available. For conditions where it is possible to temporarily load the transformer with a voltage in excess of the nominal voltage, the overfluxing blocking prevents unwanted tripping. The 5th harmonic blocking feature does not require a voltage signal. A 5th harmonic signal is derived from the differential current waveform on each phase and blocking is on a per phase basis. The overfluxing protection should be used in such applications to protect the transformer accordingly.

For applications as a differential protection device for motors, the second harmonic blocking (inrush compensation) can be set to maximum. The start-up of directly switched asynchronous motors represents a problem in differential protection due to transient transformer saturation caused by a displacement of the start-up current for relatively high primary time constants. The P64x uses transient bias to reduce the effects of CT saturation.

2.1.1 Enabling or Disabling Differential Protection

Differential protection can be disabled or enabled from the local control panel. Moreover, enabling can be done separately for each setting group. To enable the differential protection, set the cell [090C: Diff Protection] to **enabled** under the **CONFIGURATION** menu heading. Also the differential function must be enabled in the required setting group, for example, set the cell [3101: Trans Diff] to **enabled** under **GROUP 1 DIFF PROTECTION** menu heading. This enables setting group1 differential protection.

2.1.2 Current Inputs Selection

The current inputs associated to each transformer winding are set in HV CT Terminals, LV CT Terminals and TV CT Terminals.

The current inputs may be assigned as follows:

	P642	P643	P645
HV CT Terminals	01	001 011	00001 00011 00111 01011 01111
LV CT Terminals	10	100 110	10000 11000 11100 11010 11110

	P642	P643	P645
TV CT Terminals		010	00100 01100 00110 01110

Table 2 - Current inputs

The CT inputs are as follows:

- 1 means that the CT input is being used by the xx CT Terminals
- 0 means that the CT input is not being used by the xx CT Terminals

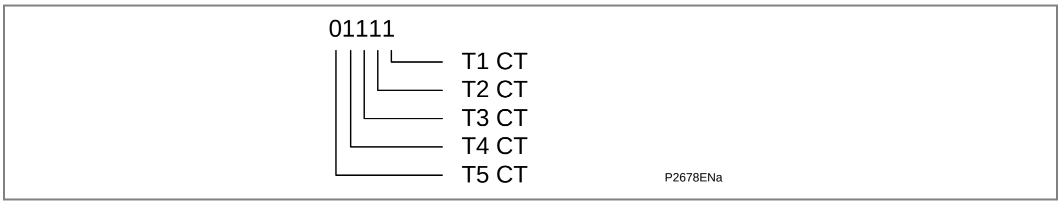

Figure 1 - CT inputs

If any CT is assigned to more than one winding, then a CT selection alarm is issued (DDB 483). When DDB 483 is asserted, the protection is also blocked (see Figure 2).

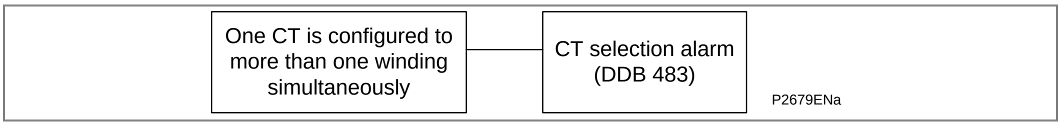
One CT is configured to more than one winding simultaneously
CT selection alarm (DDB 483)
P2679ENa

Figure 2 - CT selection diagram

2.1.3 Ratio Correction

The MiCOM P64x relay automatically calculates the ratio correction factor for each of the current inputs. The matching factors are displayed under **GROUP x SYSTEM CONFIG** menu heading as **Match Factor CT1**, **Match Factor CT2**, **Match Factor CT3**, **Match Factor CT4** and **Match Factor CT5**. The reference power for the protected object, identical for all windings, needs to be defined. For two-winding arrangements, the nominal power will usually be the reference power. For three transformers, the nominal power of the highest-power winding should be set as the reference power. The reference power is set in the cell [3007: Sref] under the **GROUP x SYSTEM CONFIG** menu heading.

The P64x calculates the ratio correction factors on the basis of the reference power, winding nominal voltage, and primary nominal currents of the current transformers.

$$I_{ref,n} = \frac{S_{ref}}{\sqrt{3}V_{nom,n}} \qquad K_{amp,n} = \frac{I_{nom,n}}{\dfrac{S_{ref}}{\sqrt{3}V_{nom,n}}}$$

Sref:	common reference power for all ends
n:	is CT1, CT2, CT3, CT4, CT5 for each of the CT inputs
Iref,n	reference current for the respective CT input
Kamp,n:	amplitude-matching factor for the respective CT input
Inom,n:	primary nominal currents for the respective CT input
Vnom,n:	primary nominal voltage for the respective CT input

The P64x checks that the matching factors are within their permissible ranges. The matching factors must satisfy the following condition:

- The matching factors must always be 0.05 ≤ Kamp,n ≤ 20

The CT para mismatch logic implemented in firmware is shown in Figure 3:

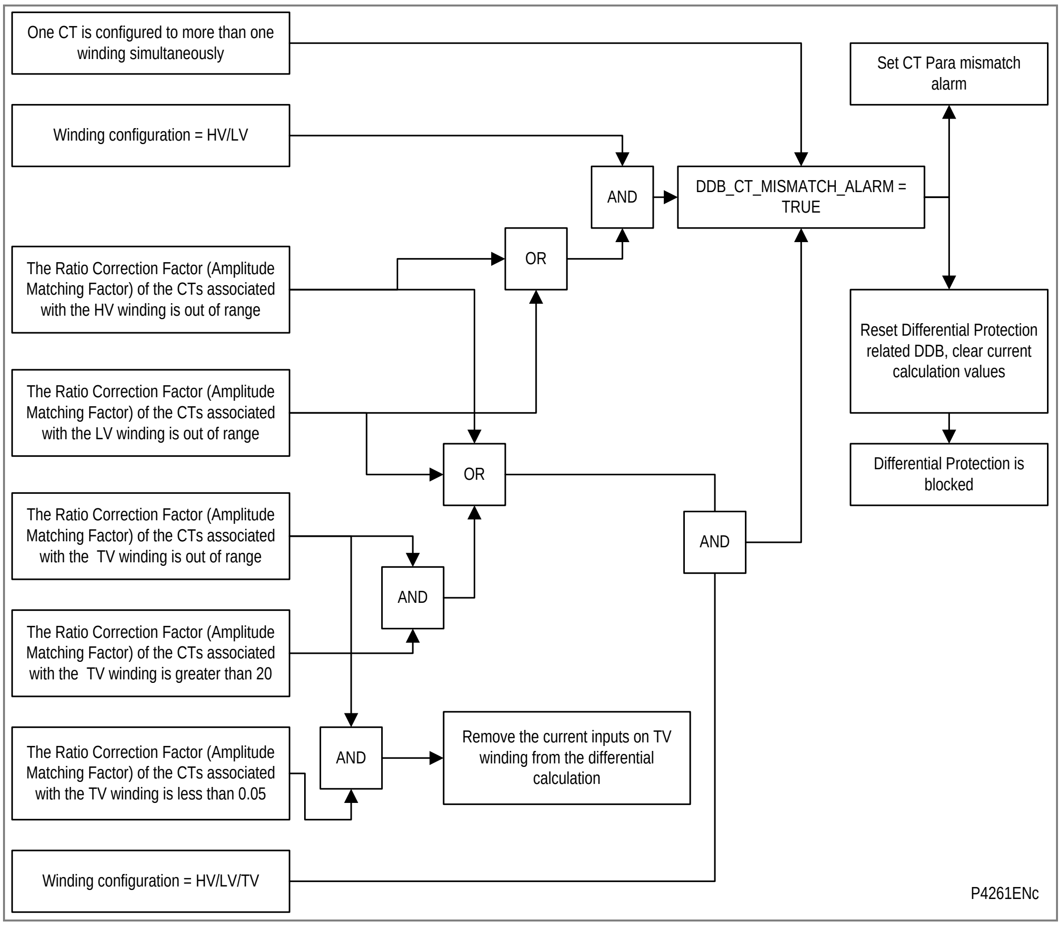
One CT is configured to more than one winding simultaneously
Winding configuration = HV/LV
The Ratio Correction Factor (Amplitude Matching Factor) of the CTs associated with the HV winding is out of range
The Ratio Correction Factor (Amplitude Matching Factor) of the CTs associated with the LV winding is out of range
The Ratio Correction Factor (Amplitude Matching Factor) of the CTs associated with the TV winding is out of range
The Ratio Correction Factor (Amplitude Matching Factor) of the CTs associated with the TV winding is greater than 20
The Ratio Correction Factor (Amplitude Matching Factor) of the CTs associated with the TV winding is less than 0.05
Winding configuration = HV/LV/TV
AND
OR
OR
AND
AND
AND
Remove the current inputs on TV winding from the differential calculation
DDB_CT_MISMATCH_ALARM = TRUE
Set CT Para mismatch alarm
Reset Differential Protection related DDB, clear current calculation values
Differential Protection is blocked
P4261ENc

Figure 3 - CT para mismatch logic diagram (Firmware Version 02C onwards)

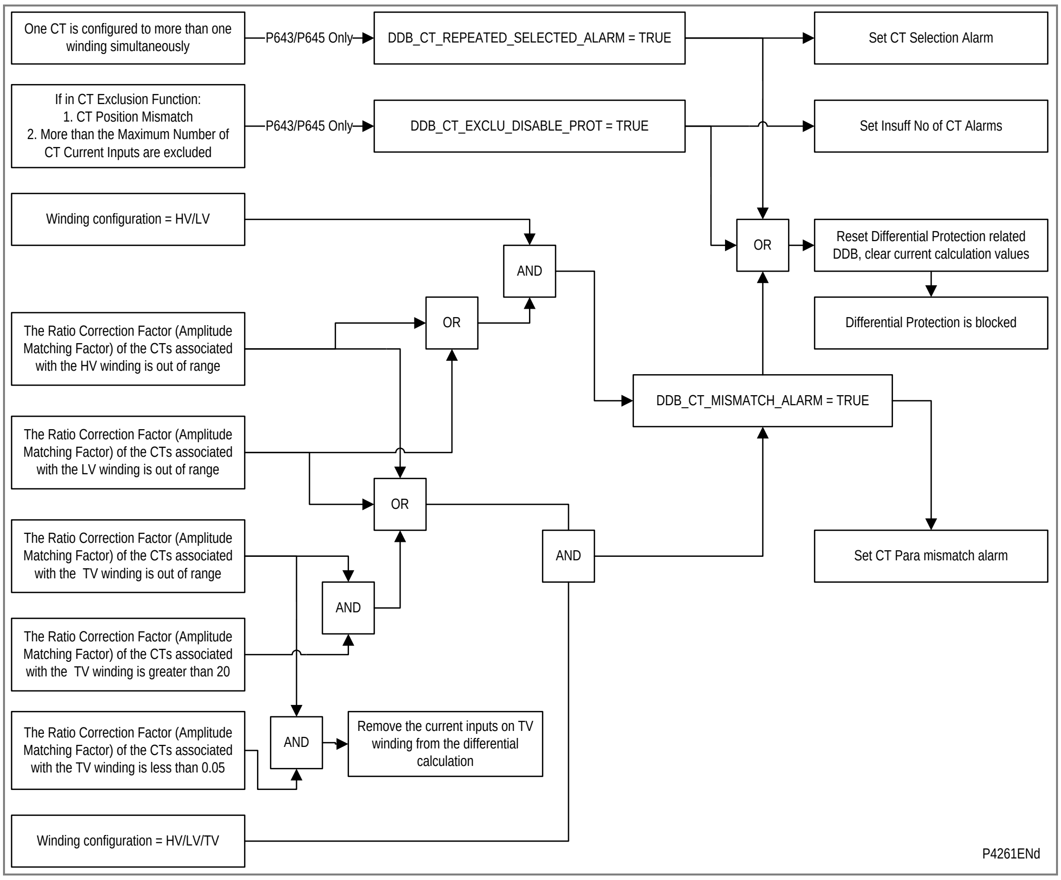
One CT is configured to more than one winding simultaneously
P643/P645 Only
DDB_CT_REPEATED_SELECTED_ALARM = TRUE
Set CT Selection Alarm
If in CT Exclusion Function:
1. CT Position Mismatch
2. More than the Maximum Number of CT Current Inputs are excluded
P643/P645 Only
DDB_CT_EXCLU_DISABLE_PROT = TRUE
Set Insuff No of CT Alarms
Winding configuration = HV/LV
AND
OR
Reset Differential Protection related DDB, clear current calculation values
Differential Protection is blocked
OR
The Ratio Correction Factor (Amplitude Matching Factor) of the CTs associated with the HV winding is out of range
DDB_CT_MISMATCH_ALARM = TRUE
The Ratio Correction Factor (Amplitude Matching Factor) of the CTs associated with the LV winding is out of range
OR
The Ratio Correction Factor (Amplitude Matching Factor) of the CTs associated with the TV winding is out of range
AND
Set CT Para mismatch alarm
AND
The Ratio Correction Factor (Amplitude Matching Factor) of the CTs associated with the TV winding is greater than 20
The Ratio Correction Factor (Amplitude Matching Factor) of the CTs associated with the TV winding is less than 0.05
AND
Remove the current inputs on TV winding from the differential calculation
Winding configuration = HV/LV/TV
P4261ENd

Figure 4 - CT para mismatch logic diagram (Firmware Version 04 onwards)

If any of the ratio correction factors in two winding applications is out of range, the CT para mismatch alarm is asserted. In three winding applications, if the ratio correction factor of the CTs associated to HV or LV windings are out of range or if the ratio correction factor of the CTs associated to TV winding is greater than 20, then the CT para mismatch alarm is asserted. **In some applications, if the ratio correction factor of the CT associated to TV winding is lower than 0.05, it may be preferred to automatically remove this current from the differential calculation. The logic shown in** Figure 3 **allows the relay to do so.**

If the CT para mismatch alarm is asserted the protection is also blocked.

The measured values of the phase currents of the windings of the protected object are multiplied by the relevant matching factors and are then available for further processing. Consequently, all threshold values and measured values always refer back to the relevant reference currents rather than to the transformer nominal currents or the nominal currents of the device.

Caution	**If the CT para mismatch alarm is asserted, the differential protection will be blocked. Other protection functions will still be working.**
Caution	**If the CT Match Factor of any CT (CT1 to CT5) is out of Range, a ‘Ct para mismatch’ alarm will appear on the LED of HMI. Change the corresponding settings to make the CT Match Factor back to valid range the Alarm will disappear automatically. For both of alarm appear or disappear, an alarm event will be recorded!**

Caution	In case that the 'Ct para mismatch' alarm is active, the Differential Protection will be disabled. Any other protection functions are still working.

2.1.4 Vector Group Matching

The transformer HV windings are indicated by capital letters and the LV winding by lower case letters. The numbers refer to positions on a clock face and indicate the phase displacement of balanced 3-phase LV line currents with respect to balanced 3-phase HV line currents. The HV side is taken as reference and it is the 12 o'clock position. Therefore, each hour represents a 30° shift; i.e. 1 represents a 30° lag and 11 represents a 30° lead (LV with respect to HV). An additional N, YNd1, (lower case for LV, d) indicates a neutral to earth connection on the high voltage winding of the power transformer.

By studying the relative phase shifts that can be obtained, it can be seen that star-star windings allow even vector group configurations and star-delta/delta-star windings allow odd group configurations.

Examples

A YNd1 connection indicates a two winding transformer with an earthed, Star-connected, high voltage winding and a Delta-connected low voltage winding. The low voltage balanced line currents lag the high voltage balanced line currents by 30° (−30° phase shift).

A Dyn1yn11 connection indicates a three winding transformer with a Delta-connected high voltage winding and two earthed Star-connected low voltage windings. The phase displacement of the first LV winding with respect to the HV winding is 30° lag (−30° phase shift), the phase displacement of the second LV winding with respect to the HV winding is 30° lead (+30° phase shift).

Vector group matching is performed on the amplitude-matched phase currents of the *low-voltage and tertiary voltage* side in accordance with the characteristic vector group number.

When the P64x is configured to protect a YNd1 transformer, the software interposing CTs used by the relay to achieve vector correction are as shown in Figure 4. No vector correction is performed on the HV amplitude matched phase currents. If the relay is in simple mode, zero sequence filtering is applied when the cell [HV Grounding] under the **GROUP 1 SYSTEM CONFIG** menu heading is set to grounded. If the relay is in advanced mode, the zero sequence filtering is enabled or disabled in the cell [Zero seq filt HV] under the **GROUP 1 DIFF PROTECTION** menu heading. Therefore, on the Y high voltage side of the transformer the software interposing CT is either Yy0 (no zero sequence filtering is required) or Ydy0 (zero sequence filtering is required). The currents on the low voltage side lag by 30° the currents on the high voltage side due to the vector group (1). The relay brings the low voltage current in phase with the high voltage current by using a Yd11 software interposing CT on the low voltage side.

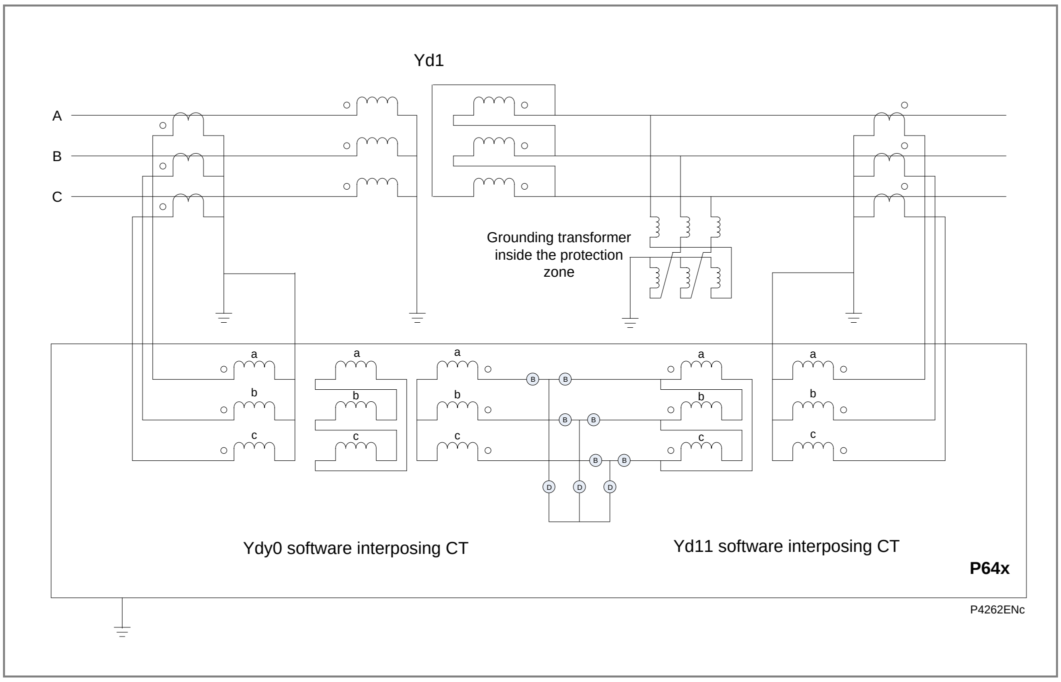
Yd1
A
B
C
Grounding transformer inside the protection zone
a
b
c
Ydy0 software interposing CT
Yd11 software interposing CT
P64x
P4262ENc

Figure 5 - Software interposing CTs for a Yd1 transformer

Consider the Y grounded winding of the YNd1 transformer during external ground faults on the high voltage side. Also consider that a source is connected to the delta side. The zero sequence component of the fault current flows through the grounded neutral that lies inside the transformer differential protection zone. The zero sequence component of the fault current is only seen by the CTs in the HV side. Therefore, zero sequence filtering for a Y grounded winding must be enabled to avoid undesirable tripping when an external ground fault occurs.

The Ydy0 software interposing CT is the equivalent of subtracting the zero sequence component from the phase currents on the high voltage side. The zero-sequence current is determined as follows from the amplitude-matched phase currents:

$$I_{amp,zero,n} = \frac{1}{3}\left(I_{amp,A,n}+I_{amp,B,n}+I_{amp,C,n}\right)$$

$$I_{amp,A,n,filtered}=I_{amp,A,n}-I_{amp,zero,n}$$

n: T1, CT, T2, CT, T3, CT, T4, CT, T5, CT for each of the CT inputs

Iamp,zero,n: zero sequence amplitude matched current for the respective CT input

Iamp,A,n: phase A amplitude matched current of the respective CT input

The grounding transformer connected to the LV side of the power transformer provides a path for LV ground faults. To avoid misoperation during external ground faults the zero sequence component needs to be filtered. In addition, the LV currents need to be in phase with the HV currents. The P64x achieves zero sequence filtering and vector correction by using a Yd11 software interposing CT.

As previously discussed, star-star windings allow even vector group configurations and star-delta/delta-star windings allow odd group configurations. The following tables show that for all odd-numbered vector group characteristics the zero-sequence current on the low-voltage side is basically always filtered out, whereas for even-numbered vector group characteristics the zero-sequence current on the low-voltage side is never filtered out automatically. The latter is also true for the high-voltage side since in that case, as explained above, no vector correction is performed.

Vector group matching and zero-sequence current filtering must always be viewed in combination. Table 3, Table 4 and Table 5 lists the mathematical phasor operations executed by the P64x during vector correction.

The indices in the formulae have these meanings:

am: amplitude-matched
s: amplitude- and vector group-matched
x: phase A, B or C
y: differential measuring system that corresponds to phases A, B or C.
n: T1 CT, T2 CT, T3 CT, T4 CT, T5 CT for each of the CT inputs
x+1: cyclically lagging phase
x-1: cyclically leading phase

No vector correction is done on the HV side of the transformer. Only zero sequence filtering is carried on if in the simple mode the winding is set as grounded or if in the advanced mode the high voltage zero sequence filter is enabled. As a result, the relay may perform the following mathematical operations on the HV side:

	With $\underline{I}_{zero}$ filtering	**Without $\underline{I}_{zero}$ filtering**
0	$I_{vec,y,n} = I_{amp,x,n} - I_{amp,zero,n}$	$I_{vec,y,n} = I_{amp,x,n}$

Table 3 - Mathematical phasor operations on the HV side

Figure 5 and Figure 6 shows various even-numbered vector group configurations:

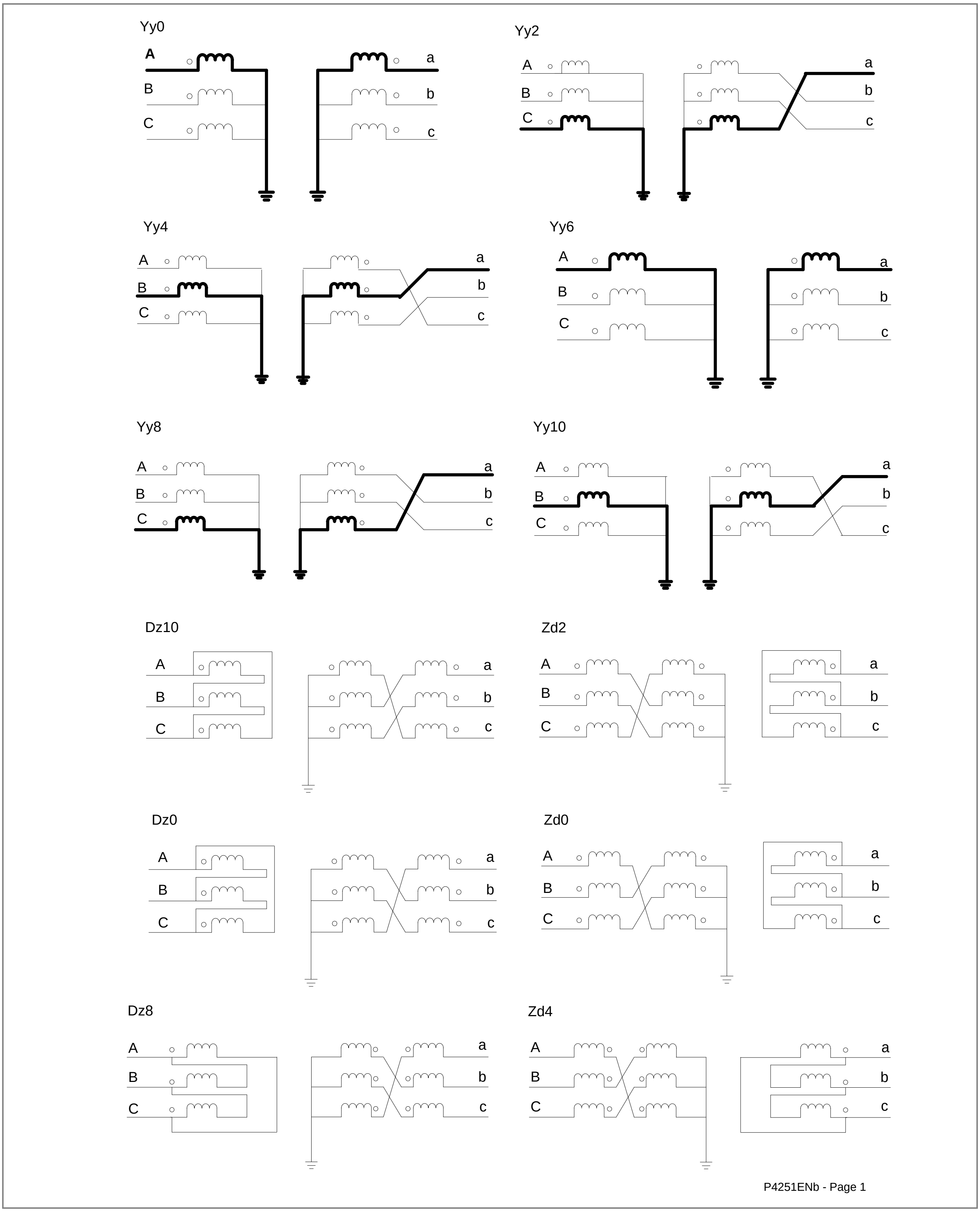
Yy0
A
B
C
a
b
c
Yy2
A
B
C
a
b
c
Yy4
A
B
C
a
b
c
Yy6
A
B
C
a
b
c
Yy8
A
B
C
a
b
c
Yy10
A
B
C
a
b
c
Dz10
A
B
C
a
b
c
Zd2
A
B
C
a
b
c
Dz0
A
B
C
a
b
c
Zd0
A
B
C
a
b
c
Dz8
A
B
C
a
b
c
Zd4
A
B
C
a
b
c
P4251ENb - Page 1

Figure 6 - Even-numbered vector groups - Page 1

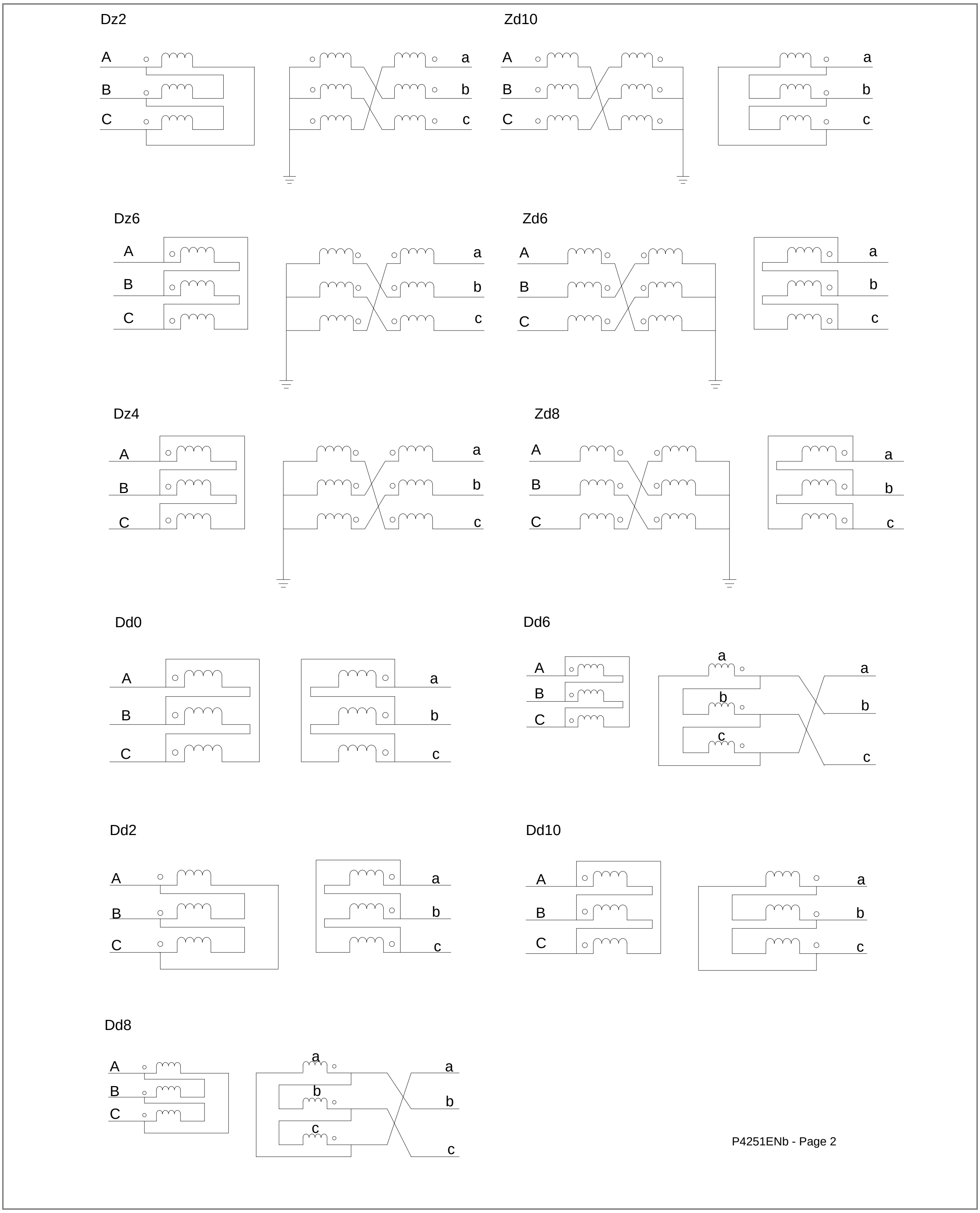
Dz2
Zd10
Dz6
Zd6
Dz4
Zd8
Dd0
Dd6
Dd2
Dd10
Dd8
A
B
C
a
b
c
P4251ENb - Page 2

Figure 7 - Even-numbered vector groups - Page 2

Considering the configurations shown in Figure 6.

- In a Yy0, Dd0, Dz0 or Zd0 power transformer configuration, the LV currents are already in phase with the HV currents. Therefore, the relay only filters the zero sequence current as required.
- In a Yy2, Dd2, Dz2 or Zd2 power transformer configuration, the LV currents lag the HV currents by 60°. To bring the LV currents in phase with the HV currents, the P64x uses a Yy10 software interposing CT.
- In a Yy4, Zd4 or Dz4 power transformer configuration, the LV currents lag the HV currents by 120°. To bring the LV currents in phase with the HV currents, the P64x uses a Yy8 software interposing CT.
- In a Yy6, Dz6, Zd6 or Dd6 power transformer configuration, the LV currents lag the HV currents by 180°. To bring the LV currents in phase with the HV currents, the P64x uses a Yy6 software interposing CT.
- In a Yy8, Dz8, Zd8 or Dd8 power transformer configuration, the LV currents lead the HV currents by 120°. To bring the LV currents in phase with the HV currents, the P64x uses a Yy4 software interposing CT.
- In a Yy10, Dz10, Zd10 or Dd10 power transformer configuration, the LV currents lead the HV currents by 60°. To bring the LV currents in phase with the HV currents, the P64x uses a Yy2 software interposing CT.

Table 4 shows the mathematical operations, equivalent to the corresponding software interposing CT, on the low-voltage side for an even-numbered vector group characteristic.

VG	With $\underline{I}_{zero}$ filtering	Without $\underline{I}_{zero}$ filtering
0	$I_{vec,y,n} = I_{amp,x,n} - I_{amp,zero,n}$	$I_{vec,y,n} = I_{amp,x,n}$
2	$I_{vec,y,n} = -\left(I_{amp,x+1,n} - I_{amp,zero,n}\right)$	$I_{vec,y,n} = -I_{amp,x+1,n}$
4	$I_{vec,y,n} = I_{amp,x-1,n} - I_{amp,zero,n}$	$I_{vec,y,n} = I_{amp,x-1,n}$
6	$I_{vec,y,n} = -\left(I_{amp,x,n} - I_{amp,zero,n}\right)$	$I_{vec,y,n} = -I_{amp,x,n}$
8	$I_{vec,y,n} = I_{amp,x+1,n} - I_{amp,zero,n}$	$I_{vec,y,n} = I_{amp,x+1,n}$
10	$I_{vec,y,n} = -\left(I_{amp,x-1,n} - I_{amp,zero,n}\right)$	$I_{vec,y,n} = -I_{amp,x-1,n}$

Table 4 - Phasor operations on LV side of an even-numbered vector group

Figure 7 shows the software interposing CTs used by the P64x when a YNyn0 power transformer is being protected. Notice that zero sequence filter is enabled on the HV and LV sides since Ydy0 interposing CTs are being used.

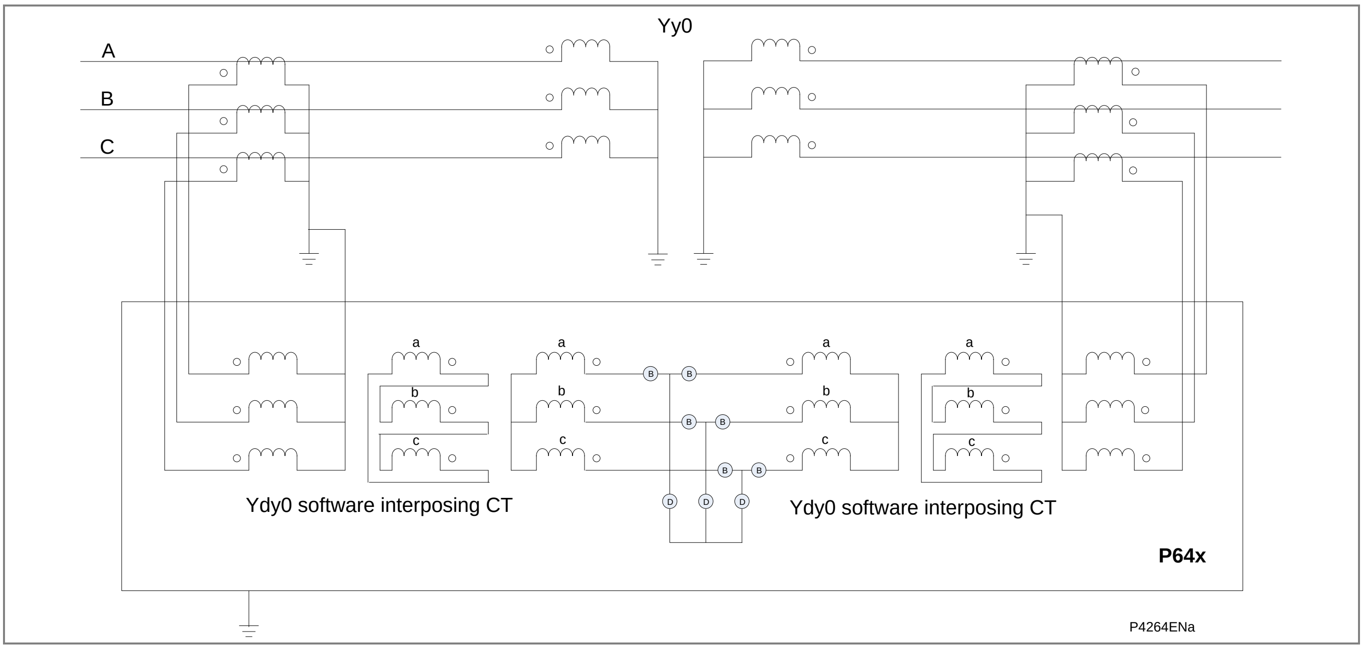
Yy0
A
B
C
a
b
c
B
D
Ydy0 software interposing CT
Ydy0 software interposing CT
P64x
P4264ENa

Figure 8 - Software interposing CTs for a YNyn0 transformer

Figure 8 and Figure 9 shows the various odd-numbered vector group configurations:

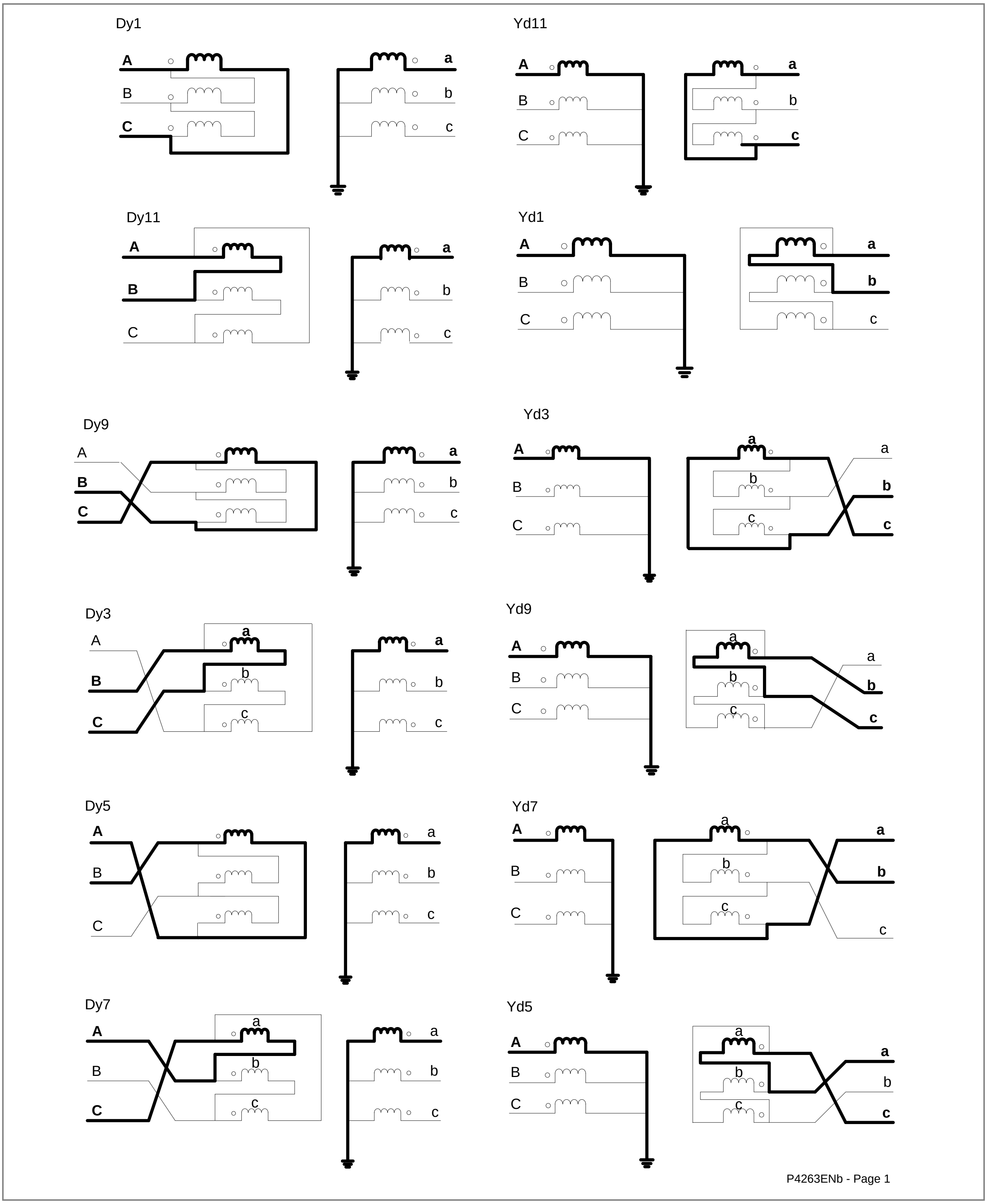
Dy1
Yd11
Dy11
Yd1
Dy9
Yd3
Dy3
Yd9
Dy5
Yd7
Dy7
Yd5
A
B
C
a
b
c
P4263ENb - Page 1

Figure 9 - Odd-numbered vector group connections - Page 1

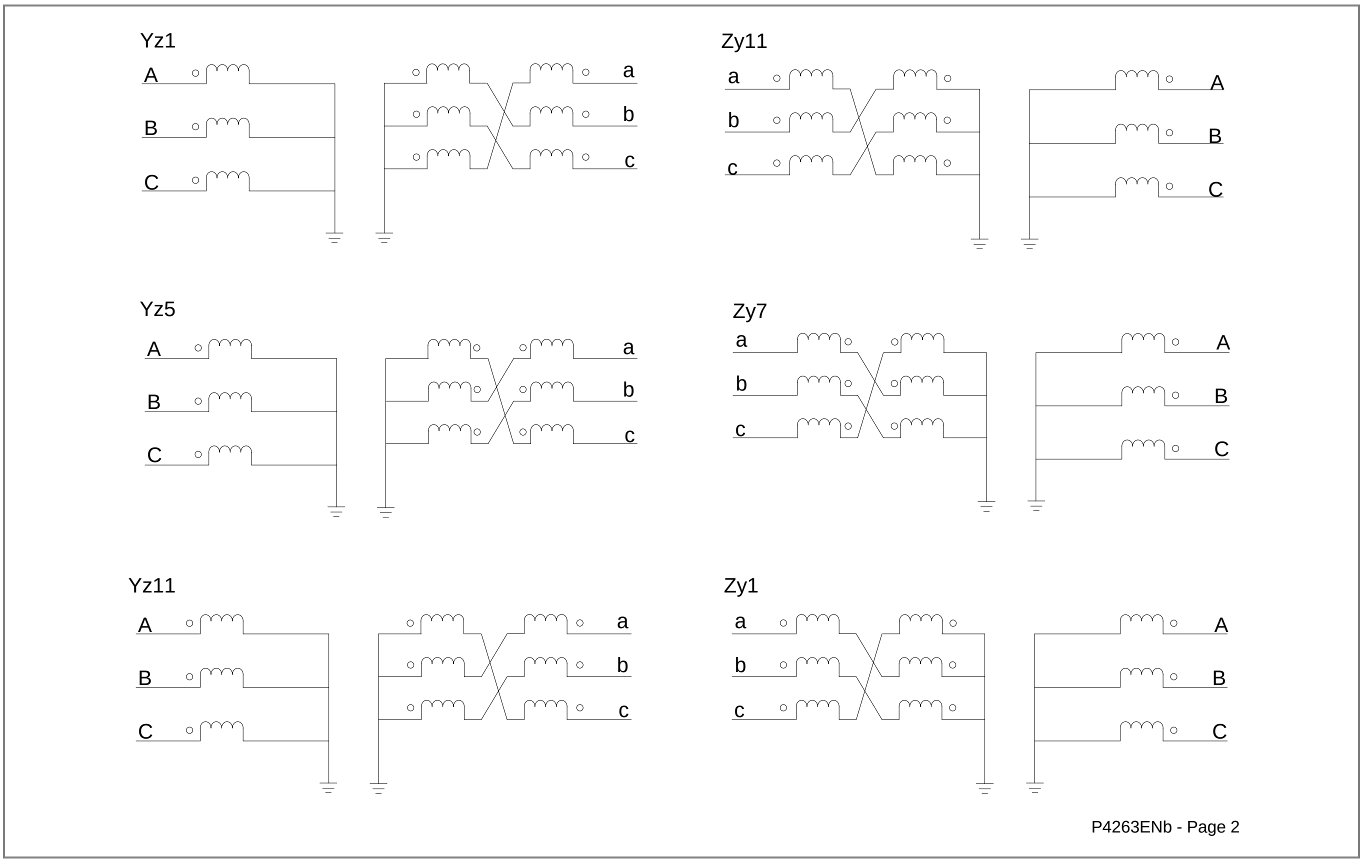

Figure 10 - Odd-numbered vector group connections - Page 2

Considering the configurations shown in Figure 9:

- In a Dy1, Yd1, Yz1 or Zy1 power transformer configuration, the LV currents lag the HV currents by 30°. The P64x uses a Yd11 software interposing CT to bring the LV currents in phase with the HV currents.
- In a Dy3 or Yd3 power transformer configuration, the LV currents lag the HV currents by 90°. The P64x uses a Yd9 software interposing CT to bring the LV currents in phase with the HV currents.
- In a Dy5, Yd5 or Yz5 power transformer configuration, the LV currents lag the HV currents by 150°. The P64x uses a Yd7 software interposing CT to bring the LV currents in phase with the HV currents.
- In a Dy7, Yd7 or Zy7 power transformer configuration, the LV currents lead the HV currents by 150°. The P64x uses a Yd5 software interposing CT to bring the LV currents in phase with the HV currents.
- In a Dy9 or Yd9 power transformer configuration, the LV currents lead the HV currents by 90°. The P64x uses a Yd3 software interposing CT to bring the LV currents in phase with the HV currents.
- In a Dy11, Yd11, Yz11 or Zy11 power transformer configuration, the LV currents lead the HV currents by 30°. The P64x uses a Yd1 software interposing CT to bring the LV currents in phase with the HV currents.

Table 5 shows the mathematical operations, equivalent to the corresponding software interposing CT, on the low-voltage side for an odd-numbered vector group characteristic:

VG	With or without I_{zero} filtering
1	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x,n} - I_{amp,x+1,n}\right)$
3	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x-1,n} - I_{amp,x+1,n}\right)$
5	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x-1,n} - I_{amp,x,n}\right)$
7	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x+1,n} - I_{amp,x,n}\right)$
9	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x+1,n} - I_{amp,x-1,n}\right)$
11	$I_{vec,y,n} = \frac{1}{\sqrt{3}} \cdot \left(I_{amp,x,n} - I_{amp,x-1,n}\right)$

Table 5 - Phasor operations on LV side of an odd-numbered vector group

Vector group matching is by input of the vector group identification number provided that the phase currents of the high and low voltage side(s) are connected in standard configuration. For other configurations, special considerations may apply. A reverse phase rotation (phase sequence A-C-B) needs to be taken into account by making the appropriate setting at the P64x. The P64x will then automatically form the complementary value of the set vector group ID to the number 12 (vector group ID = 12 - set ID).

2.1.5 Tripping Characteristics

The differential and bias currents for each phase are calculated from the current variables after amplitude and vector group matching.

Calculation of differential and biased currents is as follows:

$$I_{diff,y} = \left|\overrightarrow{I_{s,y,CT1}} + \overrightarrow{I_{s,y,CT2}} + \overrightarrow{I_{s,y,CT3}} + \overrightarrow{I_{s,y,CT4}} + \overrightarrow{I_{s,y,CT5}}\right|$$

$$I_{bias,y} = 0.5 \cdot \left[\left|\overrightarrow{I_{s,y,CT1}}\right| + \left|\overrightarrow{I_{s,y,CT2}}\right| + \left|\overrightarrow{I_{s,y,CT3}}\right| + \left|\overrightarrow{I_{s,y,CT4}}\right| + \left|\overrightarrow{I_{s,y,CT5}}\right|\right]$$

y is the measuring system that corresponds to phases A, B or C.
s is the current after the amplitude and vector group are matched.

To provide further stability for external faults, additional measures are considered on the calculation of the bias current:

2.1.5.1 Delayed Bias

The bias quantity is the maximum of the mean bias quantities calculated within the last cycle. The mean bias is the fundamental bias current. This is to maintain the bias level, therefore stability is provided when an external fault is cleared. This feature is implemented on a per-phase basis. The algorithm is expressed as follows; the function is executed 8 times per cycle:

$I_{bias\ A\_delayed}$ = Maximum [$I_{bias,\ A}$(n), $I_{bias,A}$ (n-1), ..., $I_{bias,A}$ (n - (k-1))]

$I_{bias\ B\_delayed}$ = Maximum [$I_{bias,\ B}$(n), $I_{bias,B}$ (n-1), ..., $I_{bias,B}$ (n - (k-1))]

$I_{bias\ C\_delayed}$ = Maximum [$I_{bias,\ C}$(n), $I_{bias,C}$ (n-1), ..., $I_{bias,C}$ (n - (k-1))]

2.1.5.2 Maximum Bias

The maximum delayed bias current calculated from all three phases is the maximum bias:

$I_{bias,max}$ = Maximum [$I_{biasA\_delayed}$, $I_{bias,B\_delayed}$, $I_{bias,C\_delayed}$]

The maximum bias is used to calculate the differential operating current. The differential operating current is calculated using the following characteristic equations:

Characteristic equation for the range: $0 \le I_{bias\,max} \le \frac{I_{s1}}{K_1}$

$$Iop = I_{s1}$$

Characteristic equation for the range: $\frac{I_{s1}}{K_1} \le I_{bias\,max} \le I_{s2}$

$$Iop = K_1 \cdot I_{bias\,max}$$

Characteristic equation for the range: $I_{bias\,max} \ge I_{s2}$

$$Iop = K_1 \cdot I_{s2} + K_2 \left(I_{bias\,max} - I_{s2} \right)$$

K_1: gradient of characteristic in range $\frac{I_{s1}}{K_1} \le I_{bias\,max} \le I_{s2}$

K_2: gradient of characteristic in range $I_{bias\,max} \ge I_{s2}$

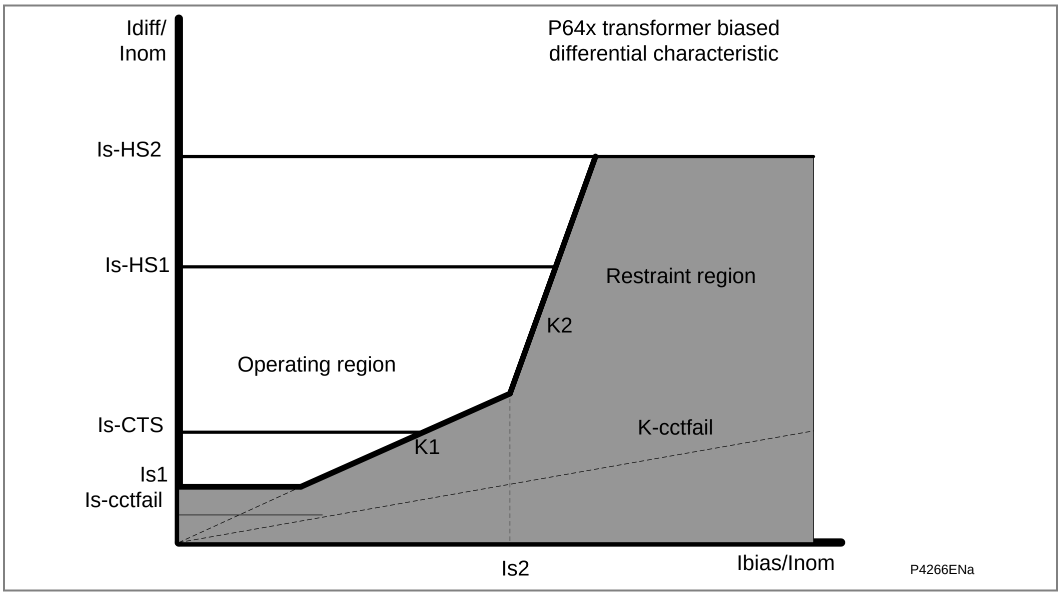

Figure 11 - Tripping characteristic of differential protection

The tripping characteristic of the differential protection device P64x has two knees. The first knee is dependent on the settings of I_{s1} and K1. The second knee of the tripping characteristic is defined by the setting I_{s2}. The lower slope provides sensitivity for internal faults. The higher slope provides stability under through fault conditions, since transient differential currents may be present due to current transformer saturation.

2.1.5.3 Transient Bias

If there is a sudden increase in the mean-bias measurement, an additional bias quantity is introduced in the bias calculation, on a per-phase basis. This quantity, named transient bias, decays exponentially. The transient bias resets to zero once the relay trips, or if the mean bias quantity is below the Is1 setting. The mean bias is the fundamental of the bias current. As explained in section 2.1.5.2 the relay calculates the operating current at the maximum bias current. The transient bias is calculated on a per phase basis and it is added to the operating current calculated at the maximum bias. Therefore, these differential current thresholds are available:

Differential threshold phase A = Iop at max bias + transient bias_phase A

Differential threshold phase B = Iop at max bias + transient bias_phase B

Differential threshold phase C = Iop at max bias + transient bias_phase C

The fundamental of the differential current is compared against the differential current threshold given above on a per phase basis. The relay calculates the differential current on a sample basis using the following equation:

$$I_{diff,y} = \left| \overrightarrow{I_{s,y,T1CT}} + \overrightarrow{I_{s,y,T2CT}} + \overrightarrow{I_{s,y,T3CT}} + \overrightarrow{I_{s,y,T4CT}} + \overrightarrow{I_{s,y,T5CT}} \right|$$

The relay calculates the fundamental of the differential current using a Fourier filter.

If the fundamental of the differential current is above the threshold, then the low set differential element might trip as long as there is no second harmonic or fifth harmonic blocking.

The transient bias technique considers a time decay constant, stability coefficients and the differential function settings to provide a dynamic bias characteristic. Figure 11 shows the relay behavior during an external fault. The transient bias enhances relay stability. For the relay to trip, the fundamental of the differential current should be above the operating current at max bias + transient bias.

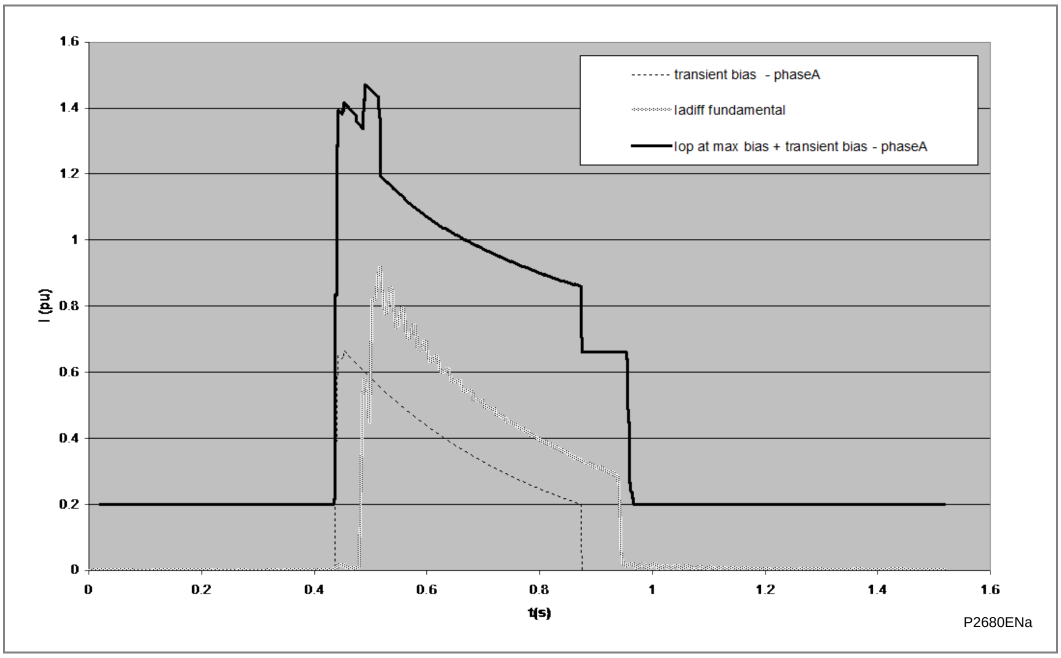

Figure 12 - Transient bias characteristic

The transient bias enhances the stability of the differential element during external faults and allows for the time delay in CT saturation caused by small external fault currents and high X/R ratios. For internal single-end or double-end fed faults the differential current is dominant and the transient bias has no effect.

The transient bias is removed after the relay has tripped to avoid the possibility of chattering. It is also removed when Ibias is less than Is1 to avoid the possibility of residual values due to the numerical effects.

No transient bias is produced under load switching conditions. Also, no transient bias is generated when the CT comes out of saturation.

2.1.6 High-Set Differential Protection Function

The high set 1 algorithm uses a peak detection method to achieve fast operating times. The peak value is the largest absolute value in the latest 24 samples (latest cycle). Since the high set 1 algorithm uses a peak detection method, Is-HS1 is set above the expected highest magnetizing inrush peak to maintain immunity to magnetizing inrush conditions. To declare high set 1 trip, two conditions must be fulfilled:

- The peak value of the differential current is greater than Is-HS1 setting.
- The bias characteristic is in the operating region.

Above the adjustable threshold Is-HS1 of the differential current, the P64x will trip without taking into account either the second harmonic blocking or the overfluxing blocking, but the bias current is considered. The high set 1 resets when the differential and bias currents are in the restraint area (gray area in Figure 10).

The high set 2 algorithm uses Fourier quantities. If the differential current exceeds the adjustable threshold Is-HS2, the bias current, the second harmonic and overfluxing restraints are no longer taken into account. As a result, the P64x issues a high set 2 trip regardless of the harmonic blocking or biased current. The high set 2 element resets when the differential current drops below 0.95*Is-HS2.

2.1.7 Low-Set Differential Protection Function

Transient bias is added for through fault stability. The transient bias is on a per-phase basis and is not affected by K1 or K2 settings.

Once the differential and bias currents are calculated, the following comparisons are made and an operate/restrained signal is obtained:

Flat slope: $0 \le I_{bias} \le \frac{I_{s1}}{K1}$

$$I_{diff} \ge I_{s1} + \text{Transient Bias}$$

K1 slope: $\frac{I_{s1}}{K_1} \le I_{bias} \le I_{s2}$

$$I_{diff} \ge K1 \cdot I_{bias\,max} + \text{Transient Bias}$$

K2 slope: $I_{bias} \ge I_{s2}$

$$I_{diff} \ge K_1 \cdot I_{s2} + K_2\left(I_{bias\,max} - I_{s2}\right) + \text{Transient Bias}$$

A count strategy is used so that the protection operates slower near the boundary of operation. This approach is used to stabilize the relay under some marginal transient conditions. The protection trips on a count of 2, which is approximately 5 ms after fault detection. The count is increased to 4 if the differential current is within 0.5*Is1 of the threshold.

2.1.8 Magnetizing Inrush Current Blocking

The phenomenon of magnetizing inrush is a transient condition which occurs primarily when a transformer is energized. It is not a fault condition, and therefore does not require the operation of the protection, which, on the contrary must remain stable during the inrush transient.

Magnetizing inrush happens under these conditions:

- Initial
- Recover
- Sympathetic

2.1.8.1 Initial Magnetization Inrush

The initial magnetizing inrush may occur when energizing the transformer after a prior period of de-energization. This has the potential of producing the maximum magnetizing inrush.

Figure 12 portrays a transformer magnetizing characteristic. To minimize material costs, weight and size, transformers are generally operated near to the knee point of the magnetizing characteristic. Consequently, only a small increase in core flux above normal operating levels will result in a high magnetizing current.

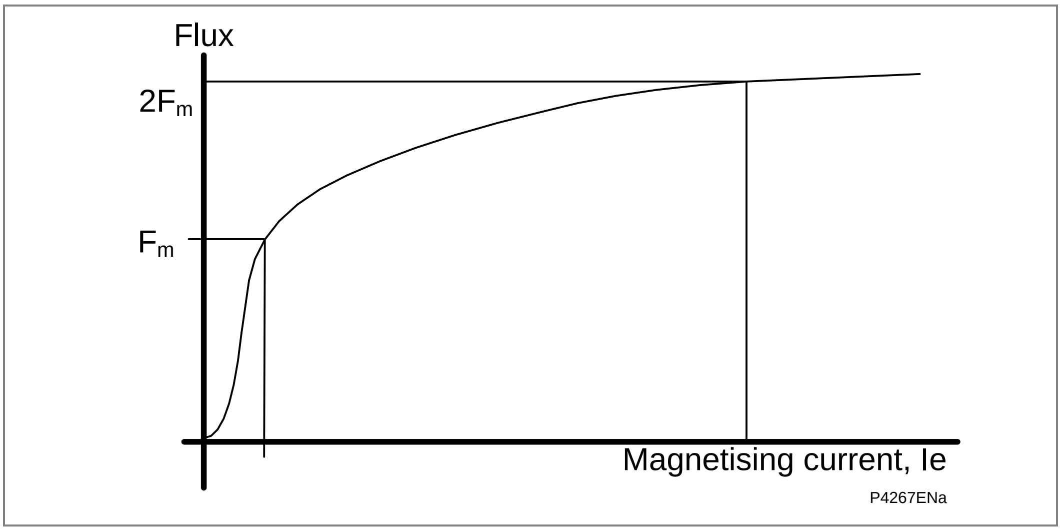

Figure 13 - Transformer magnetizing characteristic

Under normal steady state conditions, the magnetizing current associated with the operating flux level is relatively small (2-5% of full load current). However, if a transformer winding is energized at a voltage zero, with no remnant flux, the flux level during the first voltage cycle (2 x normal max flux) will result in core saturation and in a high, non-sinusoidal magnetizing current waveform. This current is commonly referred to as magnetizing inrush current and may persist for several cycles. The maximum initial-magnetizing current may be as high as 8-30 times the full-load current. Resistance in the supply circuit and transformer and the stray losses in the transformer reduce the peaks of the inrush current such that it decays to the normal exciting current value. The time constant varies from 10 cycles to as long as 1 minute in very high inductive circuits. Figure 13 shows the magnetizing inrush phenomenon.

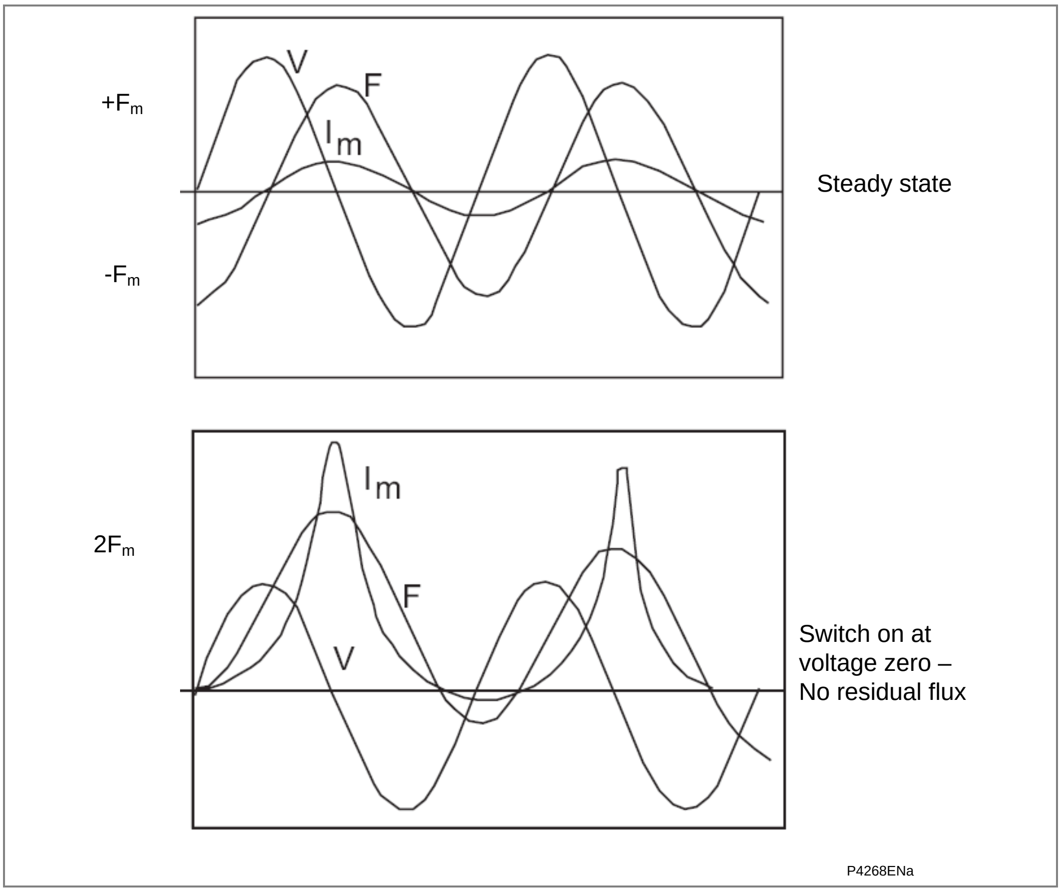

Figure 14 - Magnetizing inrush phenomenon

The magnitude and duration of magnetizing inrush current waveforms are dependant upon a number of factors such as transformer design, size, system fault level, point on wave of switching, number of banked transformers etc.

Some inrush will always occur in one or two phases and generally all three phases in a three phase circuit. Figure 14 indicates typical magnetizing inrush wave forms as seen by the differential protection.

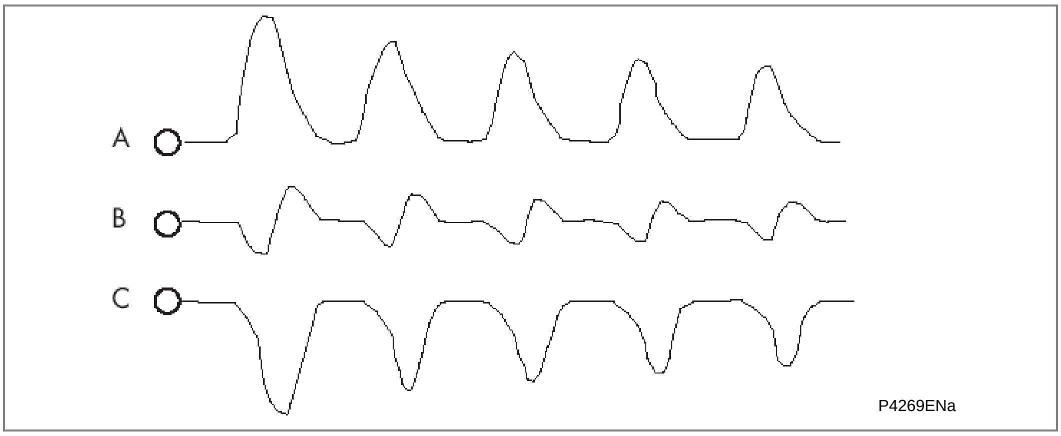

Figure 15 - Magnetizing inrush current waveforms

2.1.8.2 Recovery Magnetizing Inrush

As stated in IEEE Std. C37.91-2000, magnetizing inrush can be caused by any abrupt change of magnetizing voltage. These include the occurrence of a fault, the removal of the fault, change of character of a fault (a single phase fault evolving to two phase fault). The recovery inrush is when the voltage returns back to normal. The worst case of recovery inrush occurs after a solid three phase external fault near a transformer bank is removed and the voltage gets back to normal.

2.1.8.3 Sympathetic Magnetizing Inrush

According to IEEE Std. C37.91-2000, a severe magnetizing inrush may occur when energizing a transformer at a station at which at least one other transformer is already energized. This inrush will involve transformers that are already energized as well as transformers being energized. This inrush transient may be particularly long in duration. The inrush into the transformer being energized occurs during the opposite half-cycle to that of the already energized transformer. Therefore the net inrush into all transformers may approximate a sine wave of fundamental frequency, and therefore not operate the second harmonic blocking unit of the differential relay if it is protecting both parallel transformers.

As described above, when an unloaded transformer is energized, the inrush current at unfavorable points on wave such as for voltage zero may have values that exceed the transformer nominal current several times over. Since the high inrush current flows on the connected side only, the tripping characteristic of differential protection may give rise to a trip unless stabilizing action is taken. The fact that the inrush current has a high proportion of second harmonics offers a possibility of stabilization against tripping by the inrush current.

The P64x filters the differential current. The fundamental I_{diff}(fn) and second harmonic components I_{diff}(2*fn) of the differential current are determined. Second harmonic blocking is phase segregated. If the ratio I_{diff}(2*fn)/I_{diff}(fn) exceeds a specific adjustable value in at least one phase in two consecutive calculations, tripping is blocked optionally in one of these modes:

- Across all three phases
- Selectively for one phase

There will be no blocking if the differential current exceeds the set thresholds Is-HS1 or Is-HS2.

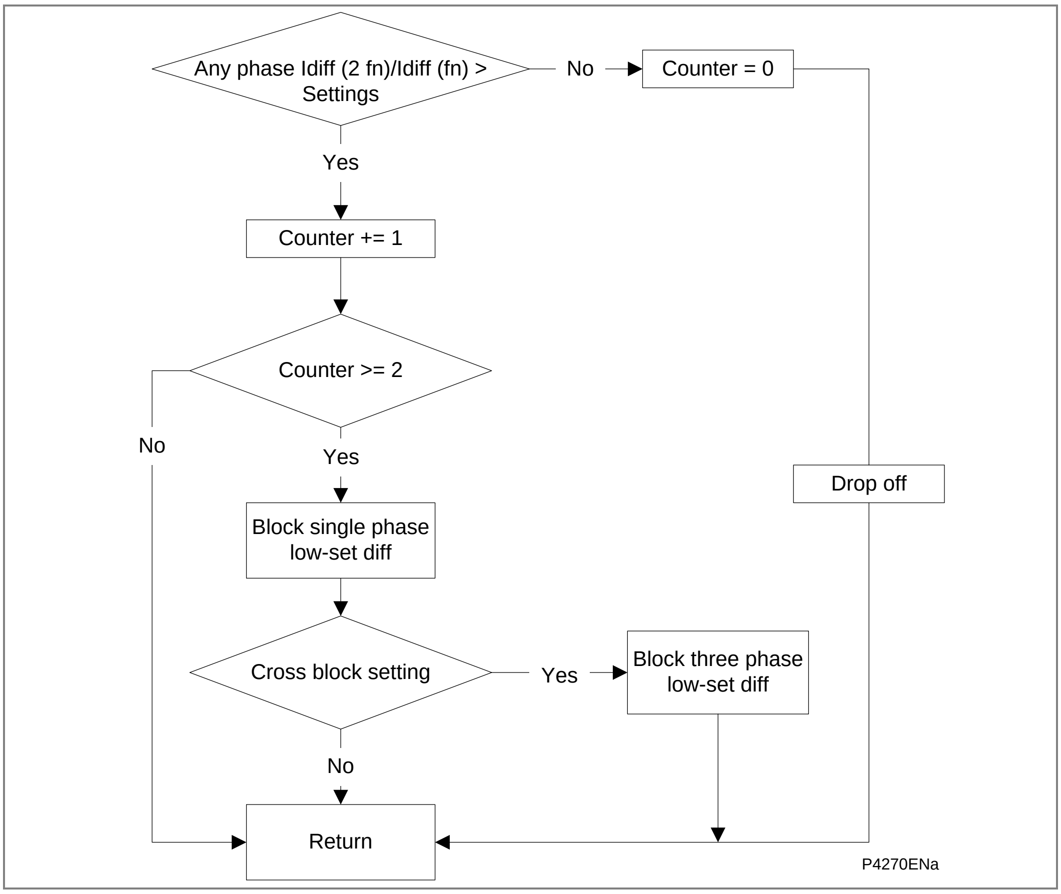
Any phase Idiff (2 fn)/Idiff (fn) > Settings
No
Counter = 0
Yes
Counter += 1
Counter >= 2
No
Yes
Drop off
Block single phase low-set diff
Cross block setting
Yes
Block three phase low-set diff
No
Return
P4270ENa

Figure 16 - Inrush stabilization (second harmonic blocking)

2.1.9 CT Saturation Detection (Patent Pending)

A patented CT saturation detection technique has been implemented in the P64x relay. This technique unblocks the low set differential element during internal faults with heavy CT saturation. During CT saturation the content of second harmonic may be high enough so that the second harmonic blocking element would be asserted thus blocking the low set differential element. As a result, the operation of the low set differential element is delayed. The CT saturation detection logic unblocks the low set differential element during CT saturation. During magnetizing inrush conditions, the ratio of second harmonic to fundamental is used to stabilize the relay. The CT saturation detection technique distinguishes between magnetizing inrush and saturation; therefore, the relay stability is maintained during inrush conditions.

To detect a CT saturation condition the differential current samples on a per phase basis are considered. The relay analyzes the differential current waveforms considering their derivatives, dynamic and fixed thresholds that were determined by Real Time Digital Simulator (RTDS) tests.

2.1.10 No Gap Detection Technique (Patent Pending)

The no gap detection technique detects light CT saturation on a per phase basis. During CT saturation the content of second harmonic may be high enough so that the second harmonic blocking element is asserted thus blocking the low set differential element. As a result, the operation of the low set differential element is delayed. The no gap detection technique unblocks the low set differential element during light CT saturation allowing the low set differential element to trip faster. Stability during inrush conditions is maintained, as this technique distinguishes between an inrush and a saturated waveform.

The no gap detection technique considers two dynamic thresholds. One is related to the gap region and the other to the wave width region of the differential current waveform. The derivatives of the differential current on a per phase basis are considered as well. To assert the no gap detection algorithm the following two conditions must be fulfilled:

- The number of continuous samples within a cycle above the dynamic gap threshold is below a fixed threshold.
- The number of continuous samples within a cycle above the dynamic wave width threshold is above a fixed threshold.

2.1.11 External Fault Detection Technique (Patent Pending)

An external fault detection technique has been implemented so that the CT saturation and No gap detection techniques do not affect the second harmonic blocking during an external fault.

The external fault detection technique considers the time to saturation, a delta bias start signal, a delta differential start signal and the ratio of delta differential to delta bias at the time of start. As soon as an external fault occurs, the bias current changes, but the differential current only increases after the time to saturation as shown in Figure 16. The external fault detection algorithm is asserted if the following conditions are fulfilled:

- The delta bias start signal is asserted first. The delta bias start signal and the delta differential start signal are asserted if the delta bias and delta differential currents are greater than 0.65Is1 respectively.
- The time difference between the assertion of the delta bias start signal and the assertion of the delta differential signal is greater than the time to saturation. The time to saturation in a 50Hz system is 2.5ms and it is 2.08ms in a 60Hz system.
- The ratio of delta differential to delta bias is smaller than a fixed threshold when the delta bias start signal is asserted.

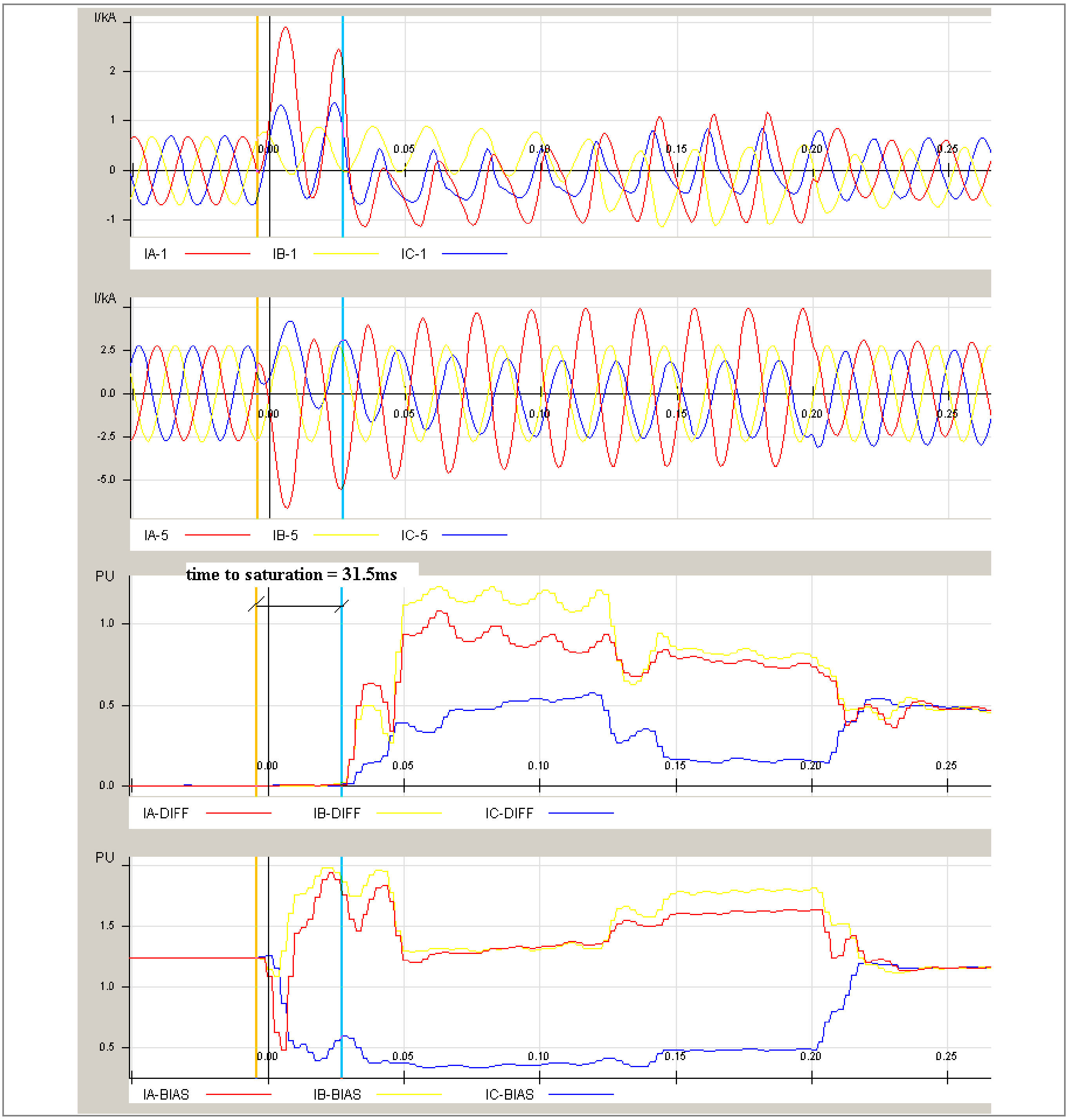

Figure 17 - Time to saturation - External AN fault

The external fault detection algorithm is on a per phase basis. If an external fault is detected on phase A, B or C, signals Ext Flt Phase A (DDB 839), Ext Flt Phase B (DDB 840) or Ext Flt Phase C (DDB 841) are asserted.

2.1.12 Differential Biased Trip Logic

The differential biased trip is affected by the CT saturation technique and by the no gap detection technique. If the second harmonic blocking is asserted and either the CT saturation detection or no gap detection technique is asserted, then the biased differential trip is unblocked. A biased differential trip will occur if the fifth harmonic blocking is not asserted and the bias differential start signal is asserted. The differential biased trip logic is described in Figure 17.

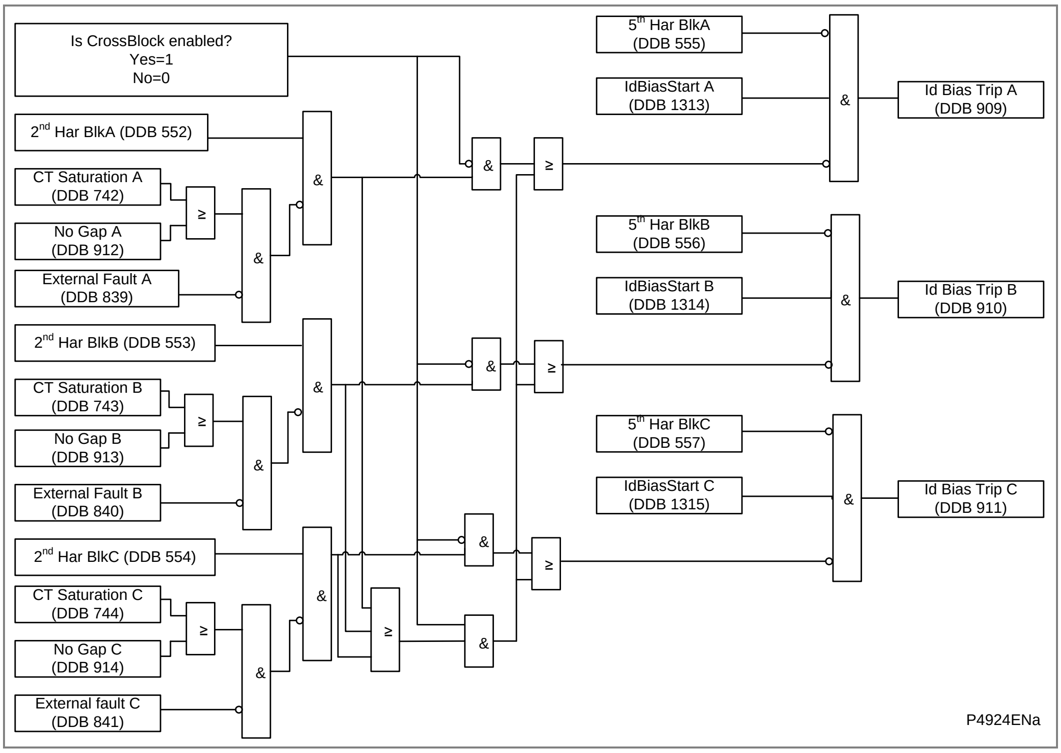
Is CrossBlock enabled?
Yes=1
No=0
2nd Har BlkA (DDB 552)
CT Saturation A (DDB 742)
No Gap A (DDB 912)
External Fault A (DDB 839)
2nd Har BlkB (DDB 553)
CT Saturation B (DDB 743)
No Gap B (DDB 913)
External Fault B (DDB 840)
2nd Har BlkC (DDB 554)
CT Saturation C (DDB 744)
No Gap C (DDB 914)
External fault C (DDB 841)
5th Har BlkA (DDB 555)
IdBiasStart A (DDB 1313)
Id Bias Trip A (DDB 909)
5th Har BlkB (DDB 556)
IdBiasStart B (DDB 1314)
Id Bias Trip B (DDB 910)
5th Har BlkC (DDB 557)
IdBiasStart C (DDB 1315)
Id Bias Trip C (DDB 911)
&
≥
P4924ENa

Figure 18 - Differential biased trip logic

2.1.13 Overfluxing Restraint

If the transformer is loaded with a voltage in excess of the nominal voltage, saturation effects occur. Without stabilization, these could lead to differential protection tripping. The fact that the current of the protected object under saturation conditions has a high proportion of fifth harmonic serves as the basis of stabilization.

The P64x filters the differential current and determines the fundamental component Idiff(fn) and the fifth harmonic component Idiff(5·fn). If the ratio Idiff(5·fn)/Idiff(fn) exceeds the set value Ih(5)%> in at least one phase in two consecutive calculations, and if the differential current is larger than 0.1 pu (minimum setting of Is1), tripping is blocked selectively for one phase.

There will be no blocking if the differential current exceeds the set thresholds Is-HS1 or Is-HS2.

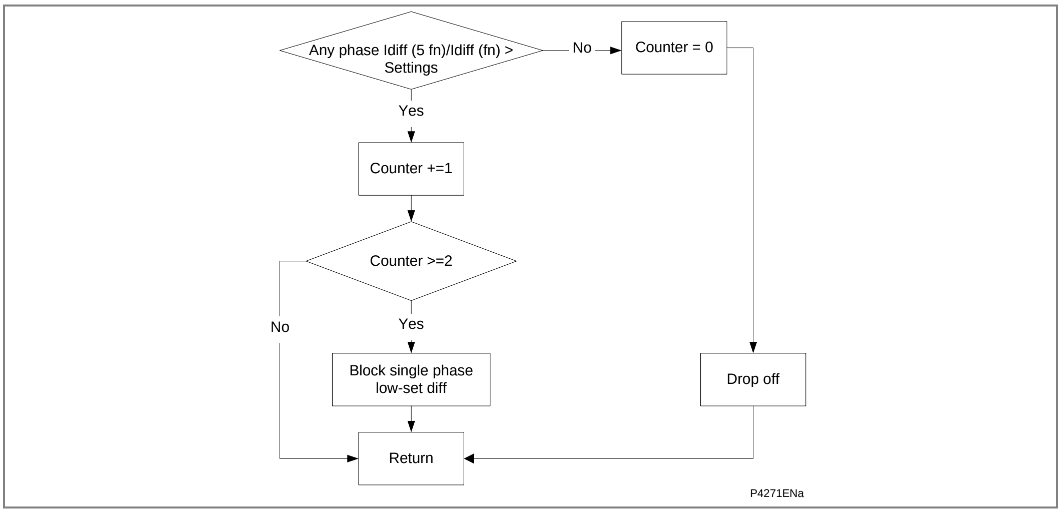
Any phase Idiff (5 fn)/Idiff (fn) > Settings
No
Counter = 0
Yes
Counter +=1
Counter >=2
No
Yes
Block single phase low-set diff
Drop off
Return
P4271ENa

Figure 19 - Overfluxing restraint

Figure 19 shows the inhibiting of the differential algorithm by magnetizing inrush or overfluxing conditions:

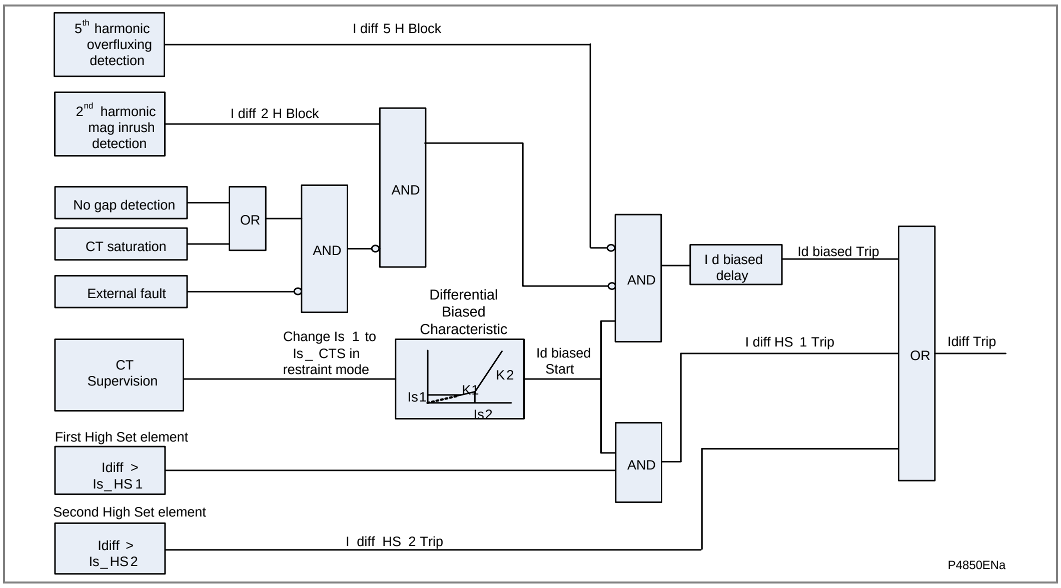
5th harmonic overfluxing detection
I diff 5 H Block
2nd harmonic mag inrush detection
I diff 2 H Block
No gap detection
CT saturation
OR
AND
AND
External fault
AND
I d biased delay
Id biased Trip
OR
Idiff Trip
Differential Biased Characteristic
Change Is 1 to Is_ CTS in restraint mode
CT Supervision
Id biased Start
Is1
K1
K2
Is2
I diff HS 1 Trip
First High Set element
Idiff > Is_HS1
AND
Second High Set element
Idiff > Is_HS2
I diff HS 2 Trip
P4850ENa

Figure 20 - Differential protection

2.2 Restricted Earth Fault (REF) Protection

The settings REF HV status, REF LV status and REF TV status can be set to disabled, low impedance REF or high impedance REF.

2.2.1 Low Impedance Restricted Earth Fault (REF)

A low impedance REF protection function per transformer winding is available for up to three ends. The low impedance REF uses a triple slope biased characteristic, the same as the differential current function. Low impedance REF is based on comparing the vector sum of the phase currents of the transformer winding to the neutral point current. The differential and bias currents are calculated from the current variables after scaling the phase currents.

If current transformer supervision operates, the low impedance REF is blocked. The activation of HV StubBus Act, LV StubBus Act or TV StubBus Act signals also blocks the low impedance REF on a per-winding basis.

In a biased differential relay, the through current is measured and used to increase the setting of the differential element. For heavy through faults, one CT in the scheme can be expected to become more saturated than the other and hence differential current can be produced. However, biasing increases the relay setting so the resulting differential current is insufficient to cause operation of the relay. To provide further stability for external faults and CT saturation, a transient bias current is considered on the calculation of the operating current.

2.2.1.1 Single Breaker Applications

The calculation of differential and mean bias currents in single breaker applications is as follows.

$$I_{bias} = \frac{1}{2}\left[\max\left[\vec{I}_{A_{CTn}}, \vec{I}_{B_{CTn}}, \vec{I}_{C_{CTn}}\right] \times K + I_N\right]$$

$$I_{diff} = \left[\left(\vec{I}_{A_{CTn}} + \vec{I}_{B_{CTn}} + \vec{I}_{C_{CTn}}\right) \times K + I_N\right]$$

Where:

CTn = T1 CT, T2 CT, T3 CT, T4 CT or T5 CT. This is determined by the settings HV CT Terminals, LV CT Terminals and TV CT Terminals. For example, if in a P645 the REF function for the HV winding is enabled and the HV CT Terminals setting is 00001, then CTn is CT1.

The neutral CT is always the reference current, so Is1 and Is2 settings are relative to this CT. Up to three neutral CT inputs are available depending on the relay model. TN1 CT is related to the HV REF function; TN2 CT to the LV REF function and TN3 CT to the TV REF function. If TN1 CT, TN2 CT or TN3 CT setting change, Is1 and Is2 settings are affected accordingly.

scaling factor = k = CTn ratio / Neutral CT ratio

The scaling factor is required to match the summation of the line currents with the current measured in the star point.

I_N = current measured by the neutral CT

Note	*In previous firmware versions, the reference CT is not the neutral CT. Please check manual version A42.*

2.2.1.2 One and a Half Breaker Applications

The low impedance restricted earth fault function in the P64x can also be used in one and a half breaker applications. Also the line CT ratios can be different. The relay uses the following equations to calculate the mean bias and differential currents:

$$I_{bias} = \left[\max\left[\left(\left|\vec{I}_{A_{CTn}}\right| + K_1 \times \left|\vec{I}_{A_{CTm}}\right|\right), \left(\left|\vec{I}_{B_{CTn}}\right| + K_1 \times \left|\vec{I}_{B_{CTm}}\right|\right), \left(\left|\vec{I}_{C_{CTn}}\right| + K_1 \times \left|\vec{I}_{C_{CTm}}\right|\right)\right] \times K_2 + I_N\right]$$

$$I_{diff} = \left[\left(\vec{I}_{A_{CTn}} + \vec{I}_{B_{CTn}} + \vec{I}_{C_{CTn}} + K_1 \times \vec{I}_{A_{CTm}} + K_1 \times \vec{I}_{B_{CTm}} + K_1 \times \vec{I}_{C_{CTm}}\right) \times K_2 + I_N\right]$$

Where:

CTn and CTm = T1 CT, T2 CT, T3 CT, T4 CT or T5 CT. CTn and CTm are the current inputs assigned to each transformer winding, and they are given in the settings HV CT Terminals, LV CT Terminals and TV CT Terminals. CTn is always the reference current, so Is1 and Is2 settings are relative to this CT.

The neutral CT is always the reference CT, so Is1 and Is2 settings are relative to it. Up to three neutral CT inputs are available depending on the relay model. TN1 CT is related to the HV REF function; TN2 CT to the LV REF function and TN3 CT to the TV REF function. If the TN1 CT, TN2 CT or TN3 CT setting change, Is1 and Is2 settings are affected accordingly.

K1 = CTm ratio / CTn ratio

K2 = CTn ratio / Neutral CT ratio.

IN = current measured by the neutral CT

From the differential and bias equations it can be observed that first the current flowing through CTm is referred to CTn. Second, CTm current referred to CTn and the current flowing through CTn are referred to the neutral CT.

Consider the HV REF function in a P645. If the HV CT Terminals setting is 00011, then CTn = T1 CT and CTm = T2 CT. Therefore, K1 = T2 CT ratio / T1 CT ratio and K2 = T1 CT ratio / Neutral CT ratio.

Now, consider the LV REF function. If the LV CT Terminals setting is 11000, then CTn = 5 and CTm = 4. Therefore, K1 = T4 CT ratio / T5 CT ratio and K2 = T5 CT ratio / Neutral CT ratio.

Finally, consider the TV REF function. In this example, only current input three is available; therefore the LV CT Terminals setting is 00100. In this case, the relay uses the differential and bias equations for single breaker applications, and K = T3 CT ratio / Neutral CT ratio.

If more than two line current transformers are assigned to the HV/LV/TV CT Terminals, the low impedance REF can also be applied. The number of scaling factors is increased accordingly.

2.2.1.3 Autotransformer Applications

The low impedance restricted earth fault function in the P64x can also be used to protect an autotransformer as shown in Figure 20. Also the line CT ratios can be different and Kn is the scaling factor of each of the current transformers involved in the application. The setting cell REF Auto Status is only available when the Winding Type setting cell is set to Auto.

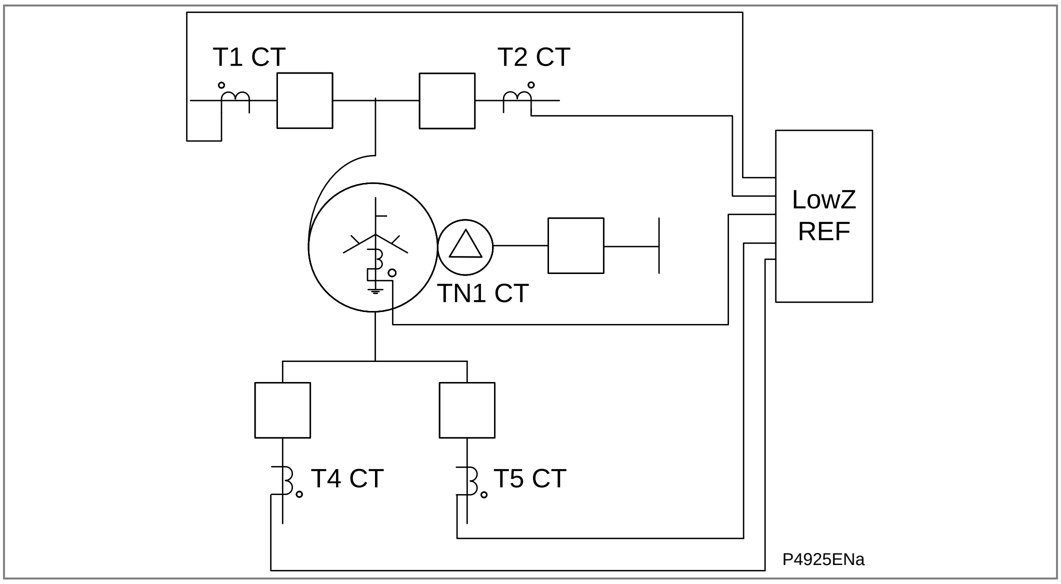

Figure 21 - Low impedance REF

The relay uses the following equations to calculate the mean bias and differential currents:

$$I_{bias} = \frac{1}{2} \times \left\{ \max\left[\sum_{n=1}^{n} \left| \vec{I} A_{Tn\,CT} \right| \times K_n, \sum_{n=1}^{n} \left| \vec{I} B_{Tn\,CT} \right| \times K_n, \sum_{n=1}^{n} \left| \vec{I} C_{Tn\,CT} \right| \times K_n \right] + \left| \vec{I}_{TN1CT} \right| \right\}$$

$$I_{diff} = \left| \sum_{n=1}^{n} \left[\left(\vec{I} A_{Tn\,CT} + \vec{I} B_{Tn\,CT} + \vec{I} C_{Tn\,CT} \right) \times K_n \right] + \vec{I}_{TN1CT} \right|$$

Where:

$$K_n = Tn\,CT\_ratio/TN1CT\_ratio$$

For example, the bias and differential calculations for the application shown in Figure 17 are as follows:

$$I_{bias} = \frac{1}{2} \times \left\{ \max \begin{bmatrix} \left|\vec{I} A_{T1CT}\right| \times K_1 + \left|\vec{I} A_{T2\,CT}\right| \times K_2 + \left|\vec{I} A_{T3\,CT}\right| \times K_3 + \left|\vec{I} A_{T4\,CT}\right| \times K_4 + \left|\vec{I} A_{T5\,CT}\right| \times K_5, \\ \left|\vec{I} B_{T1CT}\right| \times K_1 + \left|\vec{I} B_{T2\,CT}\right| \times K_2 + \left|\vec{I} B_{T3\,CT}\right| \times K_3 + \left|\vec{I} B_{T4\,CT}\right| \times K_4 + \left|\vec{I} B_{T5\,CT}\right| \times K_5, \\ \left|\vec{I} C_{T1CT}\right| \times K_1 + \left|\vec{I} C_{T2\,CT}\right| \times K_2 + \left|\vec{I} C_{T3\,CT}\right| \times K_3 + \left|\vec{I} C_{T4\,CT}\right| \times K_4 + \left|\vec{I} C_{T5\,CT}\right| \times K_5 \end{bmatrix} + \left|\vec{I}_{TN1CT}\right| \right\}$$

$$I_{diff} = \left| \begin{array}{l} \left(\vec{I}A_{T1CT} + \vec{I}B_{T1CT} + \vec{I}C_{T1CT}\right) \times K_1 \\ + \left(\vec{I}A_{T2CT} + \vec{I}B_{T2CT} + \vec{I}C_{T2CT}\right) \times K_2 \\ + \left(\vec{I}A_{T3CT} + \vec{I}B_{T3CT} + \vec{I}C_{T3CT}\right) \times K_3 \\ + \left(\vec{I}A_{T4CT} + \vec{I}B_{T4CT} + \vec{I}C_{T4CT}\right) \times K_4 \\ + \left(\vec{I}A_{T5CT} + \vec{I}B_{T5CT} + \vec{I}C_{T5CT}\right) \times K_5 \\ + \vec{I}_{TN1CT} \end{array} \right|$$

Where:

$K1 = T1CT\_ratio/TN1CT\_ratio$

$K2 = T2\,CT\_ratio/TN1CT\_ratio$

$K3 = T3\,CT\_ratio/TN1CT\_ratio$

$K4 = T4\,CT\_ratio/TN1CT\_ratio$

$K5 = T5\,CT\_ratio/TN1CT\_ratio$

TN1 CT is always the reference CT in an autotransformer application. If TN1 CT setting changes, Is1 and Is2 settings are affected accordingly.

2.2.2 Scaling Factor(s)

The scaling factor(s) described in sections 2.2.1.1 Single breaker applications, 2.2.1.2 One and a half breaker applications and 2.2.1.3 Autotransformer applications must satisfy the following condition:

- The scaling factor(s) must always be $0.05 \le K \le 20$

If this condition is not satisfied, then an alarm is issued and the low impedance REF protection is blocked.

2.2.2.1 Transient Bias

An additional bias quantity is introduced on a per-winding basis, if there is a sudden increase in the mean bias calculation. Transient bias is added for through fault stability and it decays exponentially. The transient bias is reset to zero once the relay trip or if the mean bias quantity is below 0.5*Is1.

The transient bias is removed after the relay has tripped to avoid the possibility of chattering. It is also removed when Ibias is less than 0.5*Is1 to avoid the possibility of residual values due to the numerical effects.

No transient bias is produced under load switching conditions or when the CT comes out of saturation, which will also cause an increase of bias.

The mean bias current is available as a measurement display and in the fault records.

2.2.2.2 Tripping Characteristic

The tripping characteristic of the low impedance REF has two knees. The first knee is dependent on the settings of I_{s1} and K1. The second knee of the tripping characteristic is defined by the setting I_{s2}. The lower slope provides sensitivity for internal faults. The higher slope provides stability under through fault conditions, since transient differential currents may be present due to current transformer saturation.

Once the differential and bias currents are calculated, the following comparisons are made and an operate/restrained signal is obtained:

Flat slope: $I_{bias} \leq \frac{I_{s1}}{K1}$

$$I_{diff} \geq I_{s1} + \text{Transient Bias}$$

K1 slope: $\frac{I_{s1}}{K1} \leq I_{bias} \leq I_{s2}$

$$I_{diff} \geq K1 \cdot I_{bias} + \text{Transient Bias}$$

K2 slope: $I_{bias} \geq I_{s2}$

$$I_{diff} \geq K1 \cdot I_{s2} + K2 \cdot \left(I_{bias} - I_{s2}\right) + \text{Transient Bias}$$

In the equations above, $I_{bias,y}$ is the delayed bias and as explained previously it is the highest bias current in the last cycle.

The protection trips on a count of 5, which is approximately 25 ms after fault detection.

Figure 21 shows the operating characteristic for the low impedance REF.

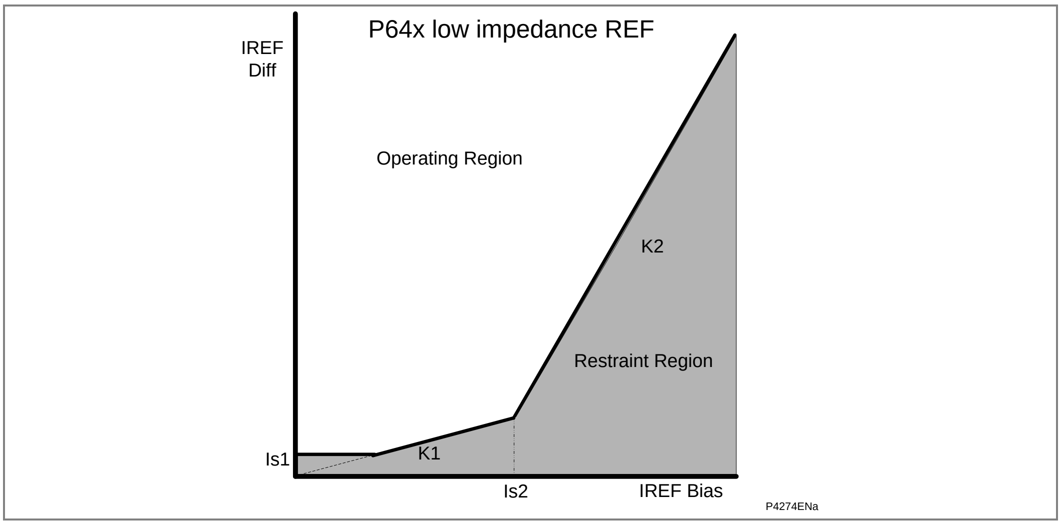

Figure 22 - Low impedance REF characteristic

2.2.3 High Impedance Restricted Earth Fault (REF)

A high impedance Restricted Earth Fault (REF) protection function per transformer winding is available for up to three ends. An external resistor is required to provide stability in the presence of saturated line current transformers.

The high impedance REF protection works on the high impedance circulating current principle shown in Figure 22.

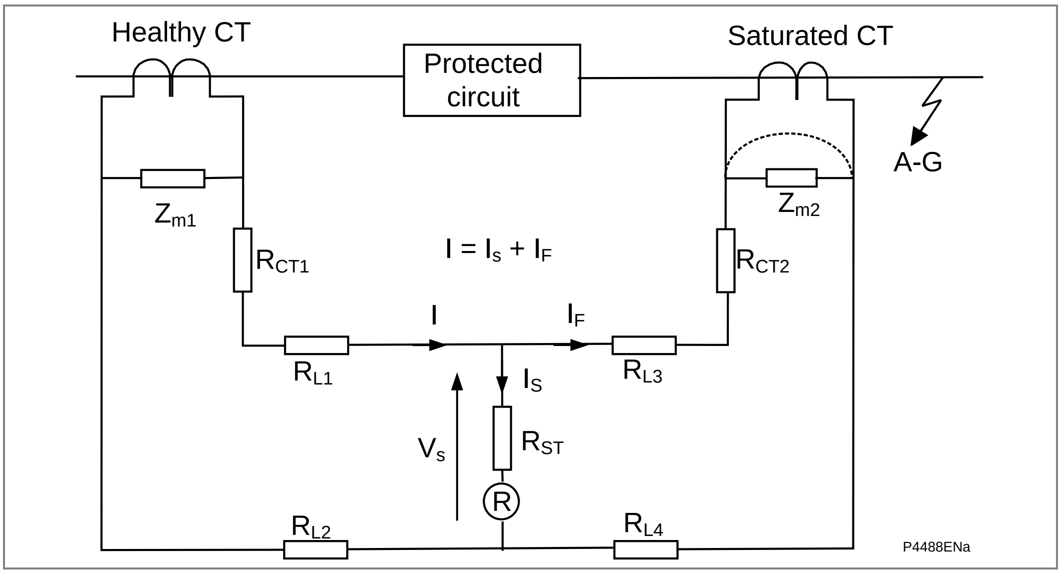

Figure 23 - High impedance differential principle

When subjected to heavy through faults the line current transformer may enter saturation unevenly, resulting in unbalance. To ensure stability under these conditions a series connected external resistor is required, so that most of the unbalanced current will flow through the saturated CT. As a result, the current flowing through the relay will be less than the setting, thus maintaining stability during external faults. Harmonics are rejected by basing the measurement on the fundamental frequency Fourier magnitude.

TN1, T1N CT is associated to the HV winding high impedance REF, or to the autotransformer high impedance TN2, T2N CT is associated to the LV winding high impedance REF and TN3, T3N CT is associated to the TV winding high impedance REF.

Current transformer supervision, HV StubBus Act, LV StubBus Act or TV StubBus Act signals do not block the high impedance REF. The appropriate logic must be configured in psl to block the high impedance REF when any of the above signals is asserted.

2.3 Overcurrent Protection (50/51)

Three four-stage overcurrent elements are included in the P64x relays. Each element provides four-stage non-directional/directional three-phase overcurrent protection with independent time delay characteristics. The overcurrent element operating quantity may be selected in the setting cell **Overcurrent x**. It can be set as T1, T2, T3, T4, T5, HV winding, LV winding and TV winding. HV, LV and TV winding consider the vectorial sum of the CT inputs associated to a particular winding.

In a P642 relay, the HV Winding **I>x Current Set** settings are relative to T1 CT, and the LV Winding **I>x Current Set** settings are relative to T2 CT.

In a P643 relay, the HV Winding **I>x Current Set** settings are relative to T1 CT. If the HV CT Terminals setting is 011, then T1 CT and T2 CT are assigned to the HV winding. If the T1 CT setting changes, **I>x Current Set** is affected accordingly. However, if the T2 CT setting changes, **I>x Current Set** settings are not affected. LV Winding **I>x Current Set** settings are relative to T3 CT. TV Winding **I>x Current Set** settings are relative to T2 CT.

In a P645 relay, the HV Winding **I>x Current Set** settings are relative to T1 CT. The LV Winding **I>x Current Set** settings are relative to T5 CT. The TV Winding **I>x Current Set** settings are relative to T3 CT. If the TV CT Terminals setting is 00110, then T2 CT and T3 CT are assigned to the TV winding. If T3 CT setting changes, **I>x Current Set** settings are affected accordingly. However, if the T2 CT setting changes, **I>x Current Set** settings are not affected.

All overcurrent and directional settings apply to all three phases but are independent for each of the four stages. The overcurrent element may be set as directional only if the three phase VT input is available in the P643/P645 and if the two single phase VT inputs are available in the P642. The VT may be assigned to the HV, LV or TV winding. Therefore, overcurrent directional elements are available to the current inputs associated to the winding which has the VT input assigned.

The first two stages of overcurrent protection have time-delayed characteristics which are selectable between Inverse Definite Minimum Time (IDMT), or Definite Time (DT). The third and fourth stages have definite time characteristics only.

Various methods are available to achieve correct relay co-ordination on a system; by means of time alone, current alone or a combination of both time and current. Grading by means of current is only possible where there is an appreciable difference in fault level between the two relay locations. Grading by time is used by some utilities but can often lead to excessive fault clearance times at or near source substations where the fault level is highest. For these reasons the most commonly applied characteristic in coordinating overcurrent relays is the IDMT type.

The inverse time delayed characteristics indicated above, comply with the following formula:

IEC curves IEEE curves

$$t = T \times \left(\frac{\beta}{(M^{\alpha} - 1)} + L \right) \quad \text{or} \quad t = TD \times \left(\frac{\beta}{(M^{\alpha} - 1)} + L \right) \text{ where:}$$

t = Operation time
β = Constant
M = I/Is
I = Measured current
Is = Current threshold setting
α = Constant
L = ANSI/IEEE constant (zero for IEC curves)
T = Time multiplier setting for IEC curves
TD = Time dial setting for IEEE curves

Curve description	Standard	β constant	α constant	L constant
Standard Inverse	IEC	0.14	0.02	0
Very Inverse	IEC	13.5	1	0
Extremely Inverse	IEC	80	2	0
Long Time Inverse	UK	120	1	0
Rectifier	UK	45900	5.6	0
Moderately Inverse	IEEE	0.0515	0.02	0.114
Very Inverse	IEEE	19.61	2	0.491
Extremely Inverse	IEEE	28.2	2	0.1217
Inverse	US	5.95	2	0.18
Short Time Inverse	US	0.16758	0.02	0.11858

Table 6 - Curve description constants

Note *The IEEE and US curves are set differently to the IEC/UK curves, with regard to the time setting. A Time Multiplier Setting (TMS) is used to adjust the operating time of the IEC curves, whereas a time dial setting is employed for the IEEE/US curves. The menu is arranged so that if an IEC/UK curve is selected, the **I>1 Time Dial** cell is not visible and if the IEEE/US curve is selected the **I>1 TMS** cell is not visible.*

Note	*The IEC/UK inverse characteristics can be used with a definite time reset characteristic, however, the IEEE/US curves may have an inverse or definite time reset characteristic. The following equation can used to calculate the inverse reset time for IEEE/US curves:*

$$tRESET = \frac{TD \times S}{(1 - M^2)} \text{ in seconds}$$

where:

TD = Time dial setting for IEEE curves

S = Constant

M = I/Is

Curve description	Standard	S constant
Moderately Inverse	IEEE	4.85
Very Inverse	IEEE	21.6
Extremely Inverse	IEEE	29.1
Inverse	US	5.95
Short Time Inverse	US	2.261

Table 7 - Curve description standards

Note	*The rectifier curve is only provided in the first and second stage characteristic setting options for phase overcurrent protection.*

2.3.1 RI Curve

The RI curve (electromechanical) has been included in the first and second stage characteristic setting options for phase overcurrent and earth fault protections. The curve is represented by this equation.

$$t = K \times \left(\frac{1}{0.339 - \left({}^{0.236}/_{M} \right)} \right) \text{ in seconds}$$

With K adjustable from 0.1 to 10 in steps of 0.05

2.3.2 Timer Hold Facility

The first two stages of overcurrent protection in the P64x relays are provided with a timer hold facility, which may either be set to zero or to a definite time value. Setting of the timer to zero means that the overcurrent timer for that stage will reset instantaneously once the current falls below 95% of the current setting. Setting of the hold timer to a value other than zero, delays the resetting of the protection element timers for this period. When the reset time of the overcurrent relay is instantaneous, the relay will be repeatedly reset and not be able to trip until the fault becomes permanent. By using the Timer Hold facility the relay will integrate the fault current pulses, thereby reducing fault clearance time.

The timer hold facility can be found for the first and second overcurrent stages as settings **I>1 tRESET** and **I>2 tRESET**, respectively. If an IEC inverse or DT operating characteristic is chosen, this time delay is set using the **I>1/2 tRESET** setting. If an IEEE/US operate curve is selected, the reset characteristic may be set to either definite time or inverse time as selected in cell **I>1/2 Reset Char**. If definite time (‘DT’) is selected the **I>1/2 tRESET** cell may be used to set the time delay. If inverse time reset (**Inverse**) is selected the reset time will follow the inverse time operating characteristic, modified by the time dial setting, selected for **I>1/2 Function**.

The functional logic diagram for non-directional overcurrent is shown in Figure 23.

A timer block input is available for each stage which will reset the overcurrent timers of all three phases if energized, taking account of the reset time delay if selected for the “I>1” and “I>2” stages. DDB signals are also available to indicate the start and trip of each phase of each stage of protection. The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

Overcurrent protection starts 1/2/3/4 are mapped internally to the ANY START DDB signal - DDB 1312.

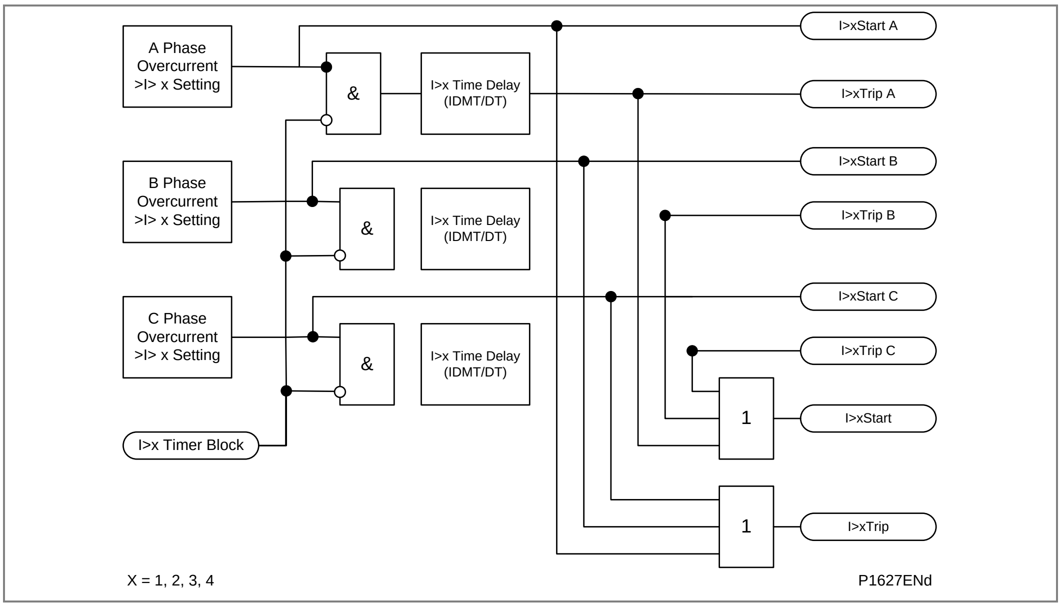
A Phase Overcurrent >I> x Setting
B Phase Overcurrent >I> x Setting
C Phase Overcurrent >I> x Setting
I>x Timer Block
&
&
&
I>x Time Delay (IDMT/DT)
I>x Time Delay (IDMT/DT)
I>x Time Delay (IDMT/DT)
I>xStart A
I>xTrip A
I>xStart B
I>xTrip B
I>xStart C
I>xTrip C
1
I>xStart
1
I>xTrip
X = 1, 2, 3, 4
P1627ENd

Figure 24 - Non-directional overcurrent logic diagram

2.4 Directional Overcurrent Protection (67)

The P643 and P645 can be provided with an additional three-phase VT input. Therefore it will only be possible to set the directionality of the overcurrent phase fault protection when this optional VT input is provided in the P643/P645. It is possible to set the directionality of the overcurrent phase fault protection in the P642 when two single phase VT inputs are available.

In a P643 relay, the HV Winding **I>x Current Set** settings are relative to T1 CT. If the HV CT Terminals setting is 011, then T1 CT and T2 CT are assigned to the HV winding. If the T1 CT setting changes, **I>x Current Set** is affected accordingly. However, if the T2 CT setting changes, **I>x Current Set** settings are not affected. LV Winding **I>x Current Set** settings are relative to T3 CT. TV Winding **I>x Current Set** settings are relative to T2 CT.

In a P645 relay, the HV Winding **I>x Current Set** settings are relative to T1 CT. The LV Winding **I>x Current Set** settings are relative to T5 CT. The TV Winding **I>x Current Set** settings are relative to T3 CT. If the TV CT Terminals setting is 00110, then T2 CT and T3 CT are assigned to the TV winding. If the T3 CT setting changes, **I>x Current Set** settings are affected accordingly. However, if the T2 CT setting changes, **I>x Current Set** settings are not affected.

The phase fault elements of the P64x relays are internally polarized by the quadrature phase-phase voltages, as shown in the table below:

Phase of protection	Operate current	Polarizing voltage
A Phase	IA	VBC
B Phase	IB	VCA
C Phase	IC	VAB

Table 8 - Phase fault elements

Note	*Under system fault conditions, the fault current vector will lag its nominal phase voltage by an angle dependent upon the system X/R ratio. It is therefore a requirement that the relay operates with maximum sensitivity for currents lying in this region. This is achieved by means of the relay characteristic angle (RCA) setting; this defines the angle by which the current applied to the relay must be displaced from the voltage applied to the relay to obtain maximum relay sensitivity. This is set in cell I>Char Angle in the Overcurrent menu. On the P64x relays, it is possible to set characteristic angles anywhere in the range -95° to +95°.*

The functional logic block diagram for directional overcurrent is shown in Figure 24.

The overcurrent level detector detects that the current magnitude is above the threshold and together with the respective polarizing voltage, a directional check is performed based on the following criteria:

Directional forward:

$$-90^\circ < (\text{angle}(I) - \text{angle}(V) - \text{RCA}) < 90^\circ$$

Directional reverse:

$$-90^\circ > (\text{angle}(I) - \text{angle}(V) - \text{RCA}) > 90^\circ$$

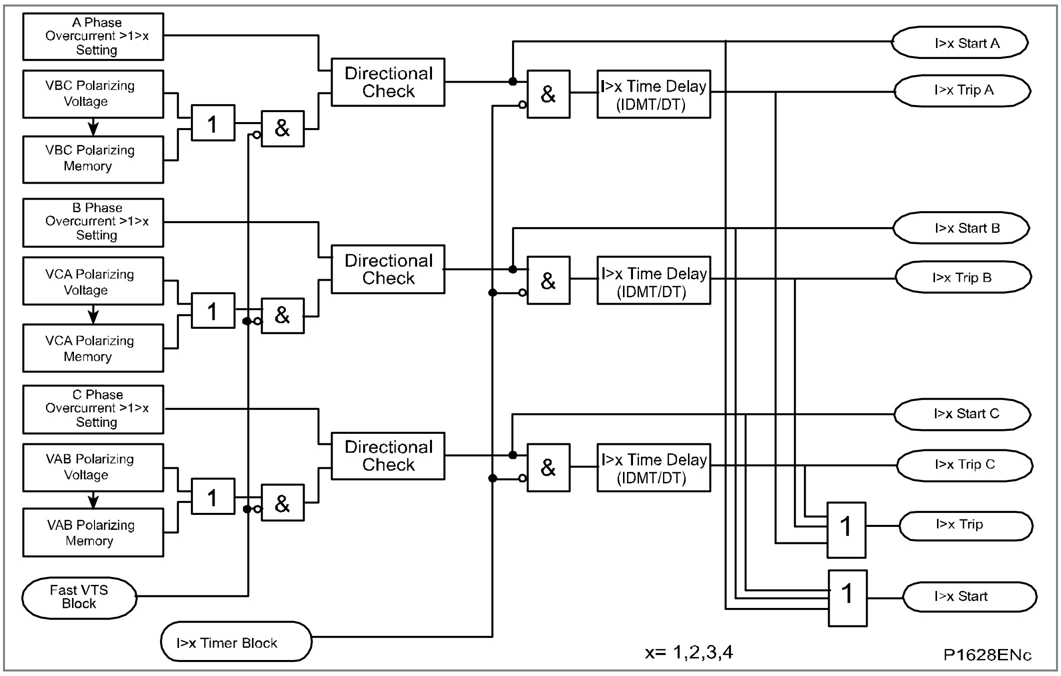
A Phase Overcurrent >1>x Setting
VBC Polarizing Voltage
VBC Polarizing Memory
B Phase Overcurrent >1>x Setting
VCA Polarizing Voltage
VCA Polarizing Memory
C Phase Overcurrent >1>x Setting
VAB Polarizing Voltage
VAB Polarizing Memory
Fast VTS Block
I>x Timer Block
1
&
Directional Check
I>x Time Delay (IDMT/DT)
I>x Start A
I>x Trip A
I>x Start B
I>x Trip B
I>x Start C
I>x Trip C
I>x Trip
I>x Start
x= 1,2,3,4
P1628ENc

Figure 25 - Directional overcurrent logic

Any of the four overcurrent stages may be configured to be directional, noting that IDMT characteristics are only selectable on the first two stages. When the element is selected as directional, a VTS Block option is available in the **I> Function Link** setting. When the relevant bit is set to 1, operation of the Voltage Transformer Supervision (VTS), will block the stage if directionalized. When set to 0, the stage will revert to non-directional on operation of the VTS.

2.4.1 Synchronous Polarization

For a close up three-phase fault, all three voltages will collapse to zero and no healthy phase voltages will be present. For this reason, the P64x relays include a synchronous polarization feature that stores the pre-fault voltage information and continues to apply it to the directional overcurrent elements for a time period of 3.2 seconds. This ensures that either instantaneous or time delayed directional overcurrent elements will be allowed to operate, even with a three-phase voltage collapse.

2.5 Voltage Controlled Overcurrent

A two stage three-phase voltage controlled overcurrent element is available in P643/P645 when the three phase VT has been fitted. Phase-to-phase voltages are used by the voltage controlled overcurrent function. In P643/P645, the phase-to-phase voltages are derived from the measured phase-to-neutral voltages.

If the current seen by a local relay for a remote fault condition is below it's overcurrent setting, a Voltage Controlled Overcurrent (VCO) element may be used to increase the relay sensitivity to such faults. In this case, a reduction in system voltage will occur; this is used to reduce the pick up level of the overcurrent protection. The current setting is modified by a multiplier k when the voltage falls below a threshold as shown in the following table:

Element	Phase to Phase control voltage	Element pickup when control voltage > setting	Element pickup when control voltage < setting
Ia>	Vab	VCO>1 I>Set, VCO>2 I>Set	VCO>1 K(RI) * VCO>1 I>Set, VCO>1 K Set * VCO>1 I>Set, VCO>2 K(RI) * VCO>2 I>Set, VCO>2 K Set * VCO>2 I>Set,
Ib>	Vbc	VCO>1 I>Set, VCO>2 I>Set	VCO>1 K(RI) * VCO>1 I>Set, VCO>1 K Set * VCO>1 I>Set, VCO>2 K(RI) * VCO>2 I>Set, VCO>2 K Set * VCO>2 I>Set,
Ic>	Vca	VCO>1 I>Set, VCO>2 I>Set	VCO>1 K(RI) * VCO>1 I>Set, VCO>1 K Set * VCO>1 I>Set, VCO>2 K(RI) * VCO>2 I>Set, VCO>2 K Set * VCO>2 I>Set,

Table 9 - Current setting modification multipliers

The voltage threshold is set in **VCO>1 V< Set, VCO>2 V< Set** setting cells. The current setting is set in **VCO>1 I>Set** and **VCO>2 I>Set** setting cells. The K multiplier is set in **VCO>1 K(RI), VCO>2 K(RI), VCO>1 K Set,** or **VCO>2 K Set** settings cells.

Two VCO stages are available and each one can be set to HV winding, LV winding, TV winding, T1 CT, T2 CT, T3 CT, T4 CT, T5 CT or disabled. If the current signal chosen for a VCO stage does not belong to the winding where the VT is located, then the VCO element is blocked and a configuration error alarm is asserted. VCO1 Config err (DDB 472) or VCO2 Config err (DDB 473) alarms might be asserted.

Note *Voltage-dependent overcurrent relays are more often applied in generator protection applications in order to give adequate overcurrent relay sensitivity for close up fault conditions. The fault characteristic of this protection must then co-ordinate with any of the downstream overcurrent relays that are responsive to the current decrement condition.*

Note Although the P642 does have two VT inputs, one is used for V/Hz protection is used by the NPS overvoltage and VCO protection. Consequently, it is not possible to use the P542 for Overvoltage or Undervoltage protection.

2.6 Earth Fault

The earth fault element is based on the neutral current of any of the transformer windings or any of the current transformer inputs. The user can select between measured neutral current or derived neutral current in the **EF x Input** setting. The earth fault derived current signal may be selected in the **EF x Derived** setting and the options are HV winding, LV winding, TV winding, T1, T2, T3, T4 and T5. If HV winding, LV winding or TV winding is chosen, then the derived zero sequence current considers the CTs assigned in **HV CT Terminals, LV CT Terminals or TV CT Terminals** respectively. If the **EF x Input** is set to measured, then the **EF x Measured** setting options are TN1, TN2 and TN3.

Three four-stage earth fault elements are available. The first and second stages have selectable IDMT or DT characteristics, while the third and fourth stages are DT only. Each stage is selectable to be either non-directional, directional forward or directional reverse. The Timer Hold facility, previously described for the overcurrent element, is available on each of the first two stages.

The description in the next three paragraphs is valid when the **EF x Input** setting is set to **Derived**.

In a P642 relay, the HV Winding **IN>x Current** settings are relative to T1 CT, and the LV Winding **IN>x Current** settings are relative to T2 CT.

In a P643 relay, the HV Winding **IN>x Current** settings are relative to T1 CT. If the **HV CT Terminals** setting is 011, then T1 CT and T2 CT are assigned to the HV winding. If the T1 CT setting changes, **IN>x Current** is affected accordingly. However, if the T2 CT setting changes, the **IN>x Current** settings are not affected. The LV Winding **IN>x Current** settings are relative to T3 CT. The TV Winding **IN>x Current** settings are relative to T2 CT.

In a P645 relay, the HV Winding **IN>x Current** settings are relative to T1 CT. The LV Winding **IN>x Current** settings are relative to T5 CT. The TV Winding **IN>x Current** settings are relative to T3 CT. If the TV CT Terminals setting is 00110, then T2 CT and T3 CT are assigned to the TV winding. If the T3 CT setting changes, the **IN>x Current** settings are affected accordingly. However, if the T2 CT setting changes, the **IN>x Current** settings are not affected.

The logic diagram for non-directional earth fault overcurrent is shown in Figure 25.

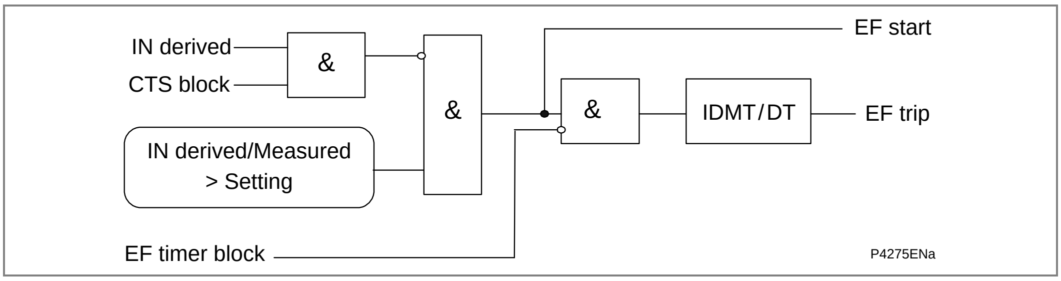

Figure 26 - Non-directional EF logic (single stage)

The earth fault protection can be set IN/OUT of service using the appropriate DDB inhibit signal that can be operated from an opto input or control command.

For inverse time delayed characteristics refer to the phase overcurrent elements, section 2.3.

2.6.1 IDG Curve

The IDG curve is provided in the first and second stage characteristic setting options for earth fault protection. It is commonly used for time delayed earth fault protection in the Swedish market.

The IDG curve is represented by the following equation:

$$t = 5.8 - 1.35 \log_e \left(\frac{I}{IN > Setting} \right) \text{ in seconds}$$

Where:

I = Measured current

IN>Setting = An adjustable setting which defines the start point of the characteristic

Although the start point of the characteristic is defined by the **IN>** setting, the actual relay current threshold is a different setting called **IDG Is**. The **IDG Is** setting is set as a multiple of **IN>**.

An additional setting **IDG Time** is also used to set the minimum operating time at high levels of fault current.

Figure 26 shows how the IDG characteristic is implemented.

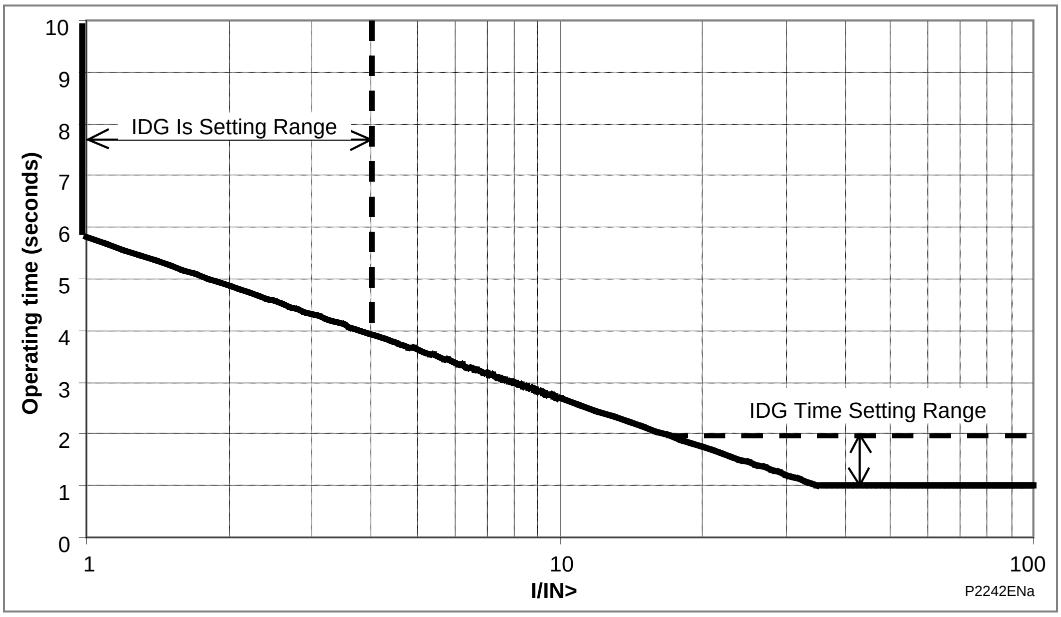

Figure 27 - IDG characteristic

2.7 Directional Earth Fault Protection (DEF)

If the earth fault element is set as directional and the **EF x Input** is set to measured, then only TN1 might be chosen to measure the zero current on the HV winding or the zero sequence current of any of the CTs assigned to the HV winding. Only TN2 might be chosen to measure the zero current on the LV winding or the zero sequence current of any of the CTs assigned to the LV winding. Only TN3 might be chosen to measure the zero current on the TV winding or the zero sequence current of any of the CTs assigned to the TV winding.

The following description is valid when the **EF x Input** setting is set to **Derived**.

In a P642 relay, if **EF x Derived** is set to HV Winding, then **IN>x Current** settings are relative to T1 CT. If **EF x Derived** is set to LV Winding, then **IN>x Current** settings are relative to T2 CT.

In a P643 relay, if **EF x Derived** is set to HV Winding, then **IN>x Current** settings are relative to T1 CT. Consider that HV CT Terminals is set to 011, therefore T1 CT and T2 CT are assigned to the HV winding. If T1 CT setting changes, **IN>x Current** is affected accordingly. However, if T2 CT setting changes, **IN>x Current** settings are not affected. If **EF x Derived** is set to LV Winding, then **IN>x Current** settings are relative to T3 CT. If **EF x Derived** is set to TV Winding, then IN**>x Current** settings are relative to T2 CT.

In a P645 relay, if **EF x Derived** is set to the HV Winding, then **IN>x Current** settings are relative to T1 CT. If **EF x Derived** is set to The LV Winding, then **IN>x Current** settings are relative to T5 CT. If **EF x Derived** is set to The TV Winding, then **IN>x Current** settings are relative to T3 CT. Consider that **TV CT Terminals** is 00110; therefore, T2 CT and T3 CT are assigned to the TV winding. If the T3 CT setting changes, **IN>x Current** settings are affected accordingly. However, if the T2 CT setting changes, **IN>x Current** settings are not affected.

Each of the four stages may be set to be directional if required. Consequently, a suitable voltage supply is required by the relay to provide the necessary polarization. The P643 and P645 may be provided with an additional three-phase VT input. Therefore only when this optional VT input is provided in the P643 or P645, it is possible to set the directionality of the overcurrent earth fault protection. In P643/P645 two options are available for polarization; Residual Voltage or Negative Sequence. In P642, it may also be possible to directionalize the earth fault element when two single phase VTs are available. In the P642, only negative sequence can be used for polarization.

2.7.1.1 Residual Voltage Polarization

With earth fault protection, the polarizing signal must be representative of the earth fault condition. As residual voltage is generated during earth fault conditions, this quantity is commonly used to polarize DEF elements. The P64x relay internally derives this voltage from the 3-phase voltage input that must be supplied from either a 5-limb or three single-phase VTs. A three-limb VT has no path for residual flux and is therefore unsuitable to supply the relay.

It is possible that small levels of residual voltage will be present under normal system conditions due to system imbalances, VT inaccuracies and relay tolerances. Hence, the P64x relay includes a user settable threshold **IN>VNPol Set** which must be exceeded in order for the DEF function to be operational. The residual voltage measurement provided in the **Measurements 1** column of the menu may assist in determining the required threshold setting during the commissioning stage, as this will indicate the level of standing residual voltage present.

Note	*Residual voltage is nominally 180° out of phase with residual current. Consequently, the DEF elements are polarized from the "-Vres" quantity. This 180° phase shift is automatically introduced in the P64x relay.*

The logic diagram for directional earth fault overcurrent with neutral voltage polarization is shown in Figure 27.

VT Supervision (VTS) selectively blocks the directional protection or causes it to revert to non-directional operation. When selected to block the directional protection, VTS blocking is applied to the directional checking which effectively blocks the start outputs as well.

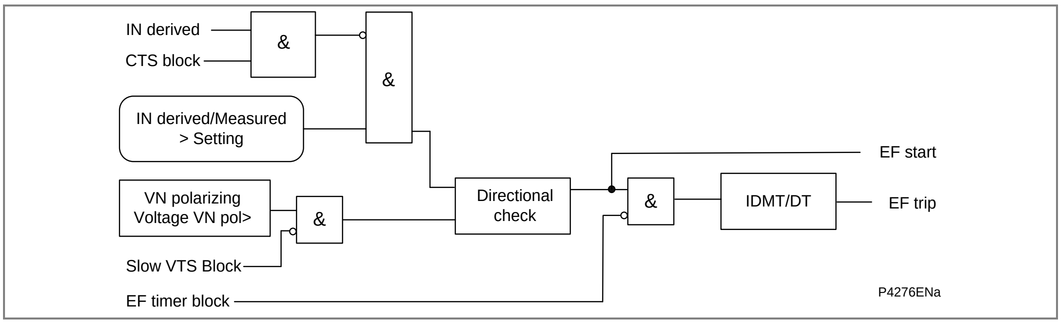
IN derived
CTS block
&
&
IN derived/Measured > Setting
VN polarizing Voltage VN pol>
&
Slow VTS Block
EF timer block
Directional check
&
IDMT/DT
EF start
EF trip
P4276ENa

Figure 28 - Directional EF with neutral voltage polarization (single state)

2.7.2 Negative Sequence Polarization

In certain applications, the use of residual voltage polarization of DEF may either be not possible to achieve, or problematic. An example of the former case would be where a suitable type of VT was unavailable, for example if only a three-limb VT was fitted. An example of the latter case would be an HV/EHV parallel line application where problems with zero sequence mutual coupling may exist.

In either of these situations, the problem may be solved by the use of Negative Phase Sequence (nps) quantities for polarization. This method determines the fault direction by comparison of nps voltage with nps current. The operate quantity, however, is still residual current.

It requires a suitable voltage and current threshold to be set in cells **IN>V2pol Set** and **IN>I2pol Set,** respectively.

Negative sequence polarizing is not recommended for impedance earthed systems regardless of the type of VT feeding the relay. This is due to the reduced earth fault current limiting the voltage drop across the negative sequence source impedance (V_2pol) to negligible levels. If this voltage is less than 0.5 volts the relay will cease to provide DEF.

The logic diagram for directional earth fault overcurrent with negative sequence polarization is shown in Figure 28.

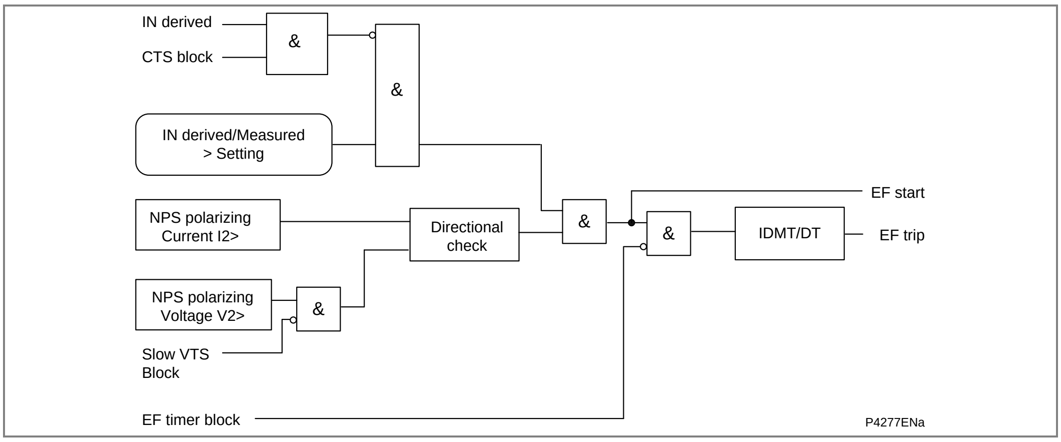
IN derived
CTS block
&
&
IN derived/Measured > Setting
NPS polarizing Current I2>
Directional check
&
NPS polarizing Voltage V2>
&
Slow VTS Block
EF timer block
&
IDMT/DT
EF start
EF trip
P4277ENa

Figure 29 - Directional EF with negative sequence polarization (single stage)

The directional criteria with negative sequence polarization is given below:

Directional forward:

- -90° < (angle(I2) - angle(V2 + 180°) - RCA) < 90°

Directional reverse:

- -90° > (angle(I2) - angle(V2 + 180°) - RCA) > 90°

2.8 Negative Phase Sequence (NPS) Overcurrent Protection (46 OC)

Three four-stage Negative Phase Sequence (NPS) overcurrent elements are available. The negative sequence overcurrent element operating quantity is either the vectorial sum of the negative sequence currents of the CT inputs associated to a particular winding or the negative sequence current flowing through any of the current inputs. The operating quantity may be selected in the setting cell **NPS O/C x**.

In a P642 relay, if **NPS O/C x** is set to HV Winding, then **I2>x Current Set** settings are relative to T1 CT. I, and f **NPS O/C x** is set to LV Winding, then **I2>x Current Set** settings are relative to T2 CT.

In a P643 relay, if **NPS O/C x** is set to HV Winding, then **I2>x Current Set** settings are relative to T1 CT. If the HV CT Terminals setting is 011, then T1 CT and T2 CT are assigned to the HV winding. If the T1 CT setting changes, **I2>x Current Set** is affected accordingly. However, if the T2 CT setting changes, **I2>x Current Set** settings are not affected. If **NPS O/C x** is set to LV Winding, then **I2>x Current Set** settings are relative to T3 CT. If **NPS O/C x** is set to TV Winding, then **I2>x Current Set** settings are relative to T2 CT.

In a P645 relay, if **NPS O/C x** is set to HV Winding, then **I2>x Current Set** settings are relative to T1 CT. If **NPS O/C x** is set to LV Winding, then **I2>x Current Set** settings are relative to T5 CT. If **NPS O/C x** is set to TV Winding, then **I2>x Current Set** settings are relative to T3 CT. If the TV CT Terminals setting is 00110, then T2 CT and T3 CT are assigned to the TV winding. If the T3 CT setting changes, **I2>x Current Set** settings are affected accordingly. However, if the T2 CT setting changes, **I2>x Current Set** settings are not affected.

The P64x relays provide four independent stages of negative phase sequence overcurrent protection. The first two stages have time-delayed characteristics which are selectable between Inverse Definite Minimum Time (IDMT) and Definite Time (DT). The third and fourth stages have definite time characteristics only. The user may choose to directionalize operation of the elements, for either forward or reverse fault protection for which a suitable relay characteristic angle may be set. Alternatively, the elements may be set as non-directional. For the negative phase sequence directional elements to operate, the relay must detect a polarizing voltage above a minimum threshold, **I2> V2pol Set**.

When the element is selected as directional, a Voltage Transformer Supervision (VTS), Block option is available. When the relevant bit is set to 1, operation of the VTS, will block the stage if directionalized. When set to 0, the stage will revert to non-directional on operation of the VTS.

A timer block input is available for each stage which will reset the NPS overcurrent timers of the relevant stage if energized, (DDB 664-667, 669-672, 674-677). All 4 stages can be blocked by energizing the inhibit DDB signal via the PSL (I2> Inhibit: DDB 663, 668, 673). DDB signals are also available to indicate the start and trip of each stage of protection, (Starts: DDB 1532-1543, Trips: DDB 1154-1165). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

Negative sequence overcurrent protection starts 1/2/3/4 are mapped internally to the ANY START DDB signal - DDB 1312.

The non-directional and directional operation is shown in Figure 29 and Figure 30.

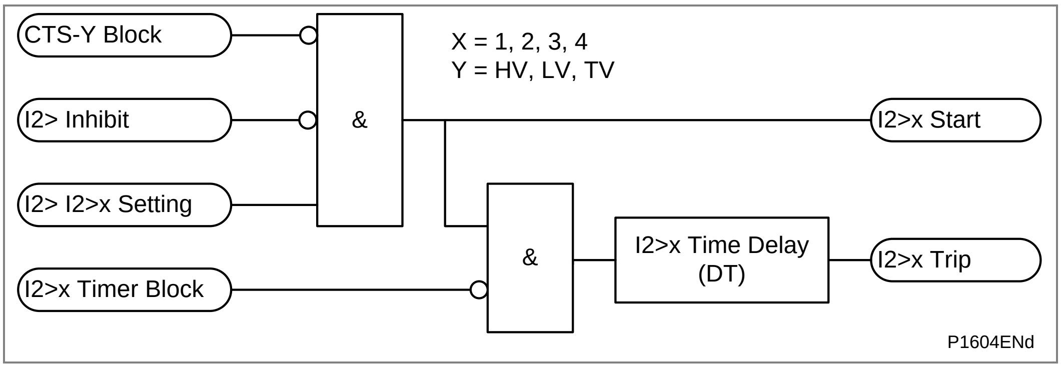
CTS-Y Block
I2> Inhibit
I2> I2>x Setting
I2>x Timer Block
&
X = 1, 2, 3, 4
Y = HV, LV, TV
I2>x Start
&
I2>x Time Delay (DT)
I2>x Trip
P1604ENd

Figure 30 - Negative sequence overcurrent non-directional operation

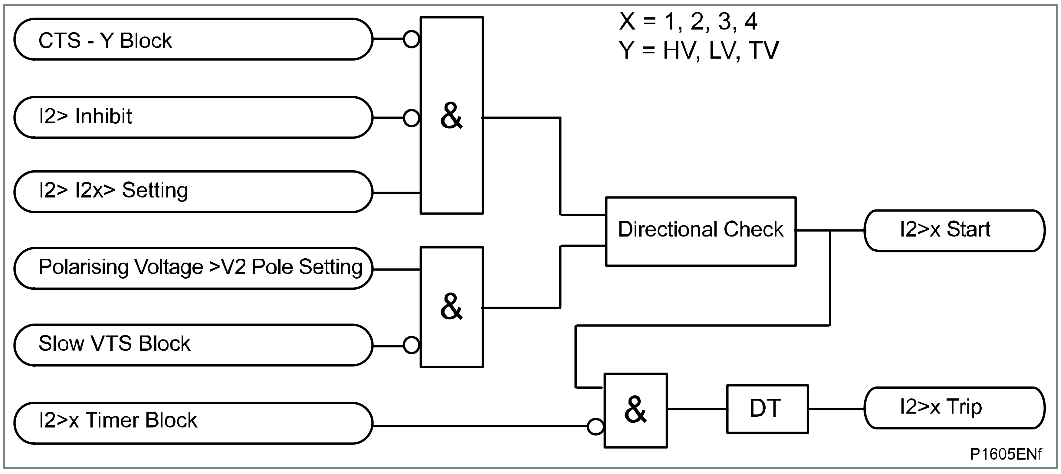
CTS - Y Block
I2> Inhibit
I2> I2x> Setting
Polarising Voltage >V2 Pole Setting
Slow VTS Block
I2>x Timer Block
&
&
X = 1, 2, 3, 4
Y = HV, LV, TV
Directional Check
I2>x Start
&
DT
I2>x Trip
P1605ENf

Figure 31 - Directionalizing the negative phase sequence overcurrent element

Directionality is achieved by comparison of the angle between the negative phase sequence voltage and the negative phase sequence current and the element may be selected to operate in either the forward or reverse direction. A suitable relay characteristic angle setting **I2> Char Angle** is chosen to provide optimum performance.

This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (-V2), in order to be at the center of the directional characteristic.

For the negative phase sequence directional elements to operate, the relay must detect a polarizing voltage above a minimum threshold, **I2> V2pol Set**. This must be set in excess of any steady state negative phase sequence voltage. This may be determined during the commissioning stage by viewing the negative phase sequence measurements in the relay.

2.9 Stub Bus Protection

The stub bus protection is only available in the P643 and P645.

When the protection is used in one and half breaker busbar topology and the disconnector of any of the three windings of the transformer is open, the differential, REF, breaker failure, and differential CTS elements related to this winding are affected.

The differential and REF protections should not trip for a stub bus fault. Therefore, the differential trip may be blocked on a per winding basis if the PSL given in Figure 33 is used. The signals HV StubBus Act (DDB 647), LV StubBus Act (DDB 648) and TV StubBus Act (DDB 649) are asserted when the appropriate conditions are met as shown in Figure 31. The REF is blocked internally on a per winding basis by the fixed logic. For example, if HV StubBus Act (DDB 647) is activated, then HV REF is blocked.

Therefore, the differential and REF protection trips are blocked when the signals HV StubBus Act (DDB 647), LV StubBus Act (DDB 648) and TV StubBus Act (DDB 649) are on.

The stub bus can be protected by a non-directional DT phase overcurrent element with a delay time set to zero seconds. To issue a stub bus trip, the overcurrent element and the StubBus Act DDB signal must assert. This can be configured in the PSL, and it is shown in Figure 31.

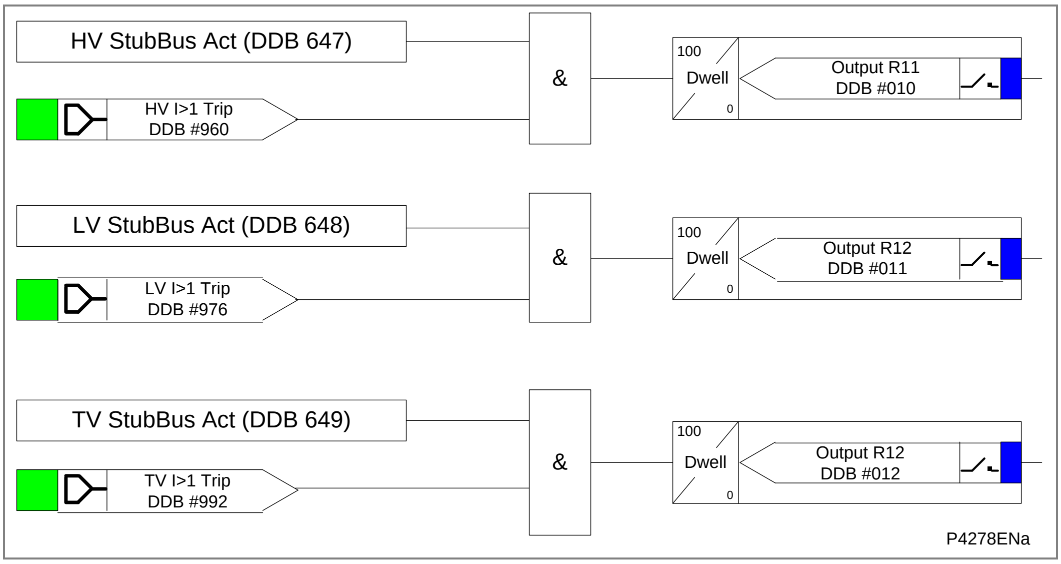
HV StubBus Act (DDB 647)
HV I>1 Trip
DDB #960
&
100
Dwell
0
Output R11
DDB #010
LV StubBus Act (DDB 648)
LV I>1 Trip
DDB #976
&
100
Dwell
0
Output R12
DDB #011
TV StubBus Act (DDB 649)
TV I>1 Trip
DDB #992
&
100
Dwell
0
Output R12
DDB #012
P4278ENa

Figure 32 - Stub bus trip

2.9.1 Inputs

Signal name	Description
IA-1, IB-1, IC-1, IA-2, IB-2, IC-2, IA-3, IB-3, IC-3, IA-4, IB-4, IC-4, IA-5, IB-5, IC-5	Phase current levels (Fourier magnitudes)
HV StubBus En	High voltage stub bus enabled
LV StubBus En	Low voltage stub bus enabled
TV StubBus En	Tertiary voltage stub bus enabled

Table 10 - Inputs

2.9.2 Outputs

Signal name	Description
HV StubBus Act	High voltage stub bus activated
LV StubBus Act	Low voltage stub bus activated
TV StubBus Act	Tertiary voltage stub bus activated
HV UndCurrent	HV undercurrent detection
LV UndCurrent	LV undercurrent detection
TV UndCurrent	TV undercurrent detection

Table 11 - Outputs

2.9.3 Operation

The stub bus activation logic is shown in Figure 32. The inputs HV StubBus En, LV StubBus En and TV StubBus En may be assigned to opto inputs in the PSL. Each opto input is connected to a normally closed auxiliary contact from the HV, LV and TV disconnector respectively. When the opto input is energized and the undercurrent element is asserted, the StubBus Act signal will also be asserted. The outputs of this logic (HV StubBus Act, LV StubBus Act and TV StubBus Act) can be used to change the trip logic and to initiate an indication if necessary.

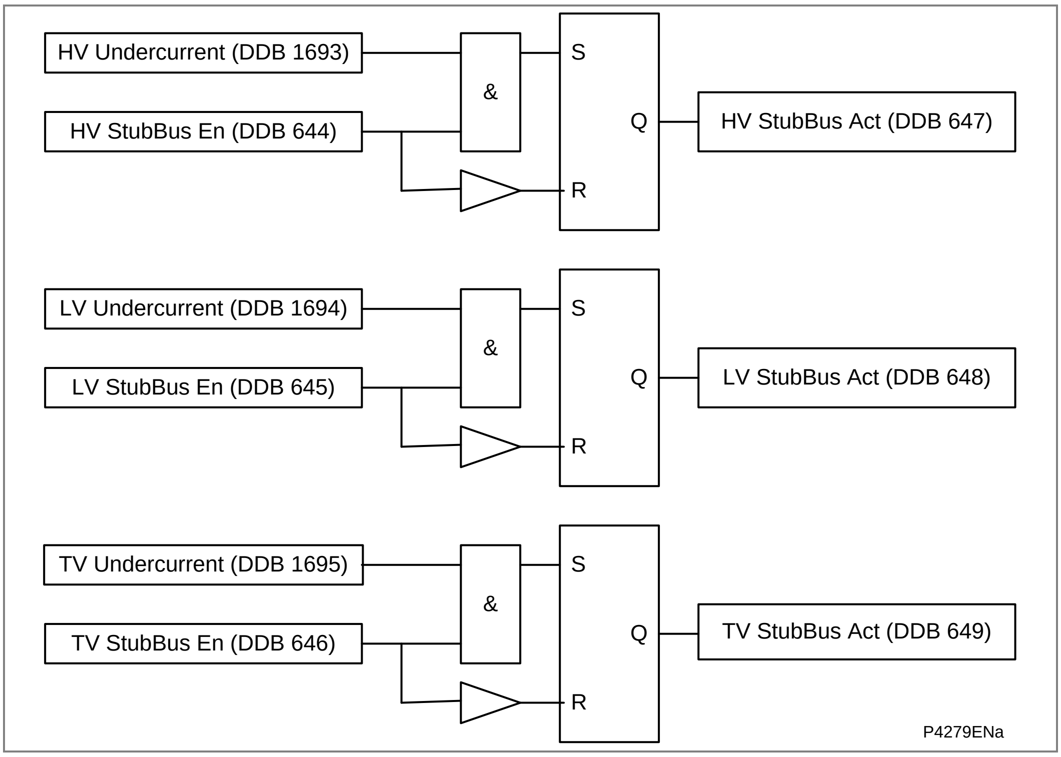
HV Undercurrent (DDB 1693)
HV StubBus En (DDB 644)
&
S
Q
R
HV StubBus Act (DDB 647)
LV Undercurrent (DDB 1694)
LV StubBus En (DDB 645)
&
S
Q
R
LV StubBus Act (DDB 648)
TV Undercurrent (DDB 1695)
TV StubBus En (DDB 646)
&
S
Q
R
TV StubBus Act (DDB 649)
P4279ENa

Figure 33 - Stub bus activation logic

Whenever stub bus is activated, the current signals from the winding whose isolator is open are not taken into consideration in the calculation of the differential and bias currents. For example, if a fault occurs within the protected zone and the low voltage stub bus is activated, the differential element would only trip the breakers connected to the high and tertiary sides of the transformer if the configuration shown in Figure 33 is used. Considering a lockout relay (86) per circuit breaker, the trip output contacts may be configured as shown in Figure 33.

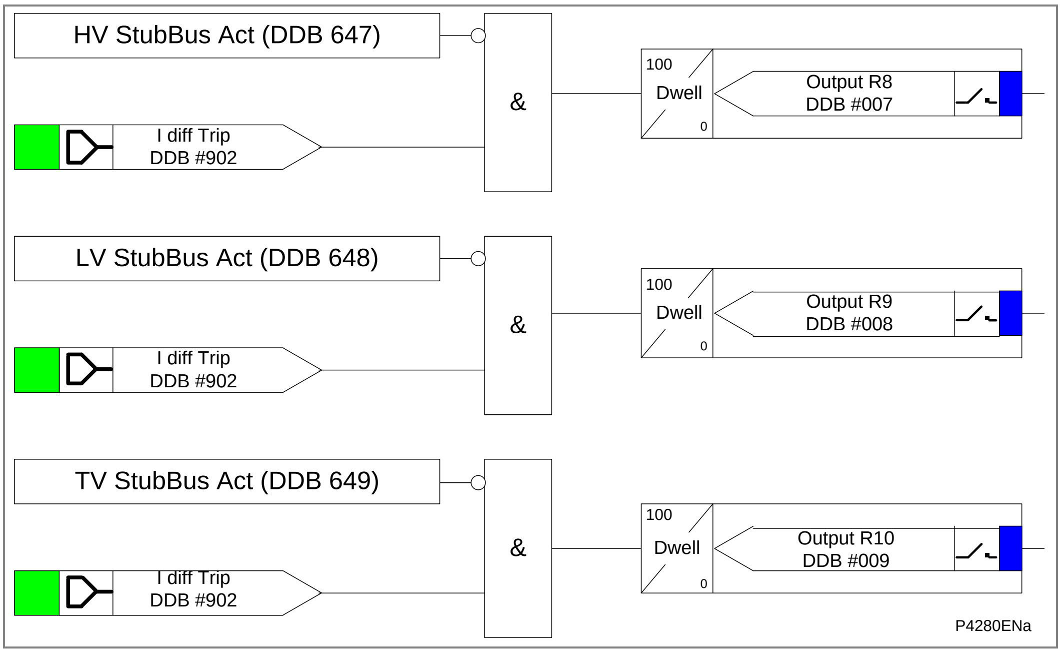
HV StubBus Act (DDB 647)
I diff Trip
DDB #902
&
100
Dwell
0
Output R8
DDB #007
LV StubBus Act (DDB 648)
I diff Trip
DDB #902
&
100
Dwell
0
Output R9
DDB #008
TV StubBus Act (DDB 649)
I diff Trip
DDB #902
&
100
Dwell
0
Output R10
DDB #009
P4280ENa

Figure 34 - Differential trip blocked due to stub bus activation

In applications where the 86 is per differential scheme, it is not possible to apply the logic in Figure 33 since the differential protection trip will be blocked each time any stub bus is activated. Hence, for this application, the stub bus protection can not be used.

The REF protection is internally blocked by the stub bus activation logic on a per winding basis. The CTS is also internally blocked by the stub bus activation logic on a per CT input basis. The breaker failure is not initiated by any general overall trip if the stub bus protection is activated (see section 2.10).

2.10 Circuit Breaker Fail Protection (CBF)

Up to five independent sets of Circuit Breaker Failure (CBF) settings are available. It is possible to set five breaker failure functions in the P645, three in the P643 and two in the P642. One phase and one earth undercurrent element are available per CBF function. The earth undercurrent element can be set as enabled or disabled. When enabled, it can be set as measured or derived. In the P645 and P643, TN1, TN2 and TN3 are single phase CTs that might be used by the CBF function. In the P642, single phase CTs TN1 and TN2 are available. Whenever TN1, TN2 or TN3 is wired to measure the neutral current associated to a particular breaker and **In< Input** is set as measured then TN1, TN2 or TN3 can be set in **In< Terminal**.

When there is a fault and the circuit breaker interrupts the CT primary current, the flux in the CT core decays to a residual level. This decaying flux introduces a decaying DC current in the CT secondary circuit known as subsidence current. The closer the CT is driven to its saturation point, the higher the subsidence current. The time constant of this subsidence current depends on the CT secondary circuit time constant and it is generally long. If the primary/secondary protection clears the fault, then the CBF function should reset fast to avoid operation of the CBF due to the subsidence current. A zero crossing detection algorithm has been implemented so that the CBF re-trip and back-trip signals are not asserted while subsidence current is flowing preventing the undercurrent elements to assert. The zero crossing detection algorithm considers the current inputs T1, T2, T3, T4 and T5 on a per phase basis. If **In< Input** is set as measured, current inputs TN1, TN2 and TN3 are considered by the zero crossing detection algorithm. If **In< Input** is set as derived, the neutral currents derived from T1, T2, T3, T4 and T5 current inputs are considered. If more than 12 consecutive samples are greater than 0A or more than 12 consecutive samples are smaller than 0A, then zero crossing detection is asserted; thus blocking the operation of the CBF. The zero crossing detection is asserted once the breaker in the primary system has opened so that the current flowing in the AC secondary circuit is the subsidence current.

The CBF protection incorporates two timers, CB Fail 1 Timer and CB Fail 2 Timer, allowing configuration for the following situations:

- Simple CBF, where only **CB Fail 1 Timer** is enabled. For any protection trip, the **CB Fail 1 Timer** is started, and normally reset when the circuit breaker opens to isolate the fault.
- If breaker opening is not detected, **CB Fail 1 Timer** times out and closes an output contact assigned to breaker failure (using the programmable scheme logic). This contact is used to backtrip upstream switchgear, generally tripping all infeeds connected to the same busbar section. DDB’s 1528, 1530, 1532, 1534 and 1536 are associated to CBF timer1.
- A re-tripping scheme, plus delayed backtripping. Here, **CB Fail 1 Timer** is used to route a trip to a second trip circuit of the same circuit breaker. This requires duplicated circuit breaker trip coils, and is known as re-tripping. Should re-tripping fail to open the circuit breaker, a backtrip may be issued following an additional time delay. The backtrip uses **CB Fail 2 Timer**, which is also started at the instant of the initial protection element trip. DDB’s 1528, 1530, 1532, 1534 and 1536 are re-trip signals and they are associated to CBF timer1. DDB’s 1529, 1531, 1533, 1535 and 1537 are back-trip signals and they are associated to CBF timer2.
- CBF elements **CB Fail 1 Timer** and **CB Fail 2 Timer** can be configured to operate for trips triggered by protection elements in the relay or using an external protection trip. The latter is achieved by allocating one of the relay opto-isolated inputs to **External Trip** using the programmable scheme logic.

Resetting of the CBF is possible from a breaker open indication (from the relay’s pole dead logic) or from a protection reset. In these cases resetting is only allowed provided the undercurrent elements have also reset. The resetting options are summarized in Table 12:

Initiation (menu selectable)	CB fail timer reset mechanism
Current based protection (e.g. 50/51/46/87.)	The resetting mechanism is fixed. [IA< operates] & [IB< operates] & [IC< operates]
Non-current based protection CBF Non I Reset setting (e.g. 27/59/81)	Three options are available. The user can select from these options. [All I< elements operate] AND [Protection element reset] [All I< elements operate] AND CB open (all 3 poles) [All I< elements operate]
External protection CBF Ext Reset	Three options are available. The user can select any or all of the options. [All I< elements operate] AND [External trip reset] [All I< elements operate] AND CB open (all 3 poles) [All I< elements operate]

Table 12 -Resetting options

If the reset option is set to I<Only, then the INTSIG Latch ResetState signal as shown in Figure 35 is always zero. In this case the zero crossing detection algorithm prevents the re-trip and back-trip signals from asserting.

The breaker failure logic for circuit breaker 1 is shown in Figure 35. The current signals come from T1 CT. Five CBF logics are available in the P645, three in the P643 and two in the P642.

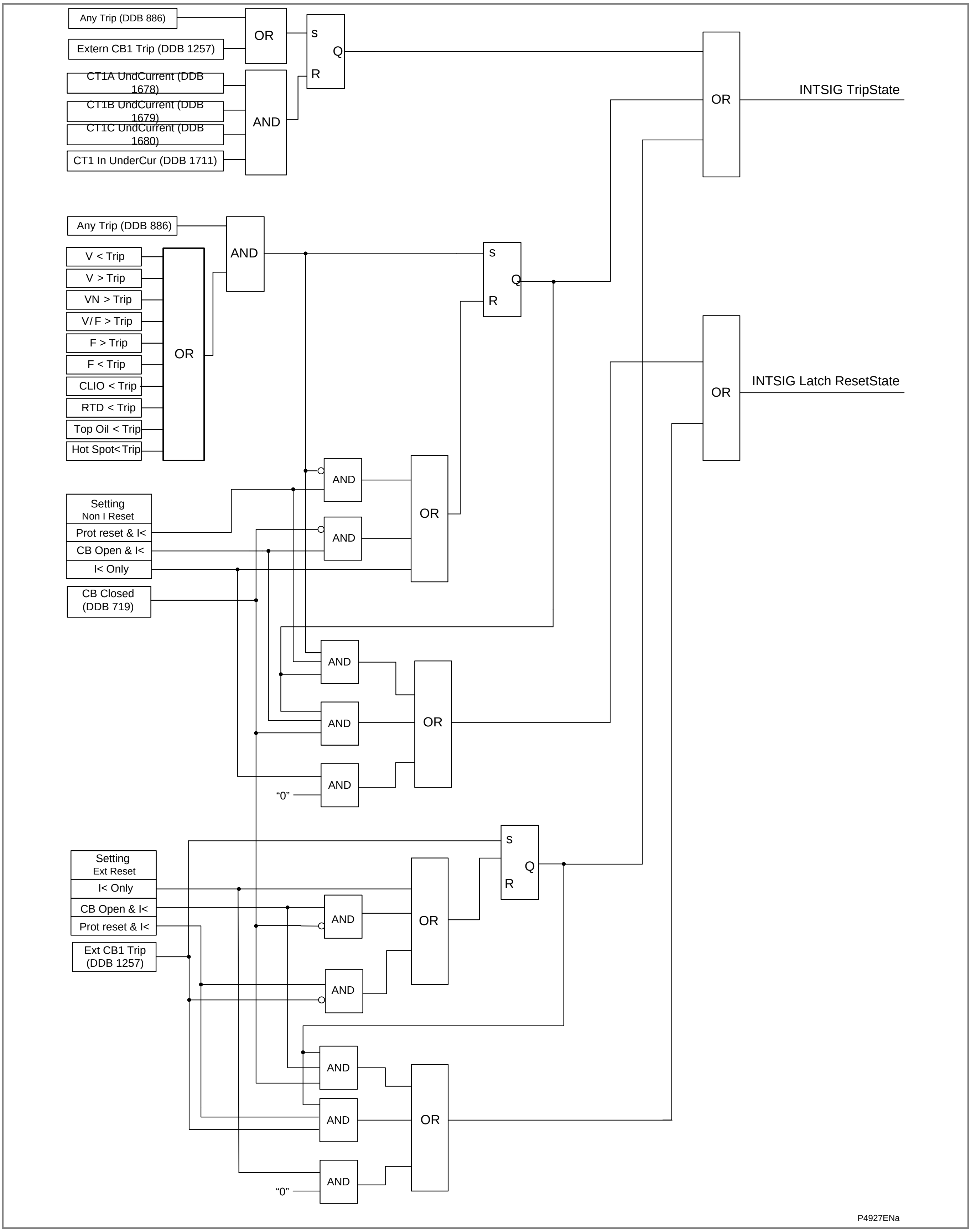
Any Trip (DDB 886)
Extern CB1 Trip (DDB 1257)
OR
S
Q
R
CT1A UndCurrent (DDB 1678)
CT1B UndCurrent (DDB 1679)
CT1C UndCurrent (DDB 1680)
CT1 In UnderCur (DDB 1711)
AND
OR
INTSIG TripState
Any Trip (DDB 886)
AND
V < Trip
V > Trip
VN > Trip
V/F > Trip
F > Trip
F < Trip
CLIO < Trip
RTD < Trip
Top Oil < Trip
Hot Spot< Trip
OR
S
Q
R
OR
INTSIG Latch ResetState
Setting
Non I Reset
Prot reset & I<
CB Open & I<
I< Only
CB Closed (DDB 719)
AND
AND
OR
AND
AND
AND
OR
"0"
Setting
Ext Reset
I< Only
CB Open & I<
Prot reset & I<
Ext CB1 Trip (DDB 1257)
S
Q
R
AND
OR
AND
AND
AND
OR
AND
"0"
P4927ENa

Figure 35 - CB fail logic

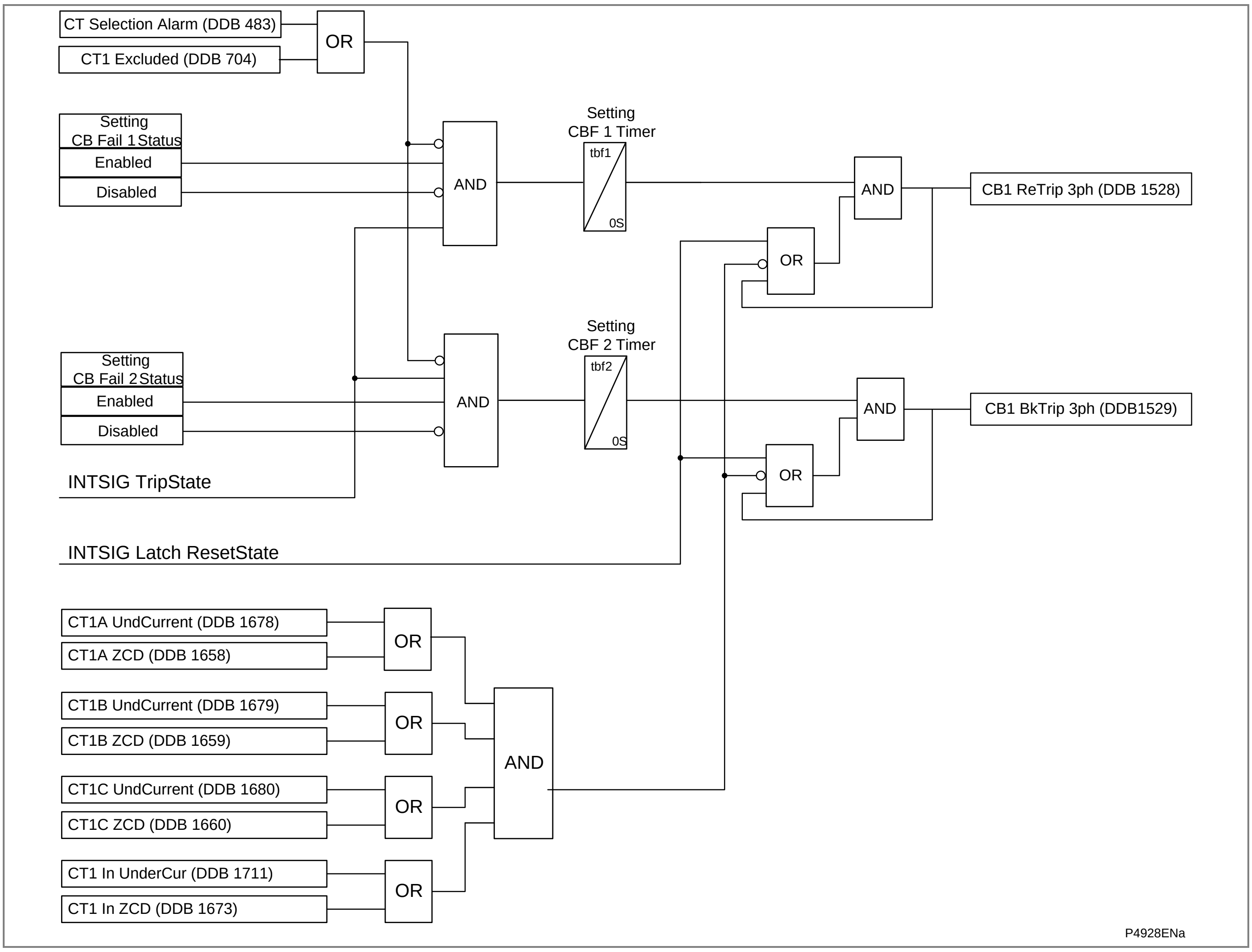
CT Selection Alarm (DDB 483)
CT1 Excluded (DDB 704)
OR
Setting
CB Fail 1 Status
Enabled
Disabled
AND
Setting
CBF 1 Timer
tbf1
0S
AND
CB1 ReTrip 3ph (DDB 1528)
OR
Setting
CB Fail 2 Status
Enabled
Disabled
AND
Setting
CBF 2 Timer
tbf2
0S
AND
CB1 BkTrip 3ph (DDB1529)
OR
INTSIG TripState
INTSIG Latch ResetState
CT1A UndCurrent (DDB 1678)
CT1A ZCD (DDB 1658)
OR
CT1B UndCurrent (DDB 1679)
CT1B ZCD (DDB 1659)
OR
CT1C UndCurrent (DDB 1680)
CT1C ZCD (DDB 1660)
OR
CT1 In UnderCur (DDB 1711)
CT1 In ZCD (DDB 1673)
OR
AND
P4928ENa

Figure 36 - CB fail logic

The waveforms shown in Figure 35 and Figure 35 were injected to the relay. A differential trip is expected and no retrip or backtrip signals should be asserted. Note that a current waveform with maximum offset has been injected; therefore, a high flux level is expected in the CT core.

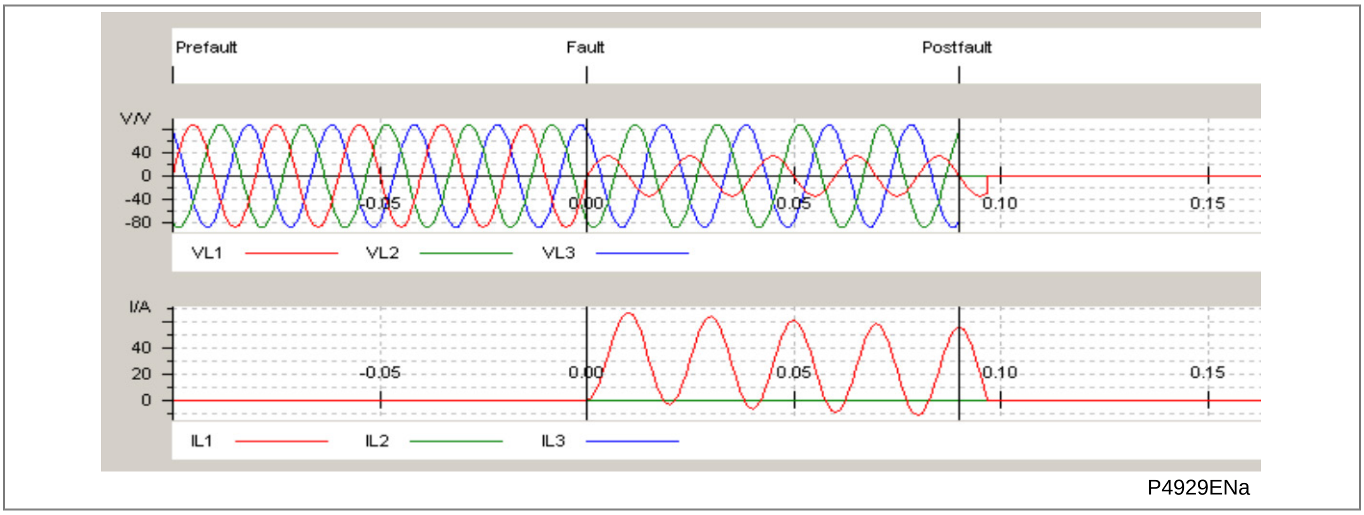

Figure 37 - CBF test - injected waveforms

Figure 37 shows the disturbance record extracted from the relay. The subsidence current in phase A due to the internal CT within the relay can be observed. It takes 15ms approximately for CT1A ZCD to assert once the current is interrupted. Even if CT1A UndCurrent is not asserted, the activation of CB1 BkTrip 3ph is prevented, because CT1A ZCD asserts.

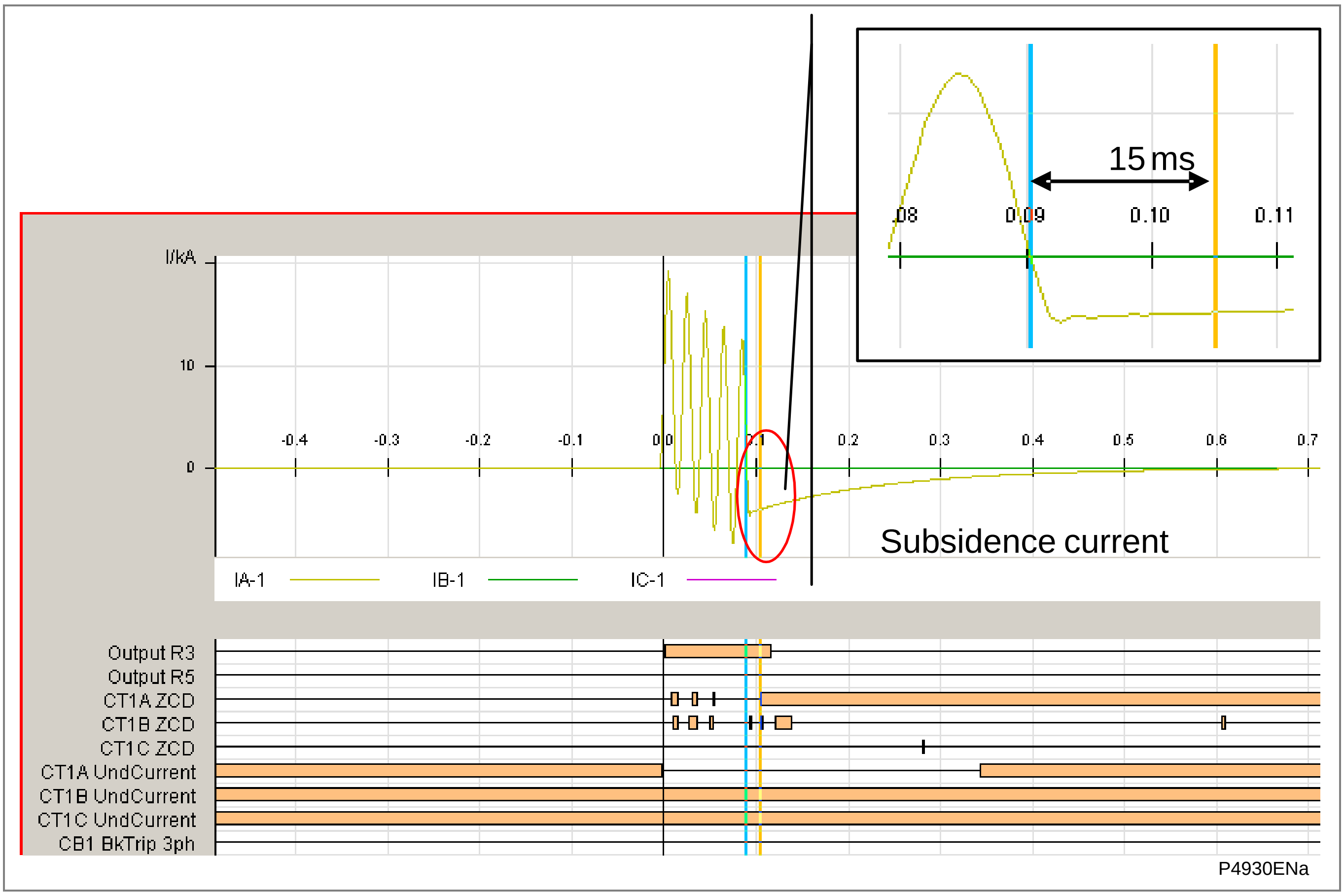

Figure 38 - CBF test - relay disturbance record

2.11 Overvoltage Protection

The overvoltage protection function is in the relay menu **Volt Protection** and it is only included in the P643 and P645 when the 3-phase VT input is available. It consists of two independent stages. These are configurable as either phase to phase or phase to neutral measuring in the **V>Measur't mode** cell.

Stage 1 may be selected as **IDMT**, **DT** or **Disabled**, in the **V>1 Function** cell. Stage 2 is **DT** only and in the **V>2 status** cell can be set as **enabled** or **disabled**.

The IDMT characteristic available on the first stage is defined by the formula:

$t = K/(M - 1)$

Where:
K = Time multiplier setting
t = Operating time in seconds
M = Measured voltage / relay setting voltage (V> Voltage Set)

The logic diagram of the first stage overvoltage function is shown in Figure 38.

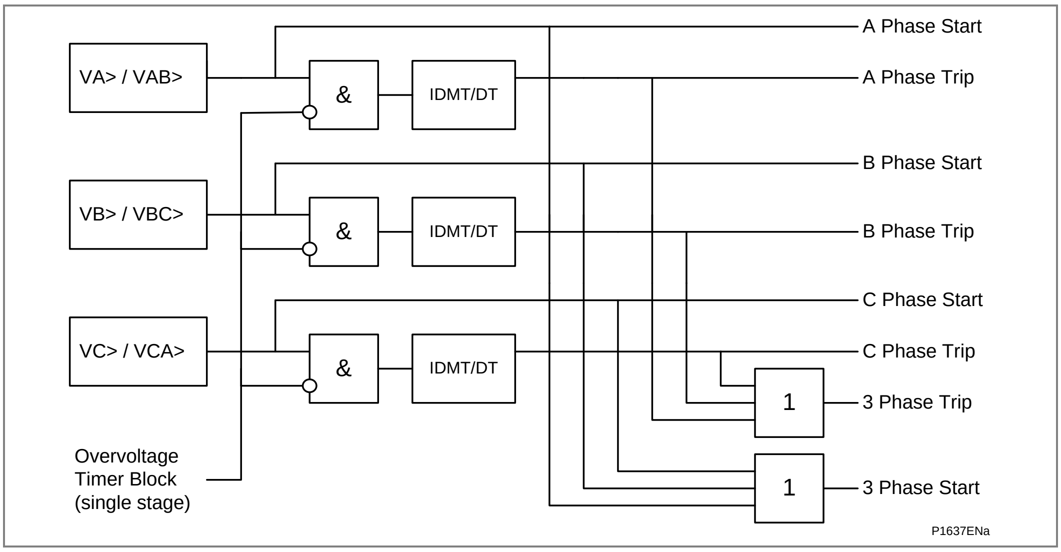
VA> / VAB>
VB> / VBC>
VC> / VCA>
Overvoltage Timer Block (single stage)
&
&
&
IDMT/DT
IDMT/DT
IDMT/DT
1
1
A Phase Start
A Phase Trip
B Phase Start
B Phase Trip
C Phase Start
C Phase Trip
3 Phase Trip
3 Phase Start
P1637ENa

Figure 39 - Overvoltage logic diagram (single stage)

2.12 Negative Sequence Overvoltage

One definite time stage of negative sequence overvoltage is available in the P643 and P645 when the three phase VT option is fitted. This function is also available in the P642 when two single phase VTs are fitted. The negative sequence overvoltage element may be enabled/disabled within the **V2>status** cell.

In the P642, phase-to-phase voltages V_{ab} and V_{bc} are required, and the relay calculates the negative sequence voltage as $\frac{\vec{V}_{ab} - a\vec{V}_{bc}}{3}$. Where $a = 1\angle 120^{\circ} = -0.5 + j0.866$.

The logic diagram for the negative sequence overvoltage protection is shown in Figure 39:

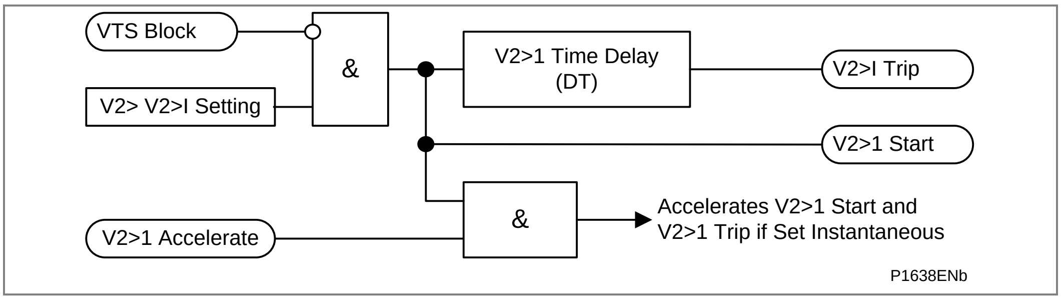
VTS Block
V2> V2>I Setting
&
V2>1 Time Delay (DT)
V2>I Trip
V2>1 Start
&
V2>1 Accelerate
Accelerates V2>1 Start and V2>1 Trip if Set Instantaneous
P1638ENb

Figure 40 - Negative sequence overvoltage logic diagram

DDB signals are available to indicate a start and a trip, (Start: DDB 1622, Trip: DDB 1215). There is also a signal to accelerate the NPS overvoltage protection start (V2>1 Accelerate: DDB 663) which accelerates the operating time of the function from typically 80 ms to 40 ms when set to instantaneous.

The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the COMMISSION TESTS column in the relay.

2.13 Undervoltage Protection

The undervoltage protection function is in the relay menu **Volt Protection**, and it is only included in the P643 and P645 when the 3-phase VT input is available It consists of two independent stages. These are configurable as either **phase-to-phase** or **phase-to -neutral** measuring in the **V<Measur't mode** cell.

Stage 1 may be selected as **IDMT**, **DT** or **Disabled**, in the **V<1 Function** cell. Stage 2 is **DT** only and in the **V<2 status** cell it can be is **enabled** or **disabled**.

The IDMT characteristic available on the first stage is defined by the following formula:

t = K/(1 - M)

Where:

K = Time multiplier setting

t = Operating time in seconds

M = Measured voltage/relay setting voltage (V< Voltage Set)

Two stages are included to provide both alarm and trip stages, where required. Alternatively, different time settings may be required depending upon the severity of the voltage dip, for example, motor loads will be able to withstand a small voltage depression for a longer time than if a major voltage excursion were to occur.

Outputs are available for single or three-phase conditions using the **V<Operate Mode** cell.

The logic diagram of the first stage undervoltage function is shown in Figure 40.

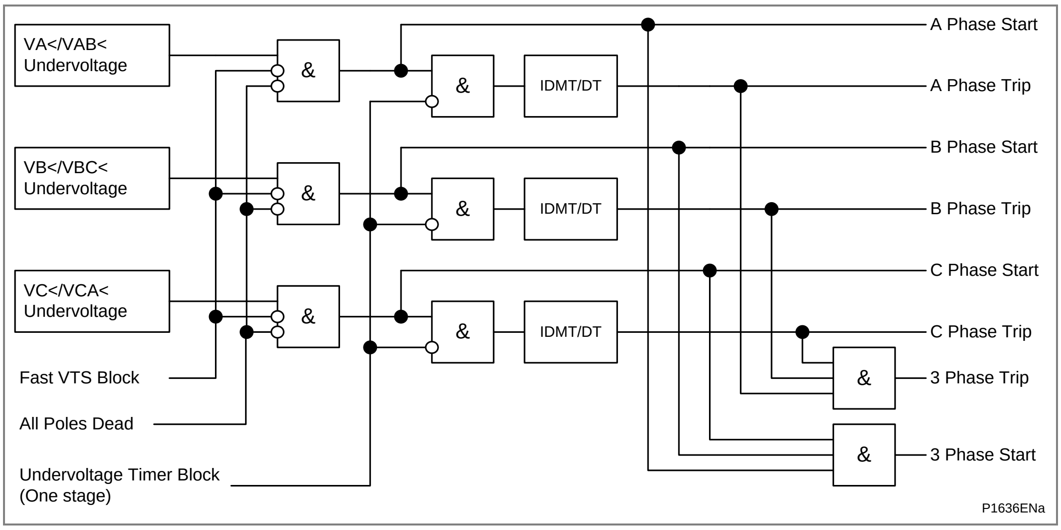
VA</VAB< Undervoltage
VB</VBC< Undervoltage
VC</VCA< Undervoltage
Fast VTS Block
All Poles Dead
Undervoltage Timer Block (One stage)
&
IDMT/DT
A Phase Start
A Phase Trip
B Phase Start
B Phase Trip
C Phase Start
C Phase Trip
3 Phase Trip
3 Phase Start
P1636ENa

Figure 41 - Undervoltage logic diagram (single stage)

When the protected feeder is de-energized, or the circuit breaker is opened, an undervoltage condition would be detected. Therefore, the **V<Poledead Inh** cell is included for each of the two stages to block the undervoltage protection from operating for this condition. If the cell is enabled, the relevant stage will become inhibited by the in-built pole dead logic in the relay. This logic produces an output when it detects either an open circuit breaker through auxiliary contacts feeding the relay opto inputs or it detects a combination of both undercurrent and undervoltage on any one phase.

2.14 Residual Overvoltage (Neutral Displacement) Protection

The residual overvoltage protection is included in the P643 and P645 when the 3-phase VT input is available.

On a healthy three-phase power system, the addition of each of the three phase to earth voltages is nominally zero, as it is the vector addition of three balanced vectors at 120° to one another. However, when an earth fault occurs on the primary system this balance is upset and a ‘residual’ voltage is produced. This could be measured, for example, at the secondary terminals of a voltage transformer having a “broken delta” secondary connection. Hence, a residual voltage-measuring relay can be used to offer earth fault protection on such a system. Note that this condition causes a rise in the neutral voltage with respect to earth that is commonly referred to as “neutral voltage displacement” or NVD.

The detection of a residual overvoltage condition is an alternative means of earth fault detection, which does not require any measurement of current. This may be particularly advantageous in high impedance earthed or insulated systems, where the provision of core balance CTs on each feeder may be either impractical, or uneconomic.

The P64x relay internally derives this residual voltage from the three-phase voltage input that must be supplied from either a 5-limb or three single-phase VTs. The NVD element in the P64x relays is a two-stage design, each stage having separate voltage and time delay settings. Stage 1 may be set to operate on either an IDMT or DT characteristic, while stage 2 may be set to DT only.

The IDMT characteristic available on the first stage is defined by the following formula:

$t = K/(M - 1)$

Where:

K = Time multiplier setting

t = Operating time in seconds

M = Derived residual voltage/relay setting voltage (VN> Voltage Set)

Two stages are included for the NVD protection to account for such applications that require both alarm and trip stages, for example, an insulated system. It is common in such a case for the system to have been designed to withstand the associated healthy phase overvoltages for a number of hours following an earth fault. In such applications, an alarm is generated soon after the condition is detected, which serves to indicate the presence of an earth fault on the system. This gives time for system operators to locate and isolate the fault. The second stage of the protection can issue a trip signal if the fault condition persists.

The functional block diagram of the first stage residual overvoltage is shown in Figure 41:

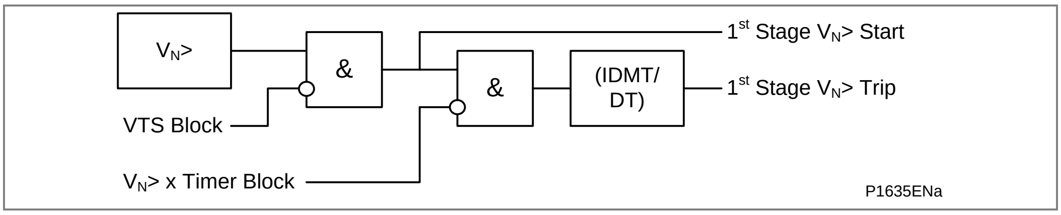

Figure 42 - Residual overvoltage logic (single stage)

VTS blocking when asserted, effectively blocks the start outputs.

When enabled, these signals are set by the residual overvoltage logic according to the status of the monitored function:

VN>1 Start	(DDB 1596)	1st Stage Residual Overvoltage Start
VN>2 Start	(DDB 1597)	2nd Stage Residual Overvoltage Start
VN>1 Timer Blk	(DDB 566)	Block Residual Overvoltage Stage 1 Time Delay
VN>2 Timer Blk	(DDB 567)	Block Residual Overvoltage Stage 2 Time Delay
VN>1 Trip	(DDB 1238)	1st Stage Residual Overvoltage Trip
VN>2 Trip	(DDB 1239)	2nd Stage Residual Overvoltage Trip

2.15 Frequency Protection

The P64x relay includes 4 stages of underfrequency and 2 stages of overfrequency protection to facilitate load shedding and subsequent restoration. All the stages can be **enabled** or **disabled** in the **F<n Status** or **F>n Status** cell, depending on which element is selected.

The logic diagram for the underfrequency logic is as shown in Figure 42. Only a single stage is shown. The other three stages are identical in functionality.

If the frequency is below the setting and not blocked, then the DT timer is started. Blocking may come from the underfrequency timer block.

If the frequency cannot be determined, the function is also blocked.

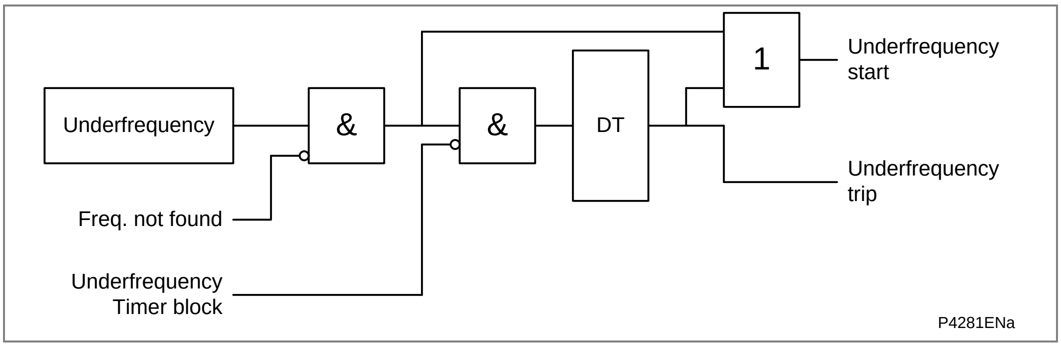
Underfrequency
&
&
DT
1
Underfrequency start
Underfrequency trip
Freq. not found
Underfrequency Timer block
P4281ENa

Figure 43 - Underfrequency logic (single stage)

The functional logic diagram for the overfrequency function is shown in Figure 43. Only a single stage is shown as the other stages are identical in functionality. If the frequency is above the setting and not blocked, the DT timer is started and after this has timed out the trip signal is issued.

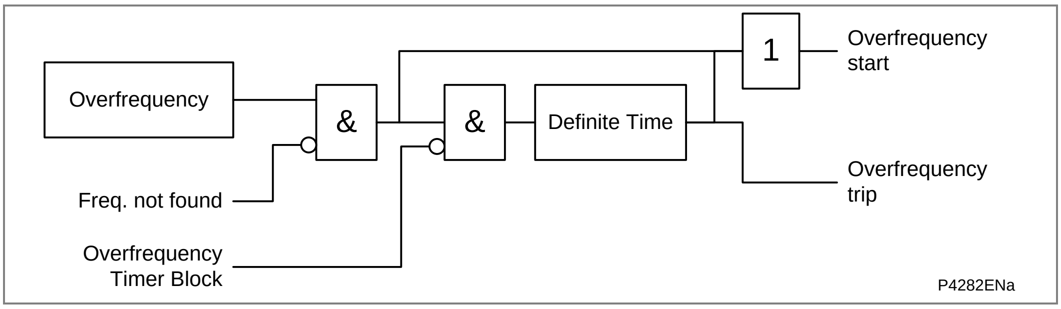
Overfrequency
&
&
Definite Time
1
Overfrequency start
Overfrequency trip
Freq. not found
Overfrequency Timer Block
P4282ENa

Figure 44 - Overfrequency logic (single stage)

When enabled, the following signals are set by the under/overfrequency logic according to the status of the monitored functions.

Freq. Not Found	(DDB 1753)	Frequency Not Found by frequency tracking
F<1 Timer Block	(DDB 638)	Block Underfrequency Stage 1 Timer
F<2 Timer Block	(DDB 639)	Block Underfrequency Stage 2 Timer
F<3 Timer Block	(DDB 640)	Block Underfrequency Stage 3 Timer
F<4 Timer Block	(DDB 641)	Block Underfrequency Stage 4 Timer
F>1 Timer Block	(DDB 642)	Block Overfrequency Stage 1 Timer
F>2 Timer Block	(DDB 643)	Block Overfrequency Stage 2 Timer
F<1 Start	(DDB 1608)	Underfrequency Stage 1 Start
F<2 Start	(DDB 1609)	Underfrequency Stage 2 Start

Freq. Not Found	(DDB 1753)	Frequency Not Found by frequency tracking
F<3 Start	(DDB 1610)	Underfrequency Stage 3 Start
F<4 Start	(DDB 1611)	Underfrequency Stage 4 Start
F>1 Start	(DDB 1612)	Overfrequency Stage 1 Start
F>2 Start	(DDB 1613)	Overfrequency Stage 2 Start
F<1 Trip	(DDB 1230)	Underfrequency Stage 1 Trip
F<2 Trip	(DDB 1231)	Underfrequency Stage 2 Trip
F<3 Trip	(DDB 1232)	Underfrequency Stage 3 Trip
F<4 Trip	(DDB 1233)	Underfrequency Stage 4 Trip
F>1 Trip	(DDB 1228)	Overfrequency Stage 1 Trip
F>2 Trip	(DDB 1229)	Overfrequency Stage 2 Trip

Table 13 - Signals logic

2.16 Thermal Overload Protection (49)

Transformer thermal overload protection is designed to protect the equipment from sustained overload that results in the machine's thermal rating being exceeded. Thermal overload protection compliments the transformer overcurrent protection by allowing modest but transient overload conditions to occur, while tripping for sustained overloads that the overcurrent protection will not detect.

The thermal overload function is based on the IEEE Standard C57.91-1995. This function can be enabled or disabled in the setting or it can be blocked in the PSL. Two three-stage definite time-delayed trip elements based on hot spot or top oil temperature are available. A pre-trip alarm is offered in the tPre-trip Set setting. This alarm indicates that thermal overload will trip after the settable time if load level remains unchanged. Four cooling modes are available, and the oil exponent and winding exponent can be set independently for each mode. The cooling mode selection can be done automatically via PSL or manually in the setting file. Two opto inputs must be configured as CM Select 1X (DDB 709) and CM Select X1 (DDB 710) in PSL and the appropriate contacts must be wired to energize/de-energize these inputs. The selected cooling mode would vary as indicated below:

CM Select 1X (DDB 709)	CM Select X1 (DDB 710)	Selected Cooling Mode
0	0	1
0	1	2
1	0	3
1	1	4

Table 14 - Selected cooling modes

The monitor winding can be set to HV, LV, TV or biased current. If the monitor winding is set to HV and the HV breaker is open, then the current flows from LV to TV. Likewise, if the monitor winding is set to LV and the LV breaker is open, then the current flows from HV to TV. If the monitor winding is set to biased current an overall through loading picture of the transformer is provided.

To calculate the top oil and hot spot winding temperature, the relay takes into consideration the ratio of the ultimate load to the rated load. The rated load is determined by the IB and the rating settings. When the monitored winding is set as the HV winding, the rated load is calculated using the HV Rating and the IB settings. When the monitored winding is set as the LV winding, the rated load is calculated using the LV Rating and the IB settings. When the monitored winding is set as the TV winding, the rated load is calculated using the TV Rating and the IB settings. When the monitored winding is set as the biased current, the rated load is calculated using the REF Power S and the IB settings. The ultimate load is the load that is actually being fed by the transformer.

The biased current used by the thermal protection is not the same as the biased current used by the differential protection. No vector correction or zero sequence filtering is taken into account. To calculate the bias current, the thermal element considers the maximum rms current on a per winding basis. Note that the bias current calculation performed by the thermal element is not on a per-phase basis. The thermal bias current calculation is as follows:

$$I_{bias} = \frac{\frac{\mathrm{Max}\left[I_{HVArms}, I_{HVBrms}, I_{HVCrms}\right]}{HV\_FLC_{Sref}} + \frac{\mathrm{Max}\left[I_{LVArms}, I_{LVBrms}, I_{LVCrms}\right]}{LV\_FLC_{Sref}} + \frac{\mathrm{Max}\left[I_{TVArms}, I_{TVBrms}, I_{TVCrms}\right]}{TV\_FLC_{Sref}}}{2}$$

Where:

HV_FLC_{Sref} = HV full load current at the reference power

LV_FLC_{Sref} = LV full load current at the reference power

TV_FLC_{Sref} = TV full load current at the reference power

The thermal overload model is executed once every power cycle. The thermal overload trip can be based on either hot spot temperature or top oil temperature, or both.

2.16.1 Inputs

Signal name	Description
IA-HV, IB-HV, IC-HV, IA-LV, IB-LV, IC-LV, IA-TV, IB-TV, IC-TV	Phase current levels (raw samples). The currents required by the thermal overload element are the currents of the winding being monitored.
IA-bias, IB-bias, IC-bias	Bias currents
Θ_{TO}	Measured top oil temperature
Θ_{A}	Measured ambient temperature
Reset thermal (DDB 888)	Reset thermal overload
TRF De-energized (DDB 878)	Transformer de-energized. If it is asserted, the transformer no-load losses are not considered.
CM Select 1X (DDB 709)	CM Select 1X is used together with CM Select X1 to configure the cooling mode selector in PSL. This selector allows choosing one of four cooling modes.
CM Select X1 (DDB 710)	CM Select 1X is used together with CM Select X1 to configure the cooling mode selector in PSL. This selector allows choosing one of four cooling modes.

Table 15 - Inputs

2.16.2 Outputs

Signal name	Description
Top oil >1 start (DDB 1337)	Top oil first stage start
Top oil >2 start (DDB 1338)	Top oil second stage start
Top oil >3 start (DDB 1339)	Top oil third stage start
Top oil >1 trip (DDB 957)	Top oil first stage trip
Top oil >2 trip (DDB 958)	Top oil second stage trip
Top oil >3 trip (DDB 959)	Top oil third stage trip
Hot spot >1 start (DDB 1334)	Hot spot first stage start
Hot spot >2 start (DDB 1335)	Hot spot second stage start
Hot spot >3 start (DDB 1336)	Hot spot third stage start
Hot spot >1 trip (DDB 954)	Hot spot first stage trip

Signal name	Description
Hot spot >2 trip (DDB 955)	Hot spot second stage trip
Hot spot >3 trip (DDB 956)	Hot spot third stage trip
Pre-trip alarm (DDB 478)	Thermal pre-trip alarm
Ambient T	Ambient temperature measurement
Top oil T	Top oil temperature measurement
Hot spot T	Hot spot temperature measurement
TOL Pre-trip left	Pre-trip time left measurement

Table 16 - Outputs

2.16.3 Operation

The thermal overload protection in the P64x uses the thermal model given by the equations for hot spot and top oil temperatures. A discrete time thermal replica model is implemented and it is described by the equations for $\Delta\Theta_{TOn}$ and $\Delta\Theta_{Hn}$.

If the top oil temperature is not available as a measured input quantity, it is calculated every cycle by the following equation:

$$\Theta_{TO} = \Theta_A + \Delta\Theta_{TO}$$

Where:

Θ_{TO} = Top oil temperature

Θ_A = Ambient temperature

$\Delta\Theta_{TO}$ = Top oil rise over ambient temperature due to a step load change

The ambient temperature can be measured directly or it can be set in the Average Amb T setting. $\Delta\Theta_{TO}$ is given by the following exponential expression containing an oil time constant:

$$\Delta\Theta_{TOn} = \left(\Delta\Theta_{TO,U} - \Delta\Theta_{TO,n-1}\right)\cdot\left(1 - e^{-\left(\frac{\Delta t}{\tau_{TO}}\right)}\right) + \Delta\Theta_{TO,n-1}$$

Where:

$\Delta\Theta_{TO,U}$ = ultimate top oil rise over ambient temperature for load L

$\Delta\Theta_{TO,n-1}$ = the previous top oil rise over ambient temperature

Δt = elapsed time between the ultimate top oil rise and the initial top oil rise

τ_{TO} = oil time constant of the transformer for any load L between the ultimate top oil rise and the initial top oil rise. This parameter is set by the user.

By using power series, top oil rise, $\Delta\Theta_{TOn}$, can be approximated as shown below:

$$\Delta\Theta_{TOn} = \left(\Delta\Theta_{TO,U} - \Delta\Theta_{TO,n-1}\right)\cdot\left(\frac{\Delta t}{\tau_{TO}}\right) + \Delta\Theta_{TO,n-1}$$

If the oil exponent n is less than 1, the top oil time constant τ_{TO} is corrected using the following equation:

$$\tau_{\text{TOcorrected}} = \tau_{\text{TO}} \times \frac{\left(\frac{\Delta\Theta_{\text{TO,U}}}{\Delta\Theta_{\text{TO,R}}}\right) - \left(\frac{\Delta\Theta_{\text{TO,n-1}}}{\Delta\Theta_{\text{TO,R}}}\right)}{\left(\frac{\Delta\Theta_{\text{TO,U}}}{\Delta\Theta_{\text{TO,R}}}\right)^{\frac{1}{n}} - \left(\frac{\Delta\Theta_{\text{TO,n-1}}}{\Delta\Theta_{\text{TO,R}}}\right)^{\frac{1}{n}}}$$

Where:

τ_{TO} = oil time constant of the transformer for any load L between the ultimate top oil rise and the initial top oil rise. This parameter is set by the user.

$\Delta\Theta_{TO,U}$ = ultimate top oil rise over ambient temperature for load L.

$\Delta\Theta_{TO,n-1}$ = the previous top oil rise over ambient temperature.

n = Oil exponent. This parameter is set by the user.

The ultimate top oil rise is given by the following equation:

$$\Delta\Theta_{TO,U} = \Delta\Theta_{TO,R} \cdot \left[\frac{K_u^2 R + 1}{R + 1}\right]^n$$

Where:

K_u= the ratio of ultimate load L to rated load

R = the ratio of the load loss at rated load to no load loss. This parameter is set by the user.

n = Oil exponent. This parameter is set by the user.

$\Delta\Theta_{TO,R}$ = top oil rise over ambient temperature at rated load. This parameter is set by the user.

The hot spot temperature can only be obtained by calculation. The following equation is used to calculate the hot spot temperature every cycle:

$$\Theta_H = \Theta_{TO} + \Delta\Theta_H$$

Where:

Θ_H = Hot spot (winding) temperature

Θ_{TO} = Top oil temperature

$\Delta\Theta_H$ = Hot spot rise above top oil temperature

The hot spot temperature rise over top oil temperature, $\Delta_{\Theta H}$, is given by:

$$\Delta\Theta_{Hn} = \left(\Delta\Theta_{H,U} - \Delta\Theta_{H,n-1}\right) \cdot \left(1 - e^{-\left(\frac{\Delta t}{\tau_w}\right)}\right) + \Delta\Theta_{H,n-1}$$

Where:

$\Delta\Theta_{H,U}$ = ultimate hot spot rise over top oil temperature for load L

$\Delta\Theta_{H,n-1}$ = previous hot spot rise over top oil temperature

Δt = elapsed time between the ultimate hot spot rise and the initial hot spot rise. Δt is one cycle.

τ_W = winding time constant at hot spot location. This parameter is set by the user.

By using power series, hot spot temperature rise, $\Delta\Theta_{Hn}$, can be approximated as shown below:

$$\Delta\Theta_{Hn} = \left(\Delta\Theta_{H,U} - \Delta\Theta_{H,n-1}\right)\cdot\left(\frac{\Delta t}{\tau_w}\right) + \Delta\Theta_{H,n-1}$$

The ultimate hot spot rise over top oil is given by:

$$\Delta\Theta_{H,U} = \Delta\Theta_{H,R}\cdot K_U{}^{2m}$$

Where:

$\Delta\Theta_{H,R}$ = winding hottest spot rise over top oil temperature at rated load. This parameter is set by the user.

K_U = the ratio of ultimate load L to rated load

m = winding exponent. This parameter is set by the user.

The load current used in the calculations is the rms value. The rms current is calculated according to the following equation:

$$L_{rms} = \sqrt{\frac{L_1{}^2 + L_2{}^2 + \ldots + L_{24}{}^2}{24}}$$

Where L_n is the sample, there are 24 sample per cycle.

Hot spot temperature, Top oil temperature and ambient temperature are stored in non-volatile memory. These measurements are updated every power cycle. The thermal state can be reset to zero by any of the following:

- The **Reset Thermal** cell under the **MEASUREMENT 3** heading on the front panel
- A remote communications interface command
- A status input state change.

The top oil temperature, hot spot temperature, ambient temperature and pre-trip time left are available as a measured value in the **Measurement 3** column.

If a more accurate representation of the thermal state of the transformer is required, the use of temperature monitoring devices (RTDs or CLIO) which target specific areas is recommended. Also, for short time overloads the application of RTDs/CLIO and overcurrent protection can provide better protection.

The transformer de-energized signal (DDB 878) has been configured in the default PSL logic. It is asserted when all the breakers are open. If this signal is asserted, the transformer no-load losses are not considered. As a result, the top oil and hottest spot temperatures are equal to the ambient temperature when the monitored current is zero. If this signal is de-asserted, the top oil and hottest spot temperatures are not equal to the ambient temperature even when the monitored current is zero. In this case the top oil and hottest spot temperatures will increase according to the equations described above.

2.17 Loss Of Life (LOL) Statistics

Deterioration of insulation is a time function of temperature. Since the temperature distribution is not uniform, the part that is operating at the highest temperature undergoes the greatest deterioration. Therefore, the hot spot temperature is considered in loss of life statistics. The Loss Of Life (LOL) model is executed once every cycle.

Two one-stage definite time delay alarm based on aging acceleration factor (F_{AA}) or LOL are available.

A reset command is provided to allow the user to reset the calculated parameters: LOL status, LOL aging factor (F_{AA}), mean aging factor ($F_{AA.m}$), Rate Of Loss Of Life (ROLOL), residual life at F_{AAm} (Lres at FAA,m), residual life at designed (Lres at designed).

2.17.1 Inputs

Signal name	Description
IA-HV, IB-HV, IC-HV, IA-LV, IB-LV, IC-LV, IA-TV, IB-TV, IC-TV	Phase current levels (raw samples). The currents required by the thermal overload element are the currents of the winding being monitored.
IA-bias, IB-bias, IC-bias	Bias currents
Θ_H	Calculated hot spot temperature
Reset LOL	Reset loss of life

Table 17 - Inputs

2.17.2 Outputs

Signal name	Description
FAA Alarm	Aging acceleration factor alarm
LOL Alarm	Loss of life alarm
LOL status	Accumulated loss of life (LOL) measurement in hrs
L_{res} at designed	Residual life at reference hottest spot temperature
Rate of LOL	Rate of loss of life (ROLOL) measurement in %
LOL aging factor	Aging acceleration factor (F_{AA}) measurement
$F_{AA,m}$	Mean aging acceleration factor ($F_{AA,m}$) measurement
L_{res} at $F_{AA,m}$	Residual life hours at $F_{AA,m}$ ($L_{res}(F_{AA,m})$) measurement

Table 18 - Outputs

2.17.3 Operation

As indicated in IEEE Std. C57.91-1995 the aging acceleration factor is the rate at which transformer insulation aging for a given hottest spot temperature is accelerated compared with the aging rate at a reference hottest spot temperature. For 65°C average winding rise transformers, the reference hottest spot temperature is 110°C. For 55°C average winding rise transformers, the reference hottest spot temperature is 95°C. For hottest spot temperatures in excess of the reference hottest spot temperature the aging acceleration factor is greater than 1. For hottest spot temperatures lower than the reference hottest spot temperature, the aging acceleration factor is less than 1.

The model used for loss of life statistics is given by the equations for LOL and F_{AA}. LOL is calculated every hour according to the following formula:

$$LOL = L(\Theta_{H,r}) - L_{res}(\Theta_{H,r})$$

Where:

$L(\Theta_{H,r})$ = life hours at reference winding hottest-spot temperature. This parameter is set by the user.

$L_{res}(\Theta_{H,r})$ = residual life hours at reference winding hottest-spot temperature

The aging acceleration factor F_{AA} is calculated once every cycle as follows:

$$F_{AA} = \frac{L(\Theta_{H,r})}{L(\Theta_H)} = \frac{e^{\left[A+\frac{B}{\Theta_{H,r}+273}\right]}}{e^{\left[A+\frac{B}{\Theta_H+273}\right]}} = e^{\left[\frac{B}{\Theta_{H,r}+273}-\frac{B}{\Theta_H+273}\right]}$$

If a 65°C average winding rise transformer is considered, the equation for F_{AA} is as follows:

$$F_{AA} = e^{\left[\frac{B}{383}-\frac{B}{\Theta_H+273}\right]}$$

If a 55°C average winding rise transformer is considered, the equation for F_{AA} is as follows:

$$F_{AA} = e^{\left[\frac{B}{368}-\frac{B}{\Theta_H+273}\right]}$$

Where:

$L(\Theta_H)$ = life hours at winding hottest-spot temperature

Θ_H = hottest-spot temperature as calculated in thermal overload protection

$\Theta_{H,r}$ = hottest-spot temperature at rated load.

B = constant B from life expectancy curve. This parameter is set by the user. IEEE Std. C57.91-1995 recommends a B value of 15000.

The residual life hours at reference hottest-spot temperature is updated every hour as follows:

$$L_{res}(\Theta_{H,r}) = L_{res,p}(\Theta_{H,r}) - \frac{\sum_{i=1}^{3600} F_{AA,i}(\Theta_H)}{3600}$$

Where:

$L_{res,p}(\Theta_{H,r})$ = residual life hours at reference temperature one hour ago

$F_{AA,i}(\Theta_H)$ = Mean aging acceleration factor, as calculated above. It is calculated every second.

The accumulated loss of life (LOL) will be updated in non-volatile memory once per hour. It will be possible to reset and set a new loss of life figure, in the event that a relay is applied in a new location with a pre-aged resident transformer.

The rate of loss of life (ROLOL) in percent per day is given as follows, and it is updated every day:

$$ROLOL = \frac{24}{L(\Theta_{H,r})} \cdot F_{AA,m}(\Theta_H) \cdot 100\%$$

The mean aging acceleration factor, $F_{AA,m}$, is updated per day, and it is given by:

$$F_{AA,m} = \frac{\sum_{n=1}^{N} F_{AAn} \cdot \Delta t_n}{\sum_{n=1}^{N} \Delta t_n} = \frac{\sum_{n=1}^{N} F_{AAn}}{N}$$

Where:

- F_{AAn} is calculated every cycle
- Δtn = 1cycle
- $F_{AA,\,m}$ states the latest one-day statistics of $F_{AA.}$ When the relay is energized for the first time, $F_{AA,\,m}$ default value is 1.

The residual life in hours at $F_{AA,m}$ is updated per day, and it is given by:

$$L_{res}(F_{AA,m}) = \frac{L_{res}(\Theta_{H,r})}{F_{AA,m}}$$

2.18 Through Fault Monitoring

Through faults are a major cause of transformer damage and failure. Both the insulation and the mechanical effects of fault currents are considered. The through fault current monitoring function in the P64x gives the fault current level, the duration of the faulty condition, the date and time for each through fault. An I^2t calculation based on the recorded time duration and maximum current is performed for each phase. This calculation is only performed when the current is above the **TF I> Trigger** setting and if **Any Differential Start (DDB 1508)** is not asserted. Cumulative stored calculations for each phase are monitored so that the user may schedule the transformer maintenance based on this data. This may also justify possible system enhancement to reduce through fault level.

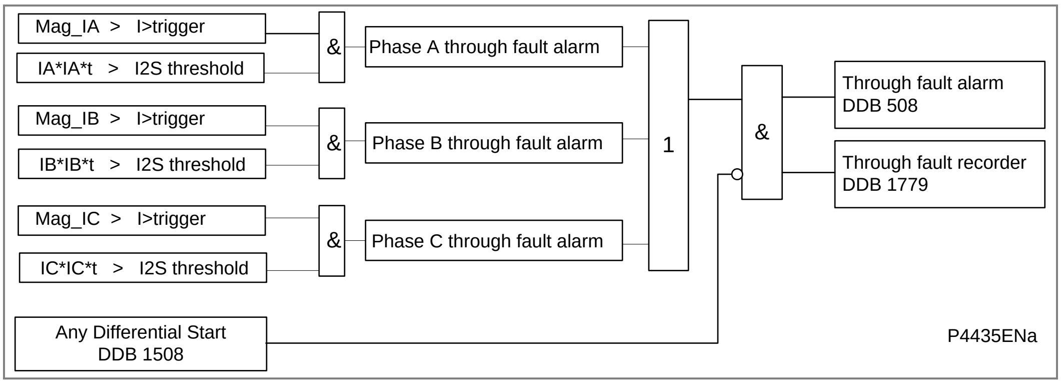
Mag_IA > I>trigger
IA*IA*t > I2S threshold
&
Phase A through fault alarm
Mag_IB > I>trigger
IB*IB*t > I2S threshold
&
Phase B through fault alarm
Mag_IC > I>trigger
IC*IC*t > I2S threshold
&
Phase C through fault alarm
1
&
Through fault alarm DDB 508
Through fault recorder DDB 1779
Any Differential Start DDB 1508
P4435ENa

Figure 45 - Through fault alarm logic

One stage alarm is available for through-fault monitoring. The alarm is issued if the maximum cumulative I^2t in the three phases exceeds the **TF I^2t> Alarm** setting. A through fault event is recorded if any of the phase currents is bigger than the **TF I> Trigger** setting. Set **TF I> Trigger** greater than the overload capability of the transformer. According to IEEE Std. C57.109-1993, values of 3.5 or less times normal base current may result from overloads rather than faults. IEEE Std. C57.91-1995, states that the suggested limit of load for loading above the nameplate of a distribution transformer with 65°C rise is 300% of rated load during short-time loading (0.5 hours or less). On the other hand, the suggested limit of load for loading above the nameplate of a power transformer with 55°C rise is 200% maximum.

To set **TF I^2t> Alarm** consider the recommendations given in IEEE Std. C57.109-1993 for transformers built beginning in the early 1970s. Consult the transformer manufacturer regarding the short circuit withstand capabilities for transformers built prior the early 1970s.

2.18.1 Inputs

Signal name	Description
IA-HV, IB-HV, IC-HV or IA-LV, IB-LV, IC-LV or IA-TV, IB-TV, IC-TV	Phase current levels (Fourier magnitudes) of the selected winding
Any Diff start (DDB1508)	Any 87 or 64 start used by the through fault monitoring logic to avoid: calculating I^2t if either the 87 or 64 element has started. asserting a through fault alarm when either the 87 or 64 element has started.

Table 19 - Inputs

2.18.2 Outputs

Signal name	Description
IA peak, IB peak, IC peak	Peak current in the monitor winding in a per phase basis
I^2t phase A, I^2t phase B, I^2t phase C	I^2t magnitude in the monitor winding in a per phase basis
Through fault alarm (DDB508)	Through fault monitoring alarm
Through fault recorder (DDB1779)	Output signal from the through fault monitoring logic used to trigger the fault recorder

Table 20 - Outputs

IA peak, IB peak, IC peak, I2t phase A, I2t phase B and I2t phase C are given in the VIEW RECORDS menu in the setting file.

2.19 Resistive Temperature Device (RTD) Thermal Protection

To protect against any general or localized overheating, the P64x relay has the ability to accept inputs from up to 10 - 3 wire Type A PT100 Resistive Temperature Sensing Devices (RTD). These are connected as shown in Figure 45.

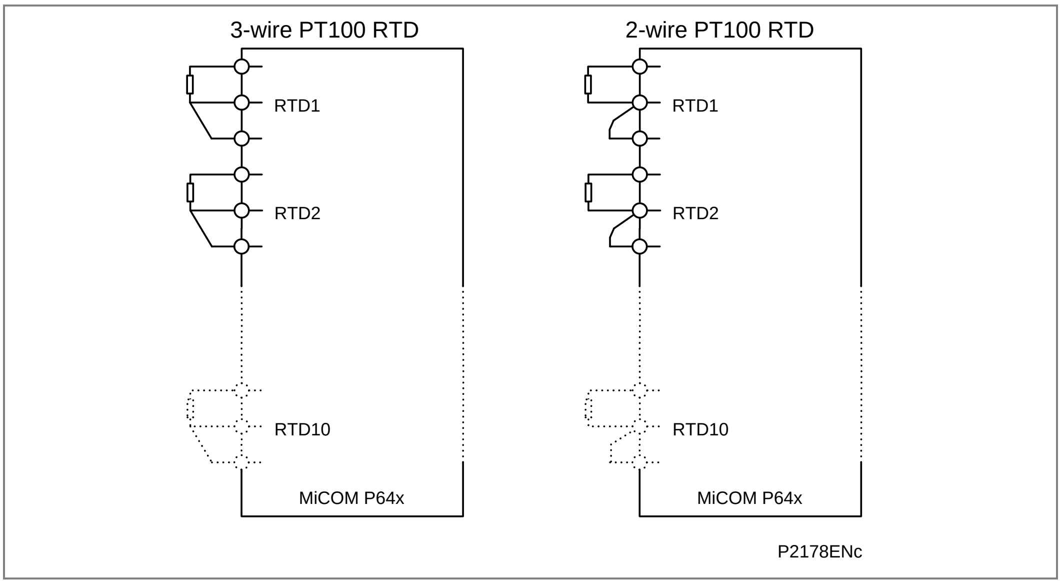

Figure 46 - Connection for RTD thermal probes

Such probes can be strategically placed in areas of the machine that are susceptible to overheating or heat damage.

Note	*Typically a PT100 RTD probe can measure temperature within the range -40° to +300°C. The resistance of these devices changes with temperature, at 0°C they have a resistance of 100Ω.*

If the measured resistance is outside the permitted range, an RTD failure alarm will be raised, indicating an open or short circuit RTD input. These conditions are signaled using DDB signals available in the PSL (DDB 453-456) and are also shown in the **Measurements 3** menu.

DDB signals are also available to indicate the alarm and trip of the each and any RTD, (Alarm: DDB 1728-1737, 452 Trip: DDB 1188-1197, 1198). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

See the *Installation* chapter *P64x/EN IN,* for recommendations on RTD connections and cables.

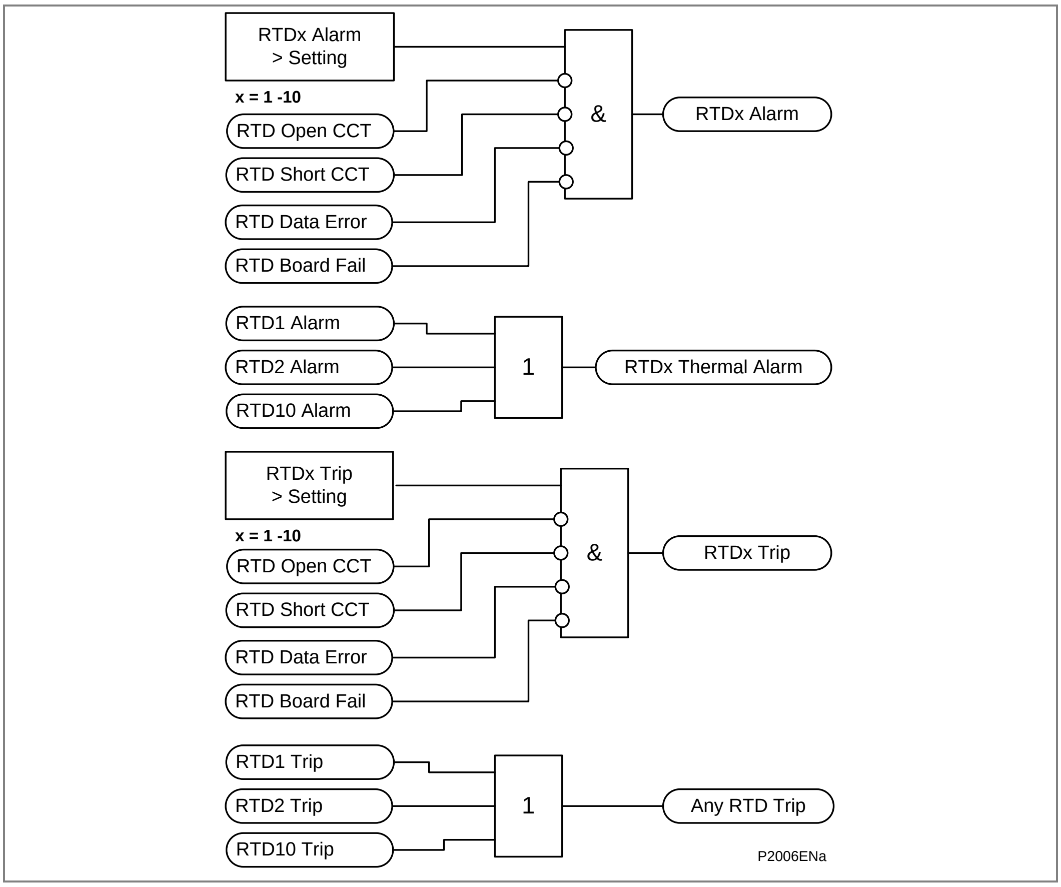
RTDx Alarm > Setting
x = 1 -10
RTD Open CCT
RTD Short CCT
RTD Data Error
RTD Board Fail
&
RTDx Alarm
RTD1 Alarm
RTD2 Alarm
RTD10 Alarm
1
RTDx Thermal Alarm
RTDx Trip > Setting
x = 1 -10
RTD Open CCT
RTD Short CCT
RTD Data Error
RTD Board Fail
&
RTDx Trip
RTD1 Trip
RTD2 Trip
RTD10 Trip
1
Any RTD Trip
P2006ENa

Figure 47 - RTD logic diagram

2.20 Current Loop Inputs and Outputs

2.20.1 Current Loop Inputs

Four analog (or current loop) inputs are provided for transducers with ranges of 0 - 1 mA, 0 - 10 mA, 0 - 20 mA or 4 - 20 mA. The analog inputs can be used for various transducers such as vibration monitors, tachometers and pressure transducers. Associated with each input there are two protection stages, one for alarm and one for trip. Each stage can be individually enabled or disabled and each stage has a definite time delay setting.

The Alarm and Trip stages can be set for operation when the input value falls below the Alarm/Trip threshold **Under** or when the input current is above the input value **Over**. The sample interval is nominally 50 ms per input.

The relationship between the transducer measuring range and the current input range is linear. The maximum and minimum settings correspond to the limits of the current input range. This relationship is shown in Figure 47.

Figure 47 also shows the relationship between the measured current and the analog to digital conversion (ADC) count. The hardware design allows for over-ranging, with the maximum ADC count (4095 for a 12-bit ADC) corresponding to 1.0836 mA for the 0 - 1 mA range, and 22.7556 mA for the 0 - 10 mA, 0 - 20 mA and 4 - 20 mA ranges. The relay will therefore continue to measure and display values beyond the Maximum setting, within its numbering capability (-9999 to 9999).

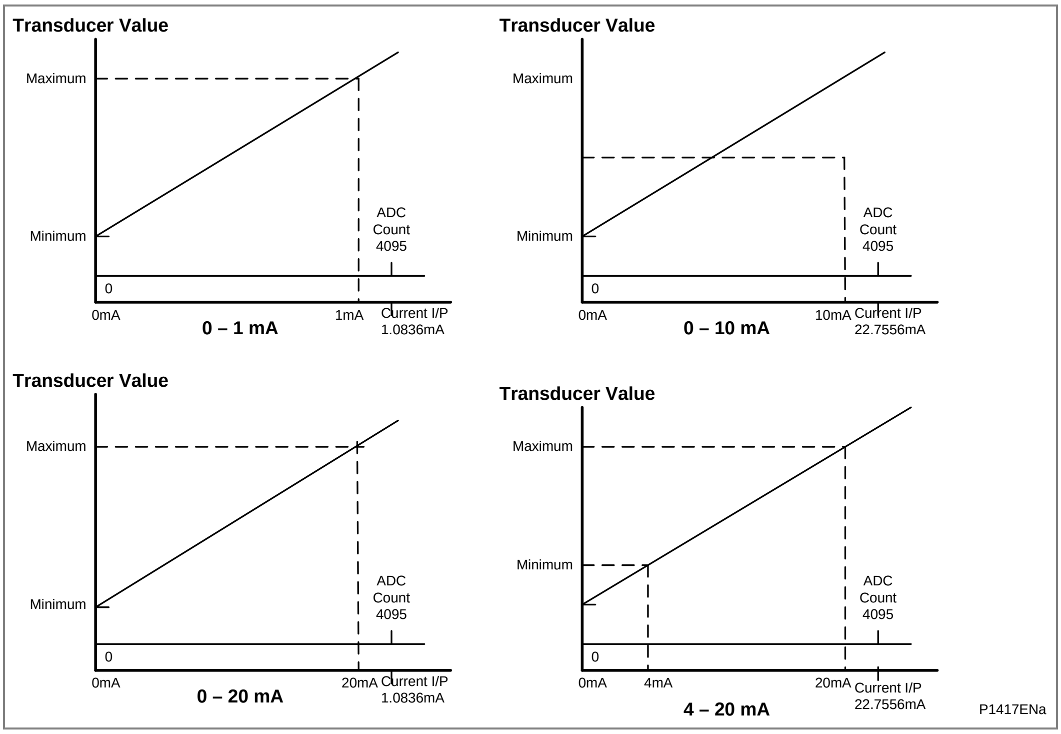

Figure 48 - Relationship between transducer value and current input range

Note	*If the Maximum is set less than the Minimum, the slopes of the graphs will be negative. This is because the mathematical relationship remains the same irrespective of how Maximum and Minimum are set, for example, for 0 - 1 mA range, Maximum always corresponds to 1 mA and Minimum corresponds to 0 mA.*

Power-on diagnostics and continuous self-checking are provided for the hardware associated with the current loop inputs. When a failure is detected, the protection associated with all the current loop inputs is disabled and a single alarm signal (CL Card I/P Fail, DDB 470) is set and an alarm (CL Card I/P Fail) is raised. A maintenance record with an error code is also recorded with additional details about the type of failure.

For the 4 - 20 mA input range, a current level below 4 mA indicates that there is a fault with the transducer or the wiring. An instantaneous under current alarm element is available, with a setting range from 0 to 4 mA. This element controls an output signal (CLI1/2/3/4 I< Fail Alm., DDB 461- 464) which can be mapped to a user defined alarm if required.

Hysteresis is implemented for each protection element. For ‘Over’ protection, the drop-off/pick-up ratio is 95%, for ‘Under’ protection, the ratio is 105%.

A timer block input is available for each current loop input stage which will reset the CLI timers of the relevant stage if energized, (DDB 714-717).If a current loop input is blocked the protection and alarm timer stages and the 4 - 20 mA undercurrent alarm associated with that input are blocked. The blocking signals may be useful for blocking the current loop inputs when the CB is open for example.

DDB signals are available to indicate starting an operation of the alarm and trip stages of the each current loop inputs, (CLI1/2/3/4 Alarm Start: DDB 1614-1617, CLI1/2/3/4 Trip Start: DDB 1618-1621, CL Input 1/2/3/4 Alarm: DDB 457-460, CLI Input1/2/3/4 Trip: DDB 1199-1202). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The current loop input starts are mapped internally to the ANY START DDB signal - DDB 1312.

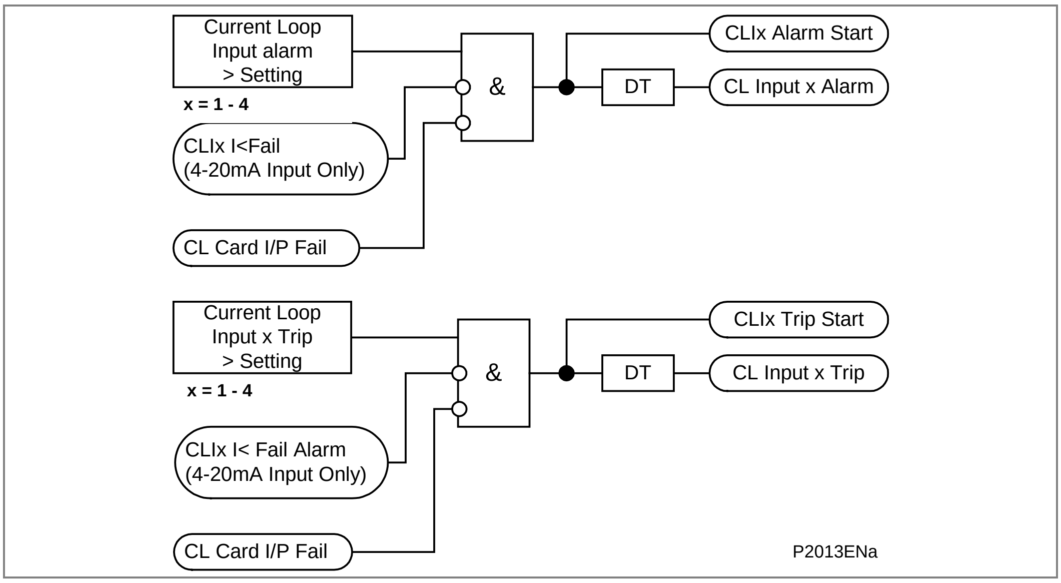
Current Loop Input alarm > Setting
x = 1 - 4
CLIx I<Fail (4-20mA Input Only)
CL Card I/P Fail
&
DT
CLIx Alarm Start
CL Input x Alarm
Current Loop Input x Trip > Setting
x = 1 - 4
CLIx I< Fail Alarm (4-20mA Input Only)
CL Card I/P Fail
&
DT
CLIx Trip Start
CL Input x Trip
P2013ENa

Figure 49 - Current loop input logic diagram

2.20.2 Current Loop Output

Four analog current outputs are provided with ranges of 0 - 1 mA, 0 - 10 mA, 0 - 20 mA or 4 - 20 mA which can alleviate the need for separate transducers. These may be used to feed standard moving coil ammeters for analog indication of certain measured quantities or into a SCADA using an existing analog RTU.

The CLIO output conversion task runs every 50 ms and the refresh interval for the output measurements is nominally 50 ms.

The user can set the measuring range for each analog output. The range limits are defined by the Maximum and Minimum settings.

This allows the user to “zoom in” and monitor a restricted range of the measurements with the desired resolution. Voltage and current quantities can be set in either primary or secondary quantities, depending on the ‘CLO1/2/3/4 Set Values - Primary/Secondary’ setting associated with each current loop output.

The output current of each analog output is linearly scaled to its range limits, as defined by the Maximum and Minimum settings. The relationship is shown in Figure 49.

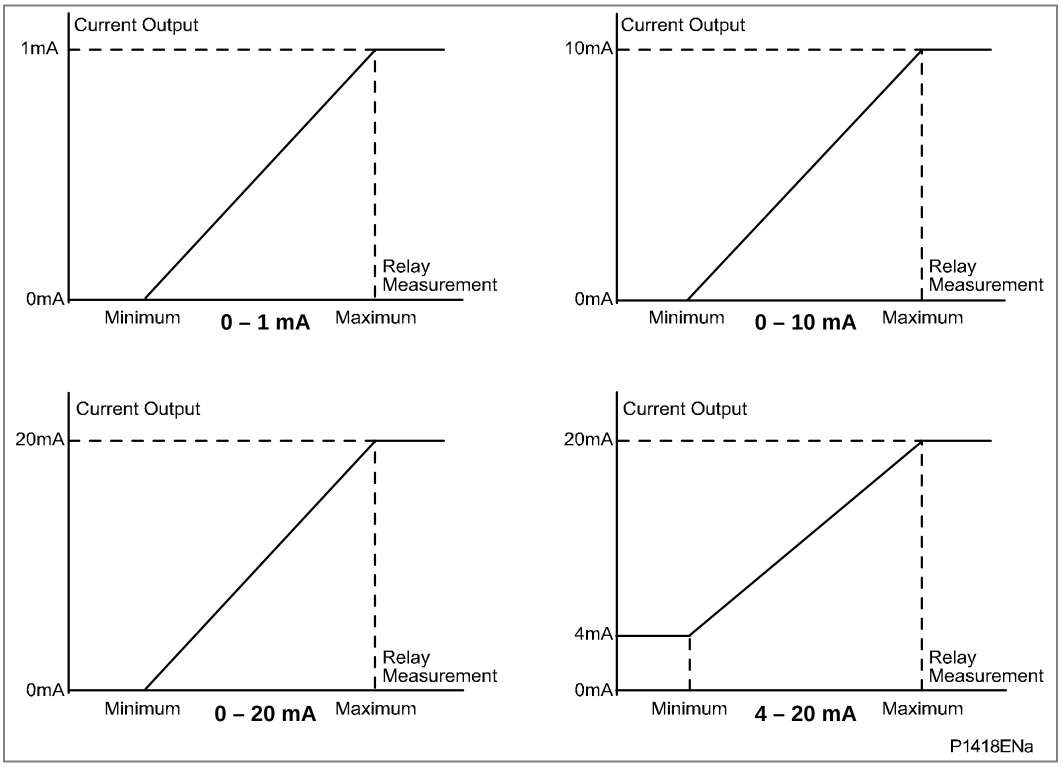

Figure 50 - Relationship between the current output and the relay measurement

Note	*If the Maximum is set less than the Minimum, the slopes of the graphs will be negative. This is because the mathematical relationship remains the same irrespective of how Maximum and Minimum are set, for example, for 0 - 1 mA range, Maximum always corresponds to 1 mA and Minimum corresponds to 0 mA.*

The P64x transducers are of the current output type. This means that the correct value of output will be maintained over the load range specified. The range of load resistance varies a great deal, depending on the design and the value of output current. Transducers with a full scale output of 10 mA will normally feed any load up to a value of 1000 Ω (compliance voltage of 10 V). This equates to a cable length of 15 km (approximately) for lightweight cable (1/0.6 mm cable). A screened cable earthed at one end only is recommended to reduce interference on the output current signal. The table below gives typical cable impedances/km for common cables. The compliance voltage dictates the maximum load that can be fed by a transducer output. Therefore, the 20 mA output will be restricted to a maximum load of 500 Ω approximately.

Cable	1/0.6 mm	1/0.85 mm	1/1.38 mm
CSA (mm^2)	0.28	0.57	1.50
R (Ω/km)	65.52	32.65	12.38

Table 21 - Cable sizes

The receiving equipment, whether it is a simple moving-coil (DC milli-ammeter) instrument or a remote terminal unit forming part of a SCADA system, can be connected at any point in the output loop and additional equipment can be installed at a later date (provided the compliance voltage is not exceeded) without any need for adjustment of the transducer output.

Where the output current range is used for control purposes, it is sometimes worthwhile to fit appropriately rated diodes, or Zener diodes, across the terminals of each of the units in the series loop to guard against the possibility of their internal circuitry becoming open circuit. In this way, a faulty unit in the loop does not cause all the indications to disappear because the constant current nature of the transducer output simply raises the voltage and continues to force the correct output signal round the loop.

Power-on diagnostics and continuous self-checking are provided for the hardware associated with the current loop outputs. When failure is detected, all the current loop output functions are disabled and a single alarm signal (CL Card O/P Fail, DDB 471) is set and an alarm (CL Card O/P Fail) is raised. A maintenance record with an error code is also recorded with additional details about the type of failure.

Current loop output parameters are shown in this table:

Current loop output parameter	Abbreviation	Units	Range	Step	Default min.	Default Max.
Current Magnitude	IA-1 Magnitude IB-1 Magnitude IC-1 Magnitude IA-2 Magnitude IB-2 Magnitude IC-2 Magnitude IA-3 Magnitude IB-3 Magnitude IC-3 Magnitude IA-4 Magnitude IB-4 Magnitude IC-4 Magnitude IA-5 Magnitude IB-5 Magnitude IC-5 Magnitude IA HV Magnitude IB HV Magnitude IC HV Magnitude IA LV Magnitude IB LV Magnitude IC LV Magnitude IA TV Magnitude (P643/P645) IB TV Magnitude (P643/P645) IC TV Magnitude (P643/P645)	A	0 to 16 A	0.01 A	0 A	1.2 A
Current Magnitude	IN HV Measured Mag IN HV Derived Mag IN LV Measured Mag IN LV Derived Mag IN TV Measured Mag (P643/P645) IN TV Derived Mag (P643/P645)	A	0 to 16 A	0.01 A	0 A	1.2 A
Phase Sequence Current Components	I0-1 Magnitude I1-1 Magnitude I2-1 Magnitude I0-2 Magnitude I1-2 Magnitude I2-2 Magnitude I0-3 Magnitude (P643/P645) I1-3 Magnitude (P643/P645) I2-3 Magnitude (P643/P645) I0-4 Magnitude (P645) I1-4 Magnitude (P645) I2-4 Magnitude (P645) I0-5 Magnitude (P645) I1-5 Magnitude (P645) I2-5 Magnitude (P645)	A	0 to 16 A	0.01 A	0 A	1.2 A
P-P Voltage Magnitude	VAB Magnitude VBC Magnitude VCA Magnitude	V	0 to 200 V	0.1 V	0 V	140 V
P-N voltage Magnitude	VAN Magnitude (P643/P645) VBN Magnitude (P643/P645) VCN Magnitude (P643/P645)	V	0 to 200 V	0.1 V	0 V	80 V
Neutral Voltage Magnitude	VN Derived Mag. (P643/645)	V	0 to 200 V	0.1 V	0 V	80 V
P-P Voltage Magnitude	Vx Magnitude	V	0 to 200 V	0.1 V	0 V	80 V
Phase Sequence Voltage Components	V1 Magnitude V2 Magnitude V0 Magnitude	V	0 to 200 V	0.1 V	0 V	80 V
RMS Phase Voltages	VAN RMS (P643/P645) VBN RMS (P643/P645) VCN RMS (P643/P645)	V	0 to 200 V	0.1 V	0 V	80 V

Current loop output parameter	Abbreviation	Units	Range	Step	Default min.	Default Max.
Frequency	Frequency	Hz	0 to 70 Hz	0.01Hz	45 Hz	65 Hz
RTD Temperatures	RTD 1 through to RTD 10	°C	-40°C to 300°C	0.1°C	0°C	200°C
Current Loop Inputs	CL Input 1 through to CL input 4	-	-9999 to 9999	0.1	0	9999
Overflux element W1	Volts/Hz W1 (P643/P645)	V/Hz	0 to 20	0.01	0	4
	V/Hz W1 Thermal (P643/P645)	%	0 to 200	0.01	0	120
Overflux element W2	Volts/Hz W2	V/Hz	0 to 20	0.01	0	4
	V/Hz W2 Thermal	%	0 to 200	0.01	0	120
Hottest spot temperature	Hot Spot T	°C	-40 to 300	0.1	0	200
Top oil temperature	Top Oil T	°C	-40 to 300	0.1	0	200
Ambient temperature	Ambient T	°C	-40 to 300	0.1	0	200
Loss of life status	LOL Status	hr	1 to 300000	1	1	300000
Note 1 The measurements internal refresh rate is 50 ms.						
Note 2 These settings are for nominal 1 A and 100/120 V versions only. For other nominal versions they need to be multiplied accordingly.						

Table 22 - Current loop output parameters

2.21 Overfluxing Protection (V/f)

Magnetic flux in the transformer core is directly proportional to the voltage and inversely proportional to the frequency. The higher the V/f ratio, the greater the magnetizing current that would lead to heating and possible insulation failure. The overfluxing protection function detects an inadmissibly high flux level in the iron core of transformers as caused by a voltage increase or a frequency decrease, or both. The rise in V/f ratio does not require an immediate trip since this condition may be transient, and the normal condition should be restored within 1 to 2 minutes as a maximum.

The P64x relay provides two four stages overfluxing element. The overfluxing element Volts/Hz W1 gets the voltage signal from the three phase VT input. The overfluxing element Volts/Hz W2 acquires the voltage signal from the single phase VT input. The protection measures the ratio of phase to phase voltage, (VAB), to frequency, V/Hz, and will operate when this ratio exceeds the setting. One stage can be set to operate with a definite time or inverse time delay (IDMT), this stage can be used to provide the protection trip output. There are also 3 other definite time stages which can be combined with the inverse time characteristic to create a combined multi-stage V/Hz trip operating characteristic using PSL. A blocking signal is provided for the V/Hz>1 stage 1 only, which has the inverse time characteristic option. The blocking signals are BLK W1 VPERHZ>1 (DDB 712) and BLK W2 VPERHZ>1 (DDB 713). This allows a definite time stage to override a section of the inverse time characteristic if required. The blocking signal has the effect of resetting the timer, the start signal and the trip signal.

There is also one definite time alarm stage that can be used to indicate unhealthy conditions before damage has occurred to the transformer.

The P642 has only one overflux element. On the other hand, the P643/P645 has two separate overflux elements for both HV side and LV side respectively.

Overfluxing is a thermal heating based function, therefore the reset timer starts whenever the flux level drops below pickup. The accumulated heat is linearly decreased from the present value down to zero over the course of the reset time. If after half the reset time, another overfluxing condition appears, the heating will restart from half of the previous accumulated level.

A reset command is provided so that the user can reset the element after injection testing. The reset command will reset all start, trip and alarm DDBs of V/Hz. Measurement related to overflux will also be reset. The overfluxing function can be reset by energizing the relevant DDB signal via the PSL (W1 Rest V/Hz: DDB 889, W2 Rest V/Hz: DDB 890).

The V/Hz>1 stages can be blocked by energizing the relevant DDB signals using the PSL (BLK W1 VPERHZ>1: DDB 712, BLK W2 VPERHZ>1: DDB 713). DDB signals are also available to indicate the start and trip of the protection, (Start: DDB 1599-1602, 1604-1607, Trip: DDB 1240-1247). A further DDB **W1 V/Hz> Alarm Start**, **W2 V/Hz> Alarm Start** signals are generated from the overfluxing alarm stage (DDB 1598, DDB 1603). The state of the DDB signals can be programmed to be viewed in the **Monitor Bit x** cells of the **COMMISSION TESTS** column in the relay.

The overfluxing protection starts are mapped internally to the ANY START DDB signal - DDB 1312.

The first trip stage can be set as an IDMT characteristic given as below:

$$t = \frac{TMS}{(M - 1)^2}$$

Where:

$$M = \frac{V/f}{(\text{ V/f Trip Setting })}$$

V = Measured voltage

f = Measured frequency

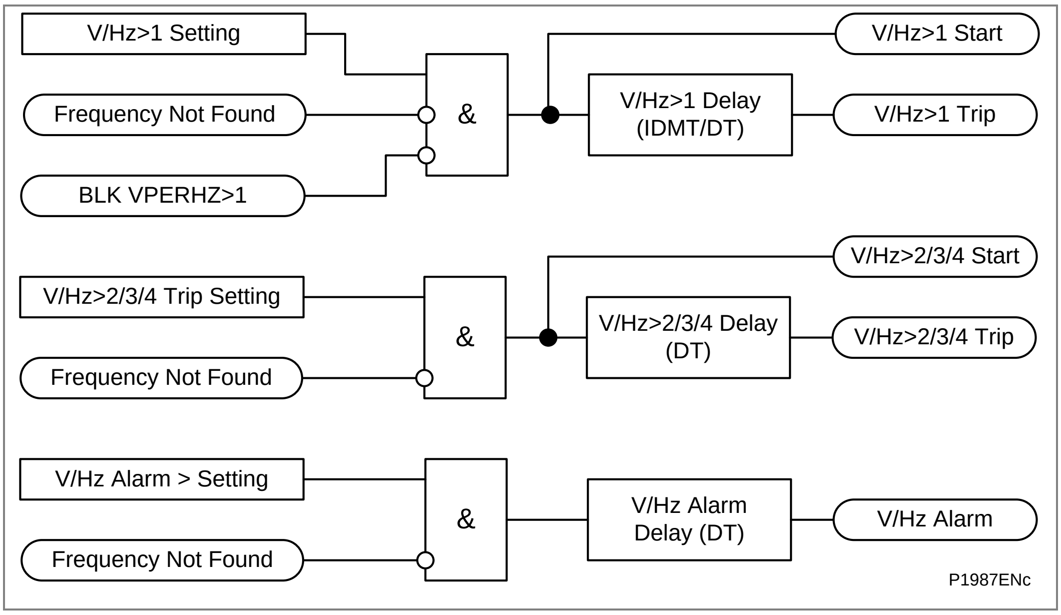
V/Hz>1 Setting
Frequency Not Found
BLK VPERHZ>1
&
V/Hz>1 Delay (IDMT/DT)
V/Hz>1 Start
V/Hz>1 Trip
V/Hz>2/3/4 Trip Setting
Frequency Not Found
&
V/Hz>2/3/4 Delay (DT)
V/Hz>2/3/4 Start
V/Hz>2/3/4 Trip
V/Hz Alarm > Setting
Frequency Not Found
&
V/Hz Alarm Delay (DT)
V/Hz Alarm
P1987ENc

Figure 51 - Overfluxing logic diagram

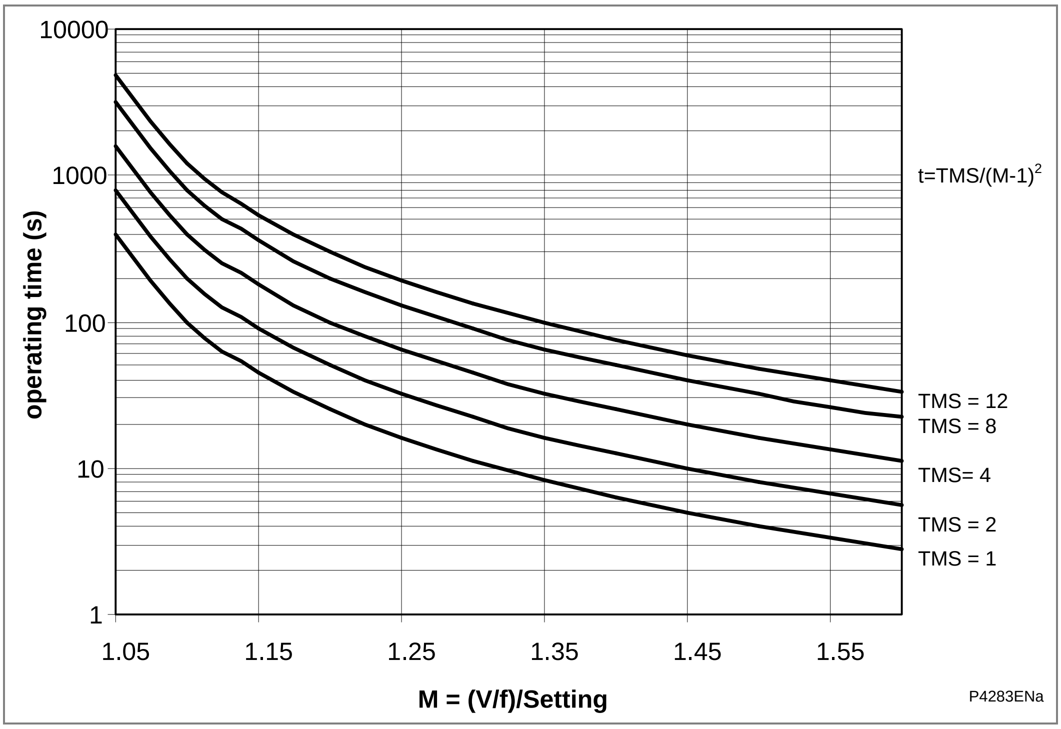

Figure 52 - IDMT overfluxing protection characteristic

The IDMT characteristic is implemented as a thermal function. The internal IDMT timer is treated as a thermal replica with a cooling characteristic. After a V/Hz excursion, the timer should reset according to the reset cooling characteristic. Otherwise, if the unit is subjected to another V/Hz excursion before it has cooled to normal condition, damage could occur before the V/Hz trip point is reached.

A linear reset curve with a Reset Time (V/Hz>x tReset) setting is used for this purpose. The actual reset time left is:

Reset time = tReset * IDMTtimer/tTarget

Where tTarget = TMS/(M-1)^2.

The actual trip time delay is:

Trip delay = tTarget * (1-RESETtimer/tReset)

The following example explains the reset characteristic. It will take tReset time for the thermal replica to reset completely to zero after the thermal replica reaches 100% of V/f>1 Trip at stage 1. If the thermal replica has not reached 100% of V/f>1 Trip, the reset time will be reduced proportionally. For example, if the Reset Time setting is set to 100 s, and the thermal replica has only reached 50% of V/f>1 Trip when V/Hz resets, the reset time will be 50 s, as shown in Stage 2. If another V/Hz excursion appears before the first reset reaches V/f>1 Reset, the V/Hz time delay takes the reset time left into consideration, as shown in Stage 3.

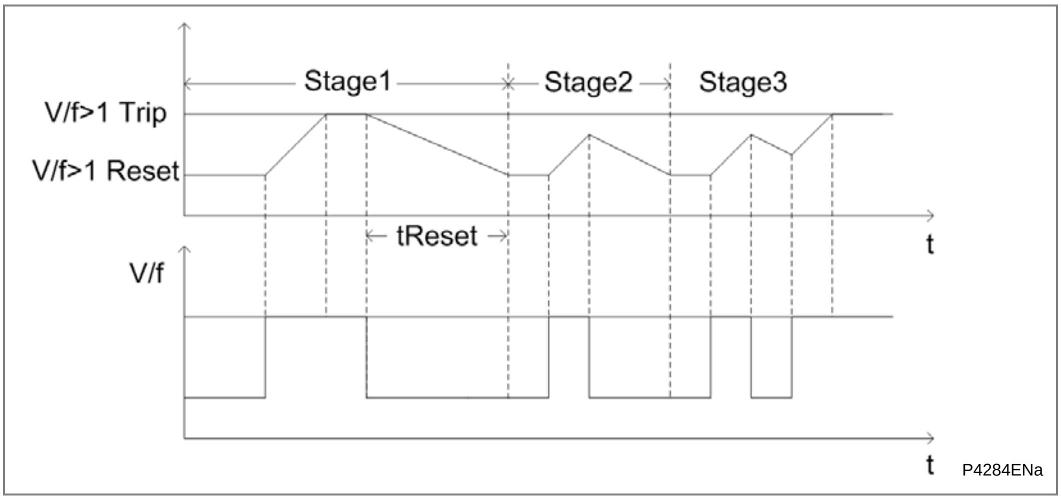
Stage1
Stage2
Stage3
V/f>1 Trip
V/f>1 Reset
tReset
t
V/f
t
P4284ENa

Figure 53 - Reset characteristic

3 OPERATION OF NON-PROTECTION FUNCTIONS

3.1 Current Transformer Supervision (CTS)

Current Transformer Supervision (CTS) is based on the measurement of the ratio of I2/I1 at all ends. When this ratio is not zero, one of the following two conditions may be present:

- An unbalanced fault is present on the system - both I2 and I1 are non-zero
- There is a 1 or 2 phase CT problem - both I2 and I1 are non-zero

If the I2/I1 ratio is greater than the set value, CTS I2/I1>2, at all ends, it is almost certainly a genuine fault condition (CTS I2/I1>2 set above maximum unbalanced load and below the minimum unbalanced fault current). Therefore CTS will not operate. If this ratio is detected at one end only, one of the following conditions may be present:

- A CT problem
- A single end fed fault condition

I1 is used to confirm whether it is a CT problem or not. If I1 > CTS I1 is detected at all ends, it must be a CT problem and CTS is allowed to operate. If this condition (I1 > CTS I1) is detected at only one end, it is assumed that either an inrush condition or a single end fed internal fault is present. Therefore, the CTS operation is blocked.

The CTS status under the **CT SUPERVISION** sub-heading can be set either as indication or restraint. In indication mode, the CTS alarm time delay is automatically set to zero. If a CT failure is present, an alarm would be issued without delay, but the differential protection would remain unrestricted. Therefore, the risk of unwanted tripping under load current is present. In restraint mode, the differential protection is blocked for 20 ms after CT failure has been detected. Then the new setting Is-CTS is applied to the differential protection, as shown in Figure 53, the restraint region of the bias characteristic increases. The low impedance REF, earth fault and NPS overcurrent protections are internally blocked by CTS when a CT failure is detected in the CT used by each protection function. Earth fault protection is immune to CTS blocking if **IN> input** is set to **measured**.

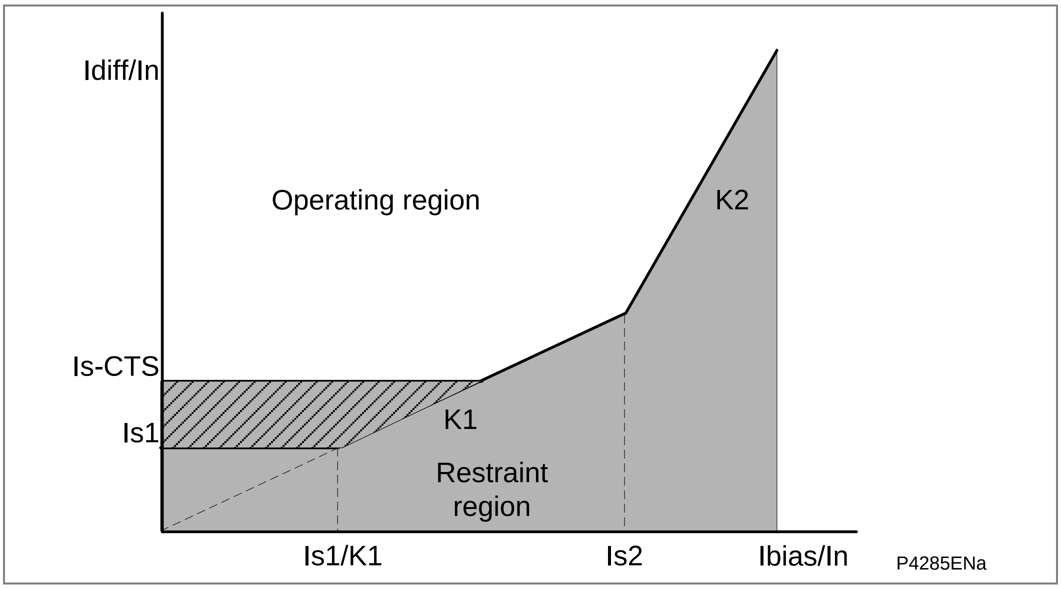

Figure 54 - CTS I1 setting applied to the differential protection

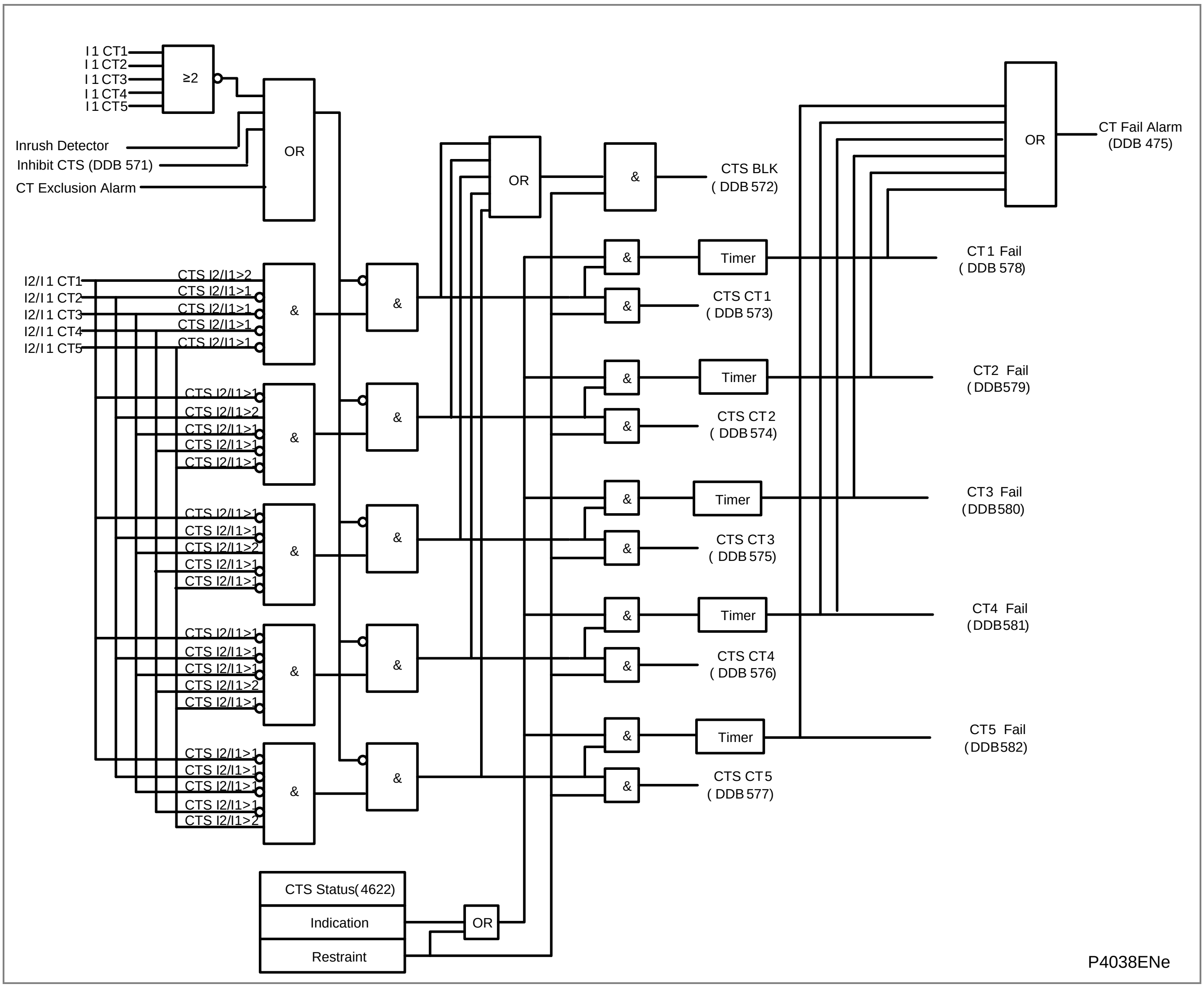
I 1 CT1
I 1 CT2
I 1 CT3
I 1 CT4
I 1 CT5
≥2
Inrush Detector
Inhibit CTS (DDB 571)
CT Exclusion Alarm
OR
I2/I 1 CT1
I2/I 1 CT2
I2/I 1 CT3
I2/I 1 CT4
I2/I 1 CT5
CTS I2/I1>2
CTS I2/I1>1
&
OR
&
CTS BLK
(DDB 572)
Timer
CT1 Fail
(DDB 578)
CTS CT1
(DDB 573)
CT2 Fail
(DDB579)
CTS CT2
(DDB 574)
CT3 Fail
(DDB580)
CTS CT3
(DDB 575)
CT4 Fail
(DDB581)
CTS CT4
(DDB 576)
CT5 Fail
(DDB582)
CTS CT5
(DDB 577)
CT Fail Alarm
(DDB 475)
CTS Status(4622)
Indication
Restraint
P4038ENe

Figure 55 - Differential CTS logic diagram

Figure 54 shows that CTS monitors the positive and negative sequence currents of all ends (2 to 5, depending on the relay model). A faulty CT is determined if the following conditions are present at the same time:

- The positive sequence current in at least two current inputs exceeds the set release threshold I1 (**CTS I1** setting under the **SUPERVISION** menu). This also means that CTS can only operate if minimum load current of the protected object is present.
- On exactly one end a high set ratio of negative to positive sequence current, CTS I2/I1>2, is exceeded.
- On all other ends the ratio of negative to positive sequence current is less than a low set value, CTS I2/I1> 1, or no significant current is present (positive sequence current is below the release threshold I1)

Only a single or double phase CT failure can be detected by this logic. The probability of symmetrical three-phase CT failures is very low, therefore in practice this is not a significant problem.

3.2 Current Input Exclusion

It is possible to exclude current inputs from the protection functions in the P643 and P645. Any current input can be excluded as follows:

The appropriate DDB (DDB 737, 738, 739, 740 or 741) is asserted and the undercurrent condition is satisfied.

The DDB 736 is asserted and DDB 737, 738, 739, 740 or 741 is asserted.

When a current input is excluded, the relay sets to zero the current from that input, so that the protection functions considering the excluded current input detect zero current. On the other hand, the relay still measures the current that might be flowing through the excluded current input and compares it against the under current element threshold. The under current threshold is fixed to 0.05 In. The inputs required are as follows:

Signal name	This signal should be asserted:
CT Exclusion enabled (DDB 736)	to exclude any of the CT inputs without considering the undercurrent elements.
T1 CT Exclusion enabled (DDB 737)	so that T1 CT may be excluded.
T2 CT Exclusion enabled (DDB 738)	so that T2 CT may be excluded.
T3 CT Exclusion enabled (DDB 739)	so that T3 CT may be excluded.
T4 CT Exclusion enabled (DDB 740)	so that T4 CT may be excluded.
T5 CT Exclusion enabled (DDB 741)	so that T5 CT may be excluded.

Table 23 - Inputs

The outputs are as follows:

Signal name	Description
T1 CT Excluded (DDB 704)	When this signal is asserted, T1 CT is excluded from every protection function.
T2 CT Excluded (DDB 705)	When this signal is asserted, T2 CT is excluded from every protection function.
T3 CT Excluded (DDB 706)	When this signal is asserted, T3 CT is excluded from every protection function.
T4 CT Excluded (DDB 707)	When this signal is asserted, T4 CT is excluded from every protection function.
T5 CT Excluded (DDB 708)	When this signal is asserted, T5 CT is excluded from every protection function.
CT exclusion-protection disabled (DDB 1723)	The status of the Tx CT excluded is stored in NVRAM. During the relay initialization after an auxiliary power supply failure, the stored state is compared with the present state. If there is a discrepancy, then this signal is asserted. When this DDB is asserted, all the protection functions using current signals are blocked.
Insufficient number of CTs (DDB 485)	This alarm is asserted when more than one current input is excluded from the P643 or when more than three current inputs are excluded from the P645.

Table 24 - Outputs

Only one current input can be excluded from the P643 and a maximum of three current inputs can be excluded from the P645. An alarm (DDB 485) is issued when more than the maximum number of current inputs is excluded. The status of DDBs 704, 705, 706, 707, and 708 is stored in NVRAM. An alarm (DDB 1723) is raised if the stored statuses do not match the statuses after the power supply is re-established. When DDB 1723 is asserted, the following functions are blocked: differential, REF, Overcurrent, negative phase sequence overcurrent, earth fault, thermal overload, through fault, circuit breaker failure, CT supervision and VT Supervision.

Figure 55 shows the current input exclusion logic.

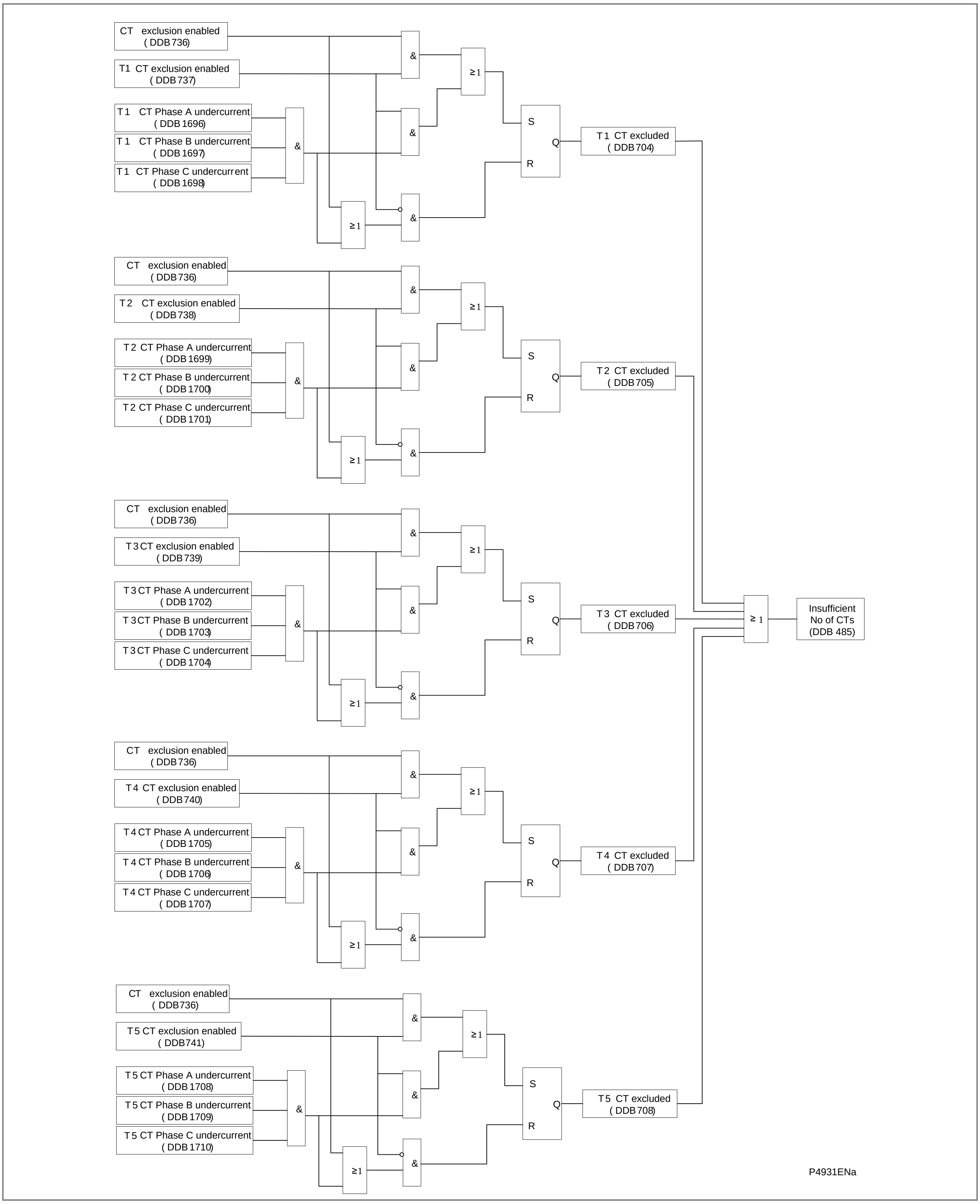
CT exclusion enabled (DDB 736)
T1 CT exclusion enabled (DDB 737)
T1 CT Phase A undercurrent (DDB 1696)
T1 CT Phase B undercurrent (DDB 1697)
T1 CT Phase C undercurrent (DDB 1698)
T1 CT excluded (DDB 704)
T2 CT exclusion enabled (DDB 738)
T2 CT Phase A undercurrent (DDB 1699)
T2 CT Phase B undercurrent (DDB 1700)
T2 CT Phase C undercurrent (DDB 1701)
T2 CT excluded (DDB 705)
T3 CT exclusion enabled (DDB 739)
T3 CT Phase A undercurrent (DDB 1702)
T3 CT Phase B undercurrent (DDB 1703)
T3 CT Phase C undercurrent (DDB 1704)
T3 CT excluded (DDB 706)
T4 CT exclusion enabled (DDB 740)
T4 CT Phase A undercurrent (DDB 1705)
T4 CT Phase B undercurrent (DDB 1706)
T4 CT Phase C undercurrent (DDB 1707)
T4 CT excluded (DDB 707)
T5 CT exclusion enabled (DDB 741)
T5 CT Phase A undercurrent (DDB 1708)
T5 CT Phase B undercurrent (DDB 1709)
T5 CT Phase C undercurrent (DDB 1710)
T5 CT excluded (DDB 708)
Insufficient No of CTs (DDB 485)
&
≥1
S
R
Q
P4931ENa

Figure 56 - Current input exclusion logic

3.3 Circuitry Fail Alarm

The circuitry fail alarm logic requires the following settings: Is-cctfail>, K-cctfail and tls-cctfail>. If the differential current is bigger than Is-cctfail> setting and not trip is issued after the tls-cctfail> time delay has elapsed, an alarm would be issued indicating a CT problem.

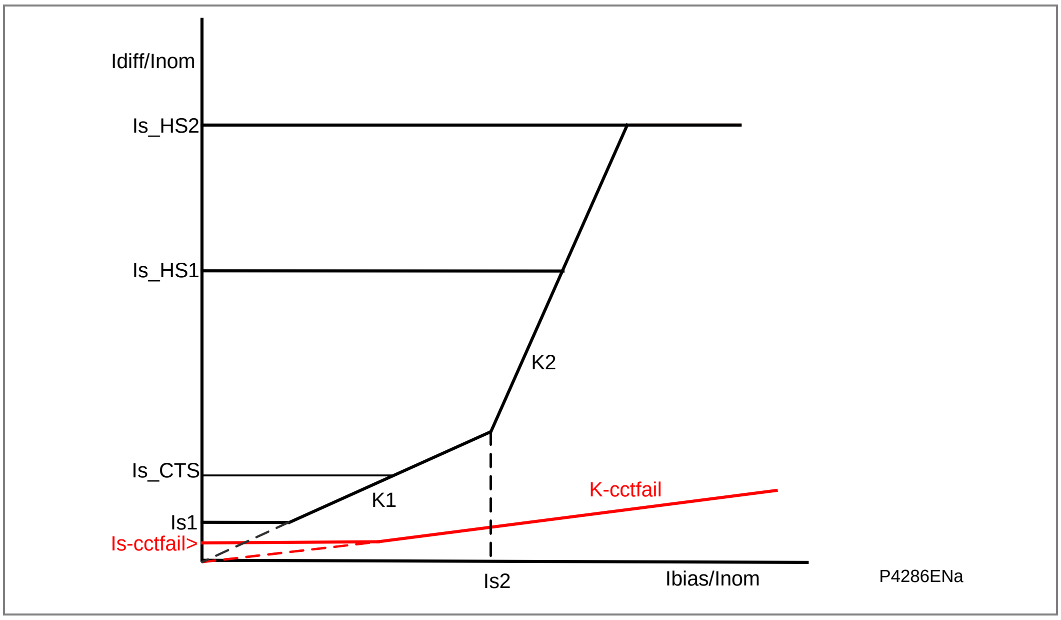

Figure 57 - Circuitry fail alarm fault characteristic

3.4 Voltage Transformer Supervision (VTS)

The Voltage Transformer Supervision (VTS) feature is used to detect failure of the ac voltage inputs to the relay. This may be caused by internal voltage transformer faults, overloading, or faults on the interconnecting wiring to relays. This usually results in one or more VT fuses blowing. Following a failure of the ac voltage input there would be a misrepresentation of the phase voltages on the power system, as measured by the relay, which may result in maloperation.

The VTS status may be set to disabled, blocking or indication. The VTS logic in the relay is designed to detect the voltage failure, and automatically adjust the configuration of protection elements whose stability would otherwise be compromised. A time-delayed alarm output is also available.

VTS can be declared by a Miniature Circuit Breaker (MCB) status input, or by an internal logic using relay measurement. For the measured method, there are three main aspects to consider regarding the failure of the VT supply. These are defined below:

- Loss of one or two phase voltages
- Loss of all three phase voltages under load conditions
- Absence of three phase voltages upon line energization

The settings **VTS I>Inhibit** and **VTS I2>Inhibi**t are in pu values. The VTS logic considers the current associated to the winding where the VT is located.

In a P642, the **VTS I>Inhibit** and **VTS I2>Inhibit** settings are always referred to CT1 or CT2 if the VT is located in the HV or LV windings respectively.

In a P643, the **VTS I>Inhibit** and **VTS I2>Inhibit** settings are always referred to CT1, CT2 or CT3 if the VT is located in the HV, TV or LV windings respectively.

In a P645, the **VTS I>Inhibit** and **VTS I2>Inhibit** settings are always referred to CT1, CT3 or CT5 if the VT is located in the HV, TV or LV windings respectively. In a P645, if the VT is in the HV winding, and the HV CT Terminals setting is 00011, then T1 CT and T2 CT are associated to the HV winding. The relay compares the HV current on a per-phase basis to the **VTS I>Inhibit** setting, and the HV negative sequence current to the **VTS I2>Inhibit** setting. In this case, the settings are always relative to T1 CT.

3.4.1 Loss of One or Two Phase Voltages

The VTS feature within the relay operates on detection of negative phase sequence (NPS) voltage without the presence of negative phase sequence current. This gives operation for the loss of one or two phase voltages. Stability of the VTS function is assured during system fault conditions, by the presence of NPS current. The use of negative sequence quantities ensures correct operation even where three-limb or ‘V’ connected VTs are used.

Negative Sequence VTS Element:

> The negative sequence thresholds used by the element are V2 = 10 V (V2 drop off is 9.5 V) and I2 = 0.05 to 0.5In settable (defaulted to 0.05 In).

3.4.2 Loss of all Three Phase Voltages Under Load Conditions

Under the loss of all three phase voltages to the relay, there will be no negative phase sequence quantities present to operate the VTS function. However, under such circumstances, a collapse of the three phase voltages will occur. If this is detected without a corresponding change in any of the phase current signals (which would be indicative of a fault), then a VTS condition will be raised. In practice, the relay detects the presence of superimposed current signals, which are changes in the current applied to the relay. These signals are generated by comparison of the present value of the current with that exactly one cycle previously. Under normal load conditions, the value of superimposed current should therefore be zero. Under a fault condition a superimposed current signal will be generated which will prevent operation of the VTS.

The phase voltage level detectors are fixed and will drop off at 10 V and pickup at 30 V.

The sensitivity of the superimposed current elements is fixed at 0.1 In.

3.4.3 Absence of Three Phase Voltages Upon Line Energization

If a VT were inadvertently left isolated prior to line energization, incorrect operation of voltage dependent elements could result. The previous VTS element detected three phase VT failure by absence of all 3 phase voltages with no corresponding change in current. On line energization there will, however, be a change in current (as a result of load or line charging current for example). An alternative method of detecting 3 phase VT failure is therefore required on line energization.

The absence of measured voltage on all 3 phases on line energization can be as a result of 2 conditions. The first is a 3 phase VT failure and the second is a close up three phase fault. The first condition would require blocking of the voltage dependent function and the second would require tripping. To differentiate between these 2 conditions an overcurrent level detector (VTS I> Inhibit) is used which will prevent a VTS block from being issued if it operates. This element should be set in excess of any non-fault based currents on line energization (load, line charging current, transformer inrush current if applicable) but below the level of current produced by a close up 3 phase fault. If the line is now closed where a 3 phase VT failure is present the overcurrent detector will not operate and a VTS block will be applied. Closing onto a three phase fault will result in operation of the overcurrent detector and prevent a VTS block being applied.

This logic will only be enabled during a live line condition (as indicated by the relays pole dead logic) to prevent operation under dead system conditions, such as where no voltage will be present and the VTS I> Inhibit overcurrent element will not be picked up.

Required to drive the VTS logic are a number of dedicated level detectors as follows:

- IA>, IB>, IC>, these level detectors operate in less than 20 ms and their settings should be greater than load current. This setting is specified as the VTS current threshold. These level detectors pick-up at 100% of setting and drop-off at 95% of setting.
- I2>, this level detector operates on negative sequence current and has a user setting. This level detector picks-up at 100% of setting and drops-off at 95% of setting.
- ∆IIA>, ∆IB>, ∆IC>, these level detectors operate on superimposed phase currents and have a fixed setting of 10% of nominal. These level detectors are subject to a count strategy such that 0.5 cycle of operate decisions must have occurred before operation.
- VA>, VB>, VC>, these level detectors operate on phase voltages and have a fixed setting, Pick-up level = 30 V (Vn = 100/120 V), 120V (Vn = 380/480 V), Drop Off level = 10V (Vn = 100/120 V), 40V (Vn = 380/480 V).
- VAB>, VBC>, these level detectors operate on phase-phase voltages and have a fixed setting, Pick-up level = 95 V (Vn = 100/120 V), Drop Off level = 70V (Vn = 100/120 V).
- V2>, this level detector operates on negative sequence voltage, it has a fixed setting of 10V/40 V depending on VT rating (100/120 or 380/480) with pick-up at 100% of setting and drop-off at 95% of setting.

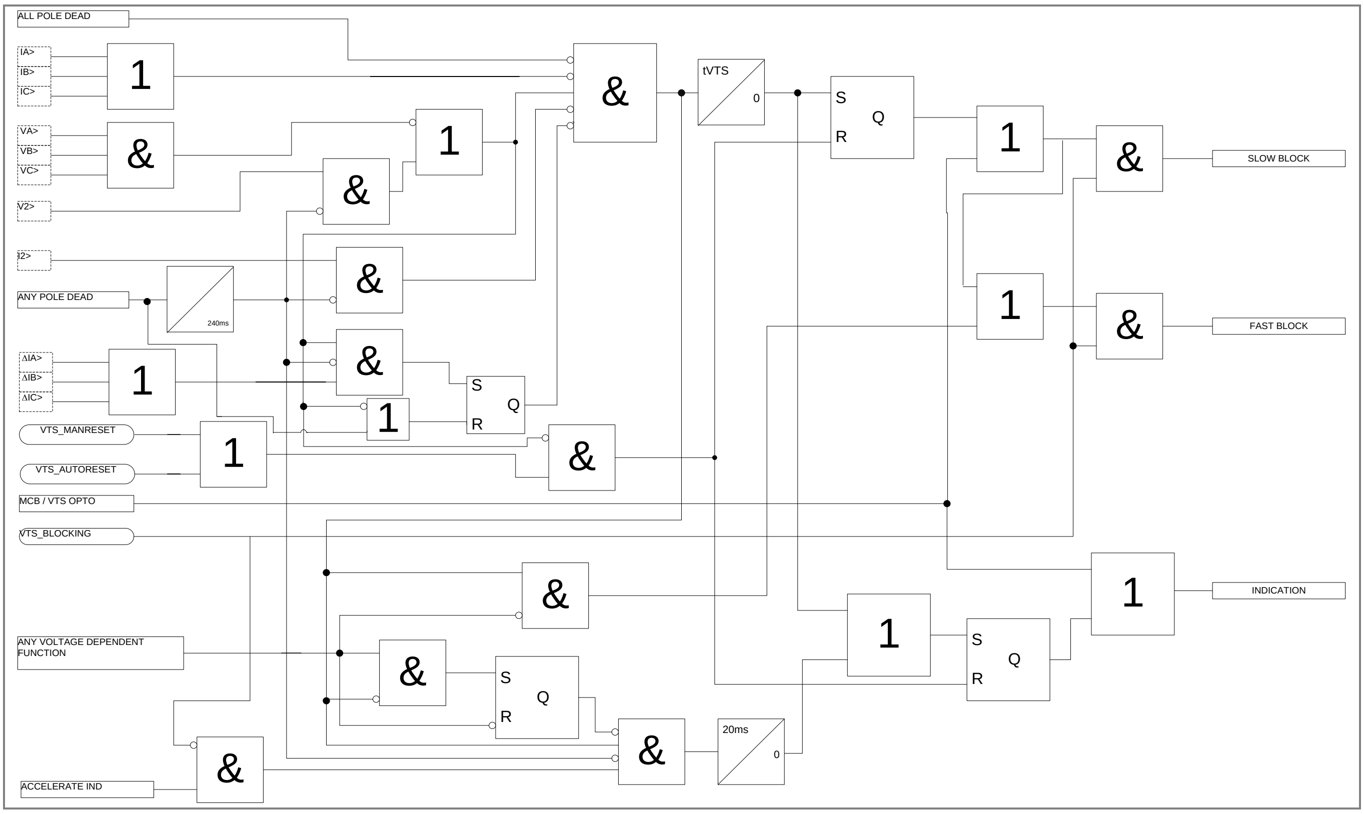
ALL POLE DEAD
IA>
IB>
IC>
VA>
VB>
VC>
V2>
I2>
ANY POLE DEAD
240ms
ΔIA>
ΔIB>
ΔIC>
VTS_MANRESET
VTS_AUTORESET
MCB / VTS OPTO
VTS_BLOCKING
ANY VOLTAGE DEPENDENT FUNCTION
ACCELERATE IND
tVTS
0
S
Q
R
20ms
SLOW BLOCK
FAST BLOCK
INDICATION

Figure 58 - VTS logic - P645 and P643

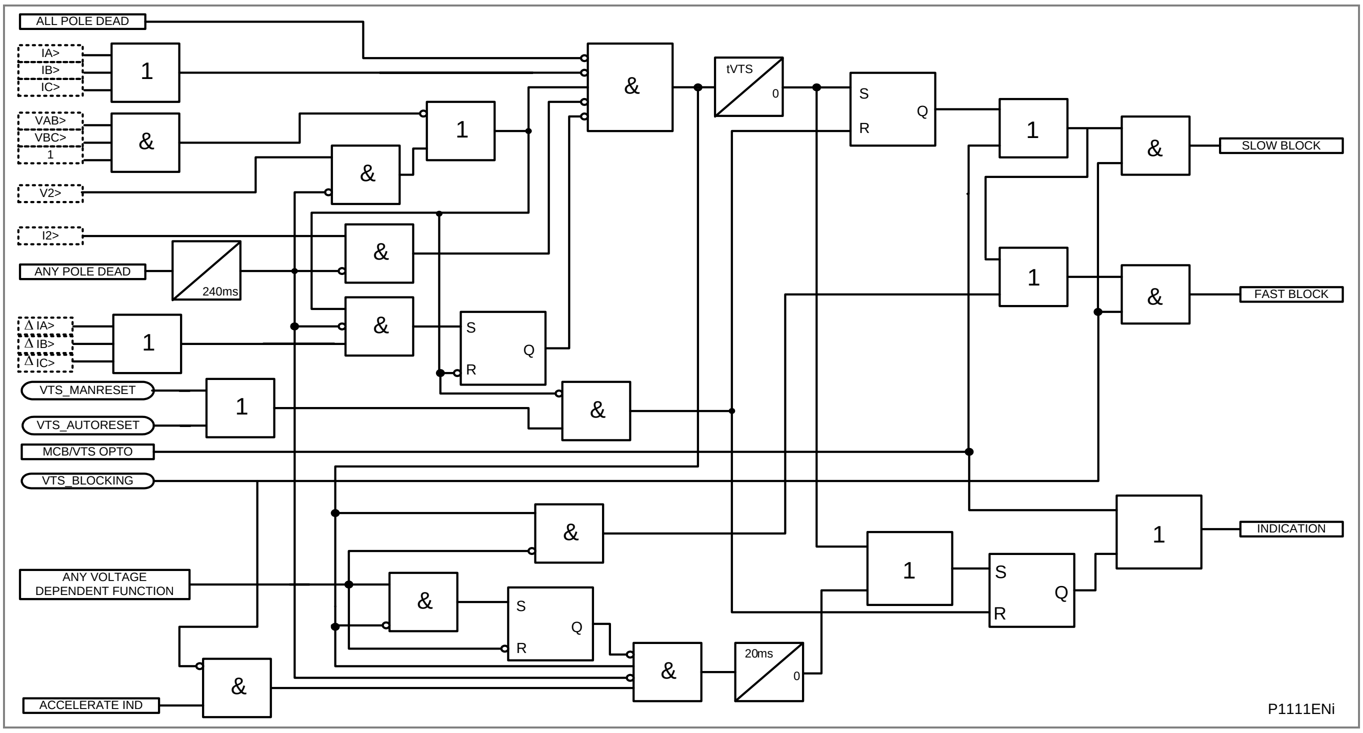
ALL POLE DEAD
IA>
IB>
IC>
VAB>
VBC>
1
V2>
I2>
ANY POLE DEAD
240ms
Δ IA>
Δ IB>
Δ IC>
VTS_MANRESET
VTS_AUTORESET
MCB/VTS OPTO
VTS_BLOCKING
ANY VOLTAGE DEPENDENT FUNCTION
ACCELERATE IND
tVTS
0
S
Q
R
20ms
SLOW BLOCK
FAST BLOCK
INDICATION
P1111ENi

Figure 59 - VTS logic - P642

3.4.3.1 Inputs

Signal name	Description
IA>, IB>, IC>	Phase current levels (Fourier magnitudes)
I2>	I2 level (Fourier magnitude).
ΔIA, ΔIB, ΔIC	Phase current samples (current and one cycle previous)
VA>, VB>, VC>	Phase voltage signals (Fourier magnitudes)
V2>	Negative sequence voltage (Fourier magnitude)
ALL POLE DEAD (DDB 1772)	Breaker is open for all phases (driven from auxiliary contact or pole dead logic).
VTS_MANRESET	A VTS reset performed via front panel or remotely.
VTS_AUTORESET	A setting to allow the VTS to automatically reset after this delay.
MCB/VTS OPTO (DDB 874)	To remotely initiate the VTS blocking using an opto
Any Voltage Dependent Function (DDB 1739)	Output from any function that uses the system voltage, if any of these functions operate before a VTS is detected; the VTS is blocked from operation. The outputs include starts and trips. It is a hidden DDB not available for customer use.
Accelerate Ind (DDB 1738)	Signal from a fast tripping voltage dependent function used to accelerate indications when the indicate only option is selected. It is a hidden DDB not available for customer use.
Any Pole Dead (DDB 1773)	Breaker is open on one or more than one phases (driven from auxiliary contact or pole dead logic)
tVTS	The VTS timer setting for latched operation

Table 25 - Inputs

3.4.3.2 Outputs

Signal name	Description
VTS Fast Block (DDB1 800)	Used to block voltage dependent functions
VTS Slow Block (DDB 1801)	Used to block the Any Pole dead signal
VTS Indication (DDB 477)	Signal used to indicate a VTS operation

Table 26 - Outputs

3.4.4 Operation

The relay may respond as follows to an operation of any VTS element:

- VTS set to provide alarm indication only (DDB 477 VT Fail Alarm);
- Optional blocking of voltage dependent protection elements (DDB 1800 VTS Fast Block, DDB 1801 VTS Slow Block);
- Optional conversion of directional overcurrent directional earth fault and directional NPS overcurrent elements to non-directional protection (available when set to blocking mode only). These settings are found in the function links cell of the relevant protection element columns in the menu.

Time delayed protection elements (Directional NPS Overcurrent) are blocked after the VTS Time Delay on operation of the VTS Slow Block. Fast operating protection elements (Directional overcurrent, Neutral Voltage Displacement, Undervoltage) are blocked on operation of the VTS Fast Block.

Note *The neutral voltage displacement protection is only blocked by VTS if the neutral voltage input is set to Derived and not Measured.*

Other protections can be selectively blocked by customizing the PSL, integrating DDB 1800 VTS Fast Block and DDB 1801 VTS Slow Block with the protection function logic.

The VTS I> Inhibit or VTS I2> Inhibit elements are used to override a VTS block in event of a fault occurring on the system which could trigger the VTS logic. Once the VTS block has been established, however, then it would be undesirable for subsequent system faults to override the block. The VTS block will therefore be latched after a user settable time delay **VTS Time Delay**. Once the signal has latched then two methods of resetting are available. The first is manually using the front panel interface (or remote communications) provided the VTS condition has been removed and secondly, when in ‘Auto’ mode, by the restoration of the three-phase voltages above the phase level detector settings mentioned previously.

A VTS indication will be given after the VTS Time Delay has expired. In the case where the VTS is set to indicate only the relay may potentially mal-operate, depending on which protection elements are enabled. In this case the VTS indication will be given before the VTS time delay expires if a trip signal is given.

Where a Miniature Circuit Breaker (MCB) is used to protect the voltage transformer ac output circuits, it is common to use MCB auxiliary contacts to indicate a three-phase output disconnection. As previously described, it is possible for the VTS logic to operate correctly without this input. However, this facility has been provided for compatibility with various utilities current practices. Energizing an opto-isolated input assigned to **MCB Open** on the relay will therefore provide the necessary block.

Where directional overcurrent elements are converted to non-directional protection on VTS operation, it must be ensured that the current pick-up setting of these elements is higher than full load current.

3.4.5 Pole Dead Logic

The pole dead logic in the P642 requires two single-phase VT inputs. It requires the three phase VT input in the P643 and P645. VAB and VBC are considered in P642 and in P643/P645 VAN, VBN and VCN are considered. The pole dead logic is only available for the winding where the three-phase VT or two single phase VTs are located. This logic is used by the relay to determine when the circuit breaker poles are open ("pole dead"). This indication may be forced, using status indication from CB auxiliary contacts (52a or 52b), or internally determined by the relay. 52b contacts need to be inverted in the PSL because only the CB closed DDB signal is available for each breaker. The relay will also initiate a pole dead condition if the following conditions are asserted:

- 3PH_CB_OPEN signal low
- Slow Block VTS signal low
- The line current and voltage fall below a preset threshold.

This is necessary so that a pole dead indication is still given even when an upstream breaker is opened. The undervoltage (V<) and undercurrent (I<) thresholds have the following, fixed, pick-up and drop-off levels:

- VA<, VB<, VC<, these level detectors operate on phase voltages and have a fixed setting, Pick-up level = 10 V (Vn = 100/120 V), 40V (Vn = 380/480 V), Drop Off level = 30V (Vn = 100/120 V), 120V (Vn = 380/480 V).
- VAB<, VBC<, these level detectors operate on phase-phase voltages and have a fixed setting, Pick-up level = 70 V (Vn = 100/120 V), Drop Off level = 95V (Vn = 100/120 V).
- IA<, IB<, IC<, these level operate on phase currents and have a fixed setting, Pick-up level = 0.05 In, Drop Off level = 0.055 In.

Note	*If the VT is connected at the busbar side, auxiliary contacts (52a or 52b) must be connected to the relay for a correct pole dead indication. See Figure 59 and Figure 60.*

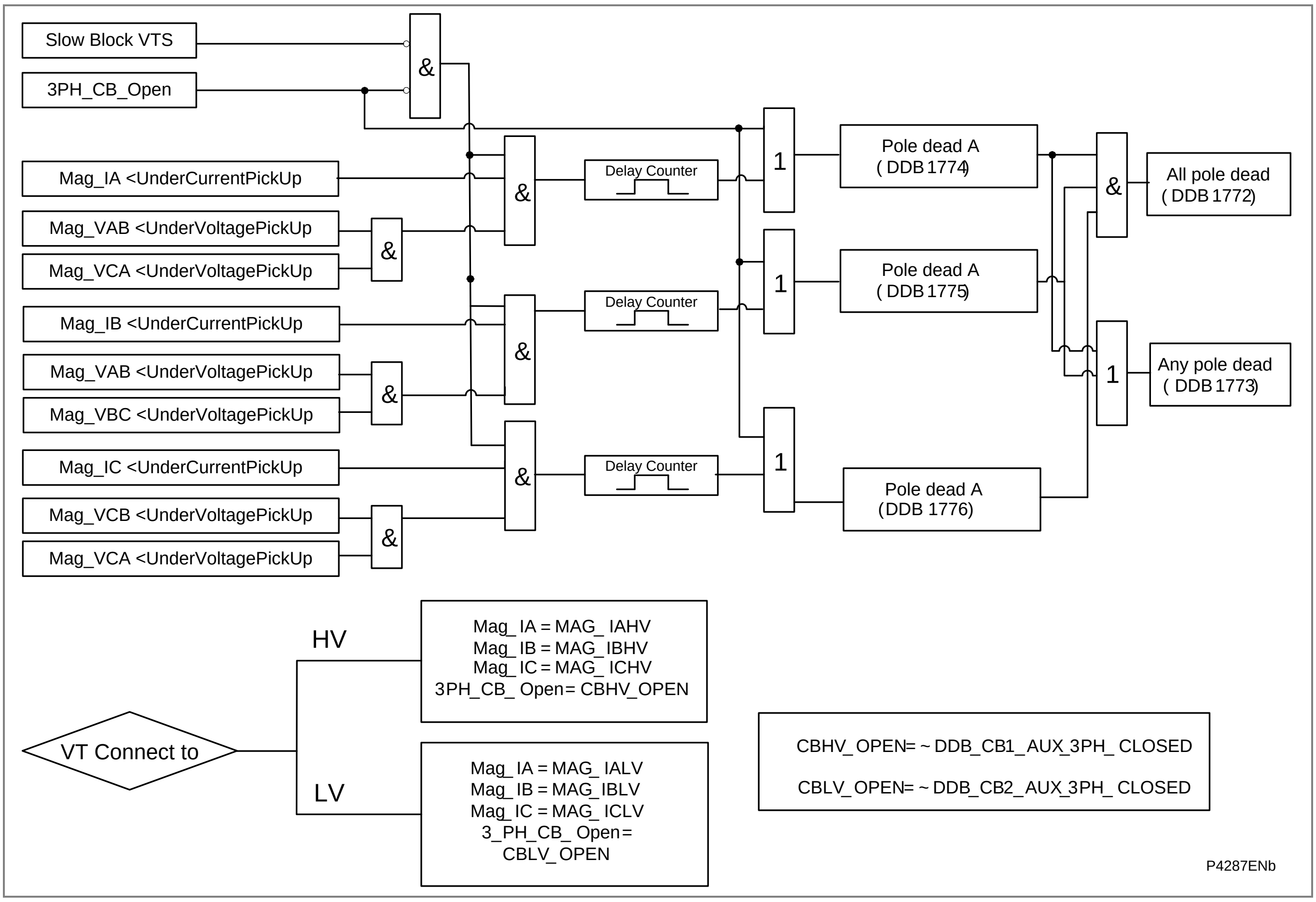
Slow Block VTS
3PH_CB_Open
&
Mag_IA <UnderCurrentPickUp
Mag_VAB <UnderVoltagePickUp
Mag_VCA <UnderVoltagePickUp
Mag_IB <UnderCurrentPickUp
Mag_VAB <UnderVoltagePickUp
Mag_VBC <UnderVoltagePickUp
Mag_IC <UnderCurrentPickUp
Mag_VCB <UnderVoltagePickUp
Mag_VCA <UnderVoltagePickUp
Delay Counter
1
Pole dead A (DDB 1774)
Pole dead A (DDB 1775)
Pole dead A (DDB 1776)
All pole dead (DDB 1772)
Any pole dead (DDB 1773)
VT Connect to
HV
LV
Mag_IA = MAG_IAHV
Mag_IB = MAG_IBHV
Mag_IC = MAG_ICHV
3PH_CB_Open = CBHV_OPEN
Mag_IA = MAG_IALV
Mag_IB = MAG_IBLV
Mag_IC = MAG_ICLV
3_PH_CB_Open = CBLV_OPEN
CBHV_OPEN = ~ DDB_CB1_AUX_3PH_CLOSED
CBLV_OPEN = ~ DDB_CB2_AUX_3PH_CLOSED
P4287ENb

Figure 60 - P642 Pole dead logic

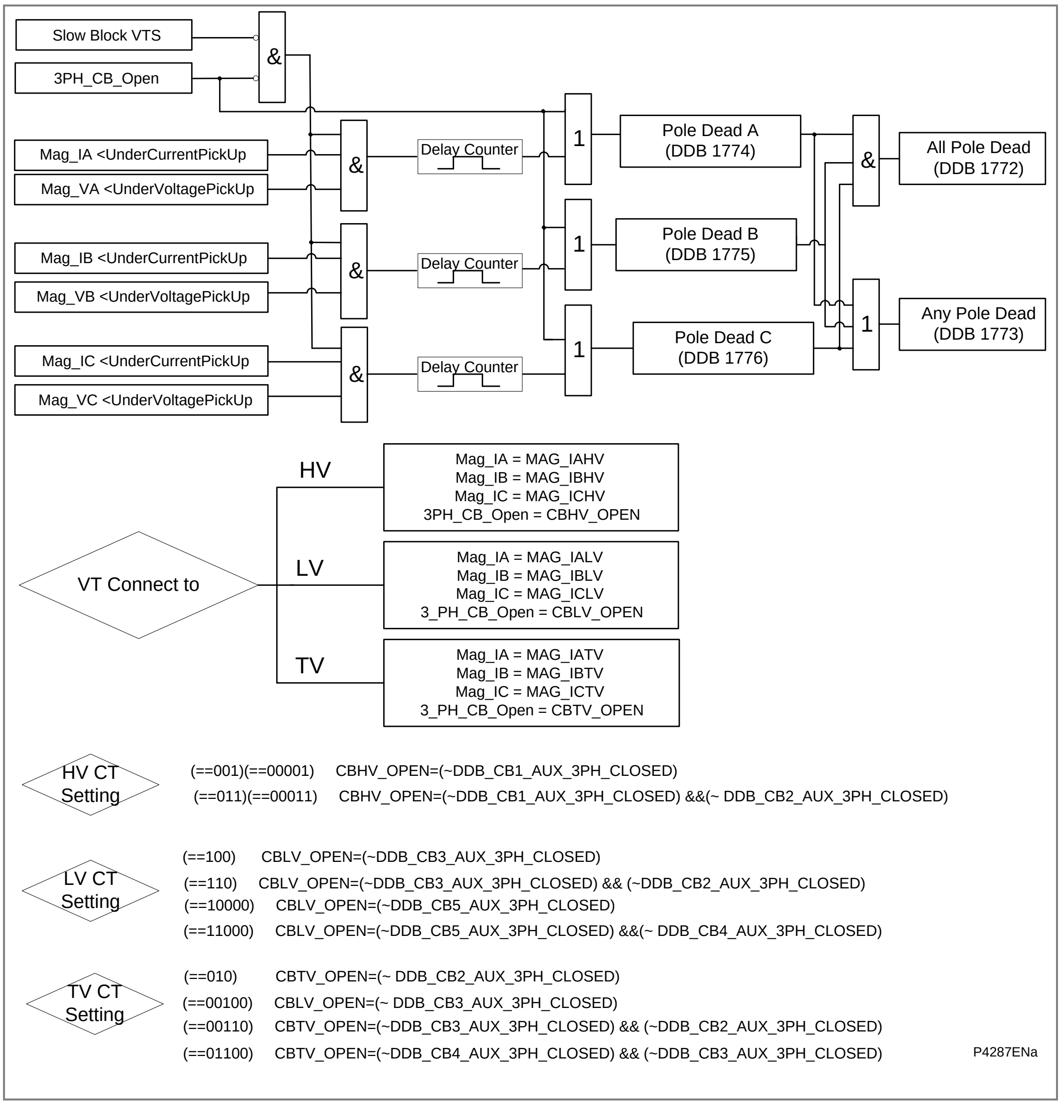
Slow Block VTS
3PH_CB_Open
&
Mag_IA <UnderCurrentPickUp
Mag_VA <UnderVoltagePickUp
&
Delay Counter
1
Pole Dead A (DDB 1774)
Mag_IB <UnderCurrentPickUp
Mag_VB <UnderVoltagePickUp
&
Delay Counter
1
Pole Dead B (DDB 1775)
Mag_IC <UnderCurrentPickUp
Mag_VC <UnderVoltagePickUp
&
Delay Counter
1
Pole Dead C (DDB 1776)
&
All Pole Dead (DDB 1772)
1
Any Pole Dead (DDB 1773)
VT Connect to
HV
Mag_IA = MAG_IAHV
Mag_IB = MAG_IBHV
Mag_IC = MAG_ICHV
3PH_CB_Open = CBHV_OPEN
LV
Mag_IA = MAG_IALV
Mag_IB = MAG_IBLV
Mag_IC = MAG_ICLV
3_PH_CB_Open = CBLV_OPEN
TV
Mag_IA = MAG_IATV
Mag_IB = MAG_IBTV
Mag_IC = MAG_ICTV
3_PH_CB_Open = CBTV_OPEN
HV CT Setting
(==001)(==00001) CBHV_OPEN=(~DDB_CB1_AUX_3PH_CLOSED)
(==011)(==00011) CBHV_OPEN=(~DDB_CB1_AUX_3PH_CLOSED) &&(~ DDB_CB2_AUX_3PH_CLOSED)
LV CT Setting
(==100) CBLV_OPEN=(~DDB_CB3_AUX_3PH_CLOSED)
(==110) CBLV_OPEN=(~DDB_CB3_AUX_3PH_CLOSED) && (~DDB_CB2_AUX_3PH_CLOSED)
(==10000) CBLV_OPEN=(~DDB_CB5_AUX_3PH_CLOSED)
(==11000) CBLV_OPEN=(~DDB_CB5_AUX_3PH_CLOSED) &&(~ DDB_CB4_AUX_3PH_CLOSED)
TV CT Setting
(==010) CBTV_OPEN=(~ DDB_CB2_AUX_3PH_CLOSED)
(==00100) CBLV_OPEN=(~ DDB_CB3_AUX_3PH_CLOSED)
(==00110) CBTV_OPEN=(~DDB_CB3_AUX_3PH_CLOSED) && (~DDB_CB2_AUX_3PH_CLOSED)
(==01100) CBTV_OPEN=(~DDB_CB4_AUX_3PH_CLOSED) && (~DDB_CB3_AUX_3PH_CLOSED)
P4287ENa

Figure 61 - P643/P645 Pole dead logic

If one or more poles are dead, the relay will indicate which phase is dead and will also assert the ANY POLE DEAD DDB signal (DDB 1773). If all phases were dead the ANY POLE DEAD signal would be accompanied by the ALL POLE DEAD DDB signal (DDB 1772).

In the event that the VT fails a signal is taken from the VTS logic (DDB 1801 - Slow Block) to block the pole dead indications that would be generated by the undervoltage and undercurrent thresholds. However, the VTS logic will not block the pole dead indications if they are initiated by a CB Open signal.

Note	*When no auxiliary contacts are available, the 3PH_CB_OPEN signal must be forced low to avoid a wrong indication of a pole dead condition.*

The 3PH_CB_Open signal is the output of an AND gate. The inputs of this AND gate are the statuses of the breakers associated with the winding where the pole dead logic is available. When no auxiliary contacts are available, the 3PH_CB_Open signal shown in the pole dead logic diagram must be forced low, so that valid all pole dead (DDB 1772) and any pole dead (DDB 1773) conditions are given. In the programmable scheme logic, the relay only has CB closed signals (DDBs 719, 721, 723, 725, 727). If there are no auxiliary breaker contacts, the CB closed signals should be forced high, so that the 3PH_CB_Open signal is low. If the 3PH_CB_Open signal is low, and the VTS Slow Block

(DDB 1801) is also low, the relay checks on the currents and voltages to detect an all pole or any pole dead condition.

Figure 61 shows a way of forcing the CB closed signals high when there are no auxiliary contacts.

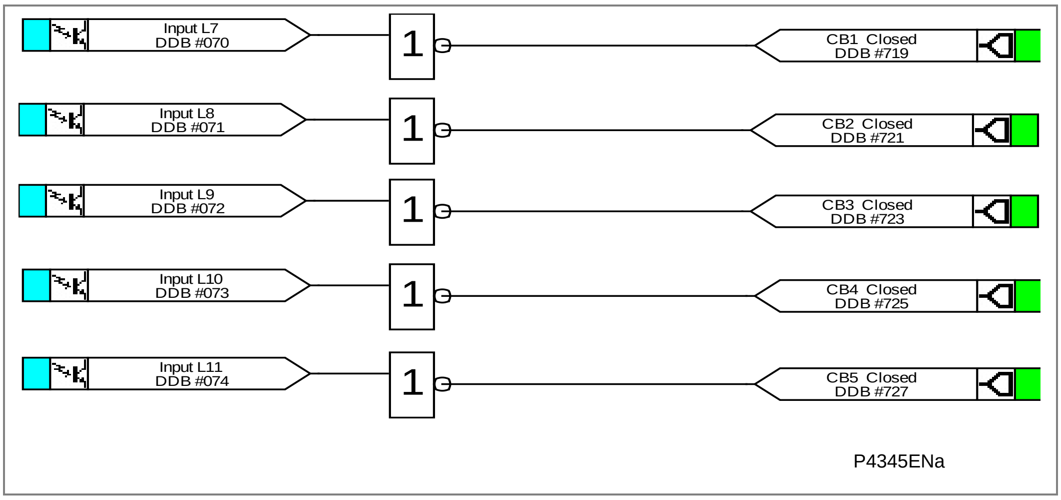
Input L7
DDB #070
Input L8
DDB #071
Input L9
DDB #072
Input L10
DDB #073
Input L11
DDB #074
1
1
1
1
1
CB1 Closed
DDB #719
CB2 Closed
DDB #721
CB3 Closed
DDB #723
CB4 Closed
DDB #725
CB5 Closed
DDB #727
P4345ENa

Figure 62 - P643/P645 Pole dead logic - CB closed signals

It is important to notice that in the absence of auxiliary breaker contacts, the CB close signals should be forced high. If not, the logic will assert the “all pole dead” and “any pole dead” signals when the winding may still be energized.

3.5 User Alarms

Thirty two user alarms are available, and each one can be set as self-reset or manual reset. The user alarm labels can be set in the setting file and these labels are displayed in the psl file as well.

3.6 Changing Setting Groups

The setting groups can be changed using 2 DDB signals or by a menu selection or by using the hotkey menu. In the **Configuration** column if **Setting Group - select via PSL** is selected, DDBs 885 (SG Select 1x) and 884 (SG Select x1), which are dedicated for setting group selection, can be used to select the setting group as shown in the table below. These DDB signals can be connected to opto inputs for local selection or control inputs for remote selection of the setting groups. If **Setting Group - select via menu** is selected, in the **Configuration** column the **Active Settings - Group1/2/3/4** can be used to select the setting group. The setting group can be changed using the hotkey menu providing that **Setting Group - select via menu** is chosen.

SG select 1x	SG select x1	Selected setting group
0	0	1
0	1	2
1	0	3
1	1	4

Table 27 - Setting Group select

Note *Setting groups comprise both Settings and Programmable Scheme Logic. Each is independent per group - not shared as common. The settings are generated in the Settings and Records application in MiCOM S1 Studio, or can be applied directly from the relay front panel menu. The programmable scheme logic can only be set using the PSL Editor application in MiCOM S1 Studio, generating files with extension ".psl".*

Warning **It is essential that where the installation needs application-specific PSL that the appropriate .psl file is downloaded (sent) to the relay, for each and every setting group that will be used. If the user fails to download the required .psl file to any setting group that may be brought into service, then factory default PSL will still be resident. This may have severe operational and safety consequences.**

3.7 Control Inputs

The control inputs function as software switches that can be set or reset either locally or remotely. These inputs can be used to trigger any function that they are connected to as part of the PSL. There are three setting columns associated with the control inputs which are: **CONTROL INPUTS**, **CTRL I/P CONFIG** and **CTRL I/P LABELS**. The function of these columns is described below:

Menu text	Default setting	Setting range	Step size
CONTROL INPUTS			
Ctrl I/P Status	00000000000000000000000000000000		
Control Input 1	No Operation	No Operation, Set, Reset	
Control Input 2 to 32	No Operation	No Operation, Set, Reset	

Table 28 - Control inputs

The Control Input commands can be found in the Control Input menu. In the Ctrl I/P status menu cell there is a 32 bit word which represents the 32 control input commands. The status of the 32 control inputs can be read from this 32 bit word. The 32 control inputs can also be set and reset from this cell by setting a 1 to set or 0 to reset a particular control input. Alternatively, each of the 32 Control Inputs can be set and reset using the individual menu setting cells Control Input 1, 2, 3, and so on. The Control Inputs are available through the relay menu as described above and also using the rear communications.

In the programmable scheme logic editor 32 Control Input signals, DDB 1824 - 1855, which can be set to a logic 1 or On state, as described above, are available to perform control functions defined by the user.

The status of the Control Inputs configured as latched is stored in flash memory. Therefore, in the event that the auxiliary supply is interrupted, the status of the control inputs is recorded even if the battery is missing or discharged. Once the auxiliary supply is restored, the control input is set to the same status as before the auxiliary supplied failed.

Menu text	Default setting	Setting range	Step size
CTRL I/P CONFIG			
Hotkey Enabled	11111111111111111111111111111111		
Control Input 1	Latched	Latched, Pulsed	
Ctrl Command 1	SET/RESET	SET/RESET, IN/OUT, ENABLED/DISABLED, ON/OFF	

Menu text	Default setting	Setting range	Step size
CTRL I/P CONFIG			
Control Input 2 to 32	Latched	Latched, Pulsed	
Ctrl Command 2 to 32	SET/RESET	SET/RESET, IN/OUT, ENABLED/DISABLED, ON/OFF	

Table 29 - Ctrl I/P Config

Menu text	Default setting	Setting range	Step size
CTRL I/P LABELS			
Control Input 1	Control Input 1	16 character text	
Control Input 2 to 32	Control Input 2 to 32	16 character text	

Table 30 - Ctrl I/P labels

The CTRL I/P CONFIG column has several functions, one of which allows the user to configure the control inputs as either latched or pulsed. A latched control input will remain in the set state until a reset command is given, either by the menu or the serial communications. A pulsed control input, however, will remain energized for 10 ms after the set command is given and will then reset automatically (no reset command is required).

In addition to the latched/pulsed option this column also allows the control inputs to be individually assigned to the “Hotkey” menu by setting **1** in the appropriate bit in the **Hotkey Enabled** cell. The hotkey menu allows the control inputs to be set, reset or pulsed without the need to enter the **CONTROL INPUTS** column. The **Ctrl Command** cell also allows the **SET/RESET** text, displayed in the hotkey menu, to be changed to something more suitable for the application of an individual control input, such as **ON / OFF** or **IN / OUT**.

The **CTRL I/P LABELS** column makes it possible to change the text associated with each individual control input. This text will be displayed when a control input is accessed by the hotkey menu, or it can be displayed in the PSL.

3.8 PSL DATA Column

The MiCOM P64x range of relays contains a PSL DATA column that can be used to track PSL modifications. A total of 12 cells are contained in the PSL DATA column, 3 for each setting group. The function for each cell is shown below:

Grp PSL Ref	When downloading a PSL to the relay, the user will be prompted to enter which groups the PSL is for and a reference ID. The first 32 characters of the reference ID will be displayed in this cell. The ◁ and ▷ keys can be used to scroll through 32 characters as only 16 can be displayed at any one time.
18 Nov 2002 08:59:32.047	This cell displays the date and time when the PSL was down loaded to the relay.
Grp 1 PSL ID - 2062813232	This is a unique number for the PSL that has been entered. Any change in the PSL will result in a different number being displayed.

Note *The above cells are repeated for each setting group.*

Table 31 - PSL Data column

3.9 Auto Reset of Trip LED Indication

The trip LED can be reset when the flags for the last fault are displayed. The flags are displayed automatically after a trip occurs, or can be selected in the fault record menu. The reset of trip LED and the fault records is performed by pressing the ⓒ key once the fault record has been read.

Setting **Sys Fn Links** in the **SYSTEM DATA** Column to logic **1** sets the trip LED to automatic reset. Resetting will occur when the circuit is reclosed and the **Any Pole Dead** signal (DDB 1773) has been reset for three seconds. Resetting, however, will be prevented if the **Any start** signal is active after the breaker closes.

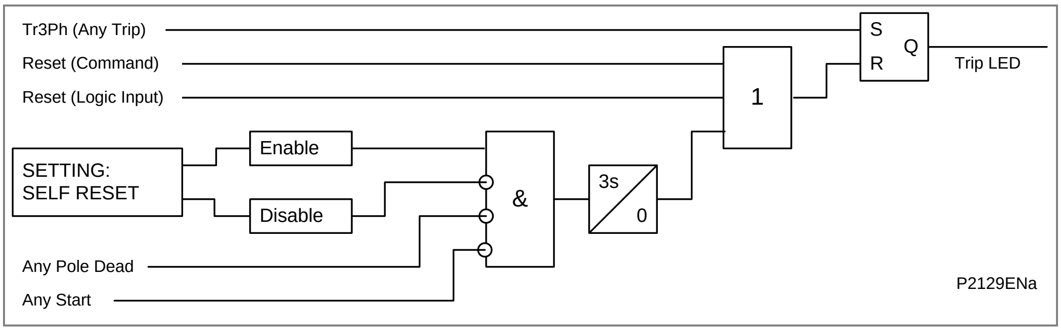

Figure 63 - Trip LED logic diagram

3.10 Reset of Programmable LEDs and Output Contacts

The programmable LEDs and output contacts can be set to be latched in the programmable scheme logic. If there is a fault record then clearing the fault record by pressing the ⓒ key once the fault record has been read will clear any latched LEDs and output contacts. If there is no fault record, then as long as the initiating signal to the LED or output contact is reset the LEDs and contacts can be reset by one of these methods.

- Using the View Records - Reset Indications menu command cell
- Using DDB 876 **Reset Relays/LED** which can be mapped to an Opto Input or a Control Input for example

3.11 Real Time Clock Synchronization via Opto-Inputs

In modern protective schemes it is often desirable to synchronize the relays real time clock so that events from different relays can be placed in chronological order. This can be done using the IRIG-B input, if fitted, or via the communication interface connected to the substation control system. In addition to these methods the P64x range offers the facility to synchronize using an opto-input by routing it in PSL to DDB 881 (Time Sync.). Pulsing this input will result in the real time clock snapping to the nearest minute if the pulse input is ±3 s of the relay clock time. If the real time clock is within 3 s of the pulse the relay clock will crawl (the clock will slow down or get faster over a short period) to the correct time. The recommended pulse duration is 20 ms to be repeated no more than once per minute. An example of the time sync. function is shown below:

Time of “Sync. Pulse”	Corrected time
19:47:00 to 19:47:29	19:47:00
19:47:30 to 19:47:59	19:48:00
Note The above assumes a time format of hh:mm:ss	

Table 32 - Time Sync function

To avoid the event buffer from being filled with unnecessary time sync. events, it is possible to ignore any event that generated by the time sync. opto input. This can be done by applying the following settings:

Menu text	Value
RECORD CONTROL	
Opto Input Event	Enabled
Protection Event	Enabled
DDB 63 - 32 (Opto Inputs)	Set “Time Sync.” associated opto to 0

Table 33 - Record control

To improve the recognition time of the time sync. opto input by approximately 10 ms, the opto input filtering could be disabled. This is achieved by setting the appropriate bit to 0 in the Opto Filter Cntl cell in the OPTO CONFIG column.

Disabling the filtering may make the opto input more susceptible to induced noise. Fortunately the effects of induced noise can be minimized by using the methods described in the *Firmware Design* chapter *P64x/EN FD.*

3.12 Function Keys

The P643/P645 relay offers users 10 function keys for programming any operator control functionality such as Reset latched Relays/LEDS/Alarms, Select Group 2 using the PSL. Each function key has an associated programmable tri-color LED that can be programmed to give the desired indication on function key activation.

These function keys can be used to trigger any function that they are connected to as part of the PSL. The function key commands can be found in the ‘Function Keys’ menu (see the Settings chapter, *P64x/EN ST*). In the **Fn. Key Status** menu cell there is a 10-bit word which represent the 10 function key commands and their status can be read from this 10-bit word.

In the programmable scheme logic editor 10 function key signals, DDB 352 - 361, which can be set to a logic 1 or On state, as described above, are available to perform control functions defined by the user.

The **Function Key**s column has the **Fn. Key n Mode** cell which allows the user to configure the function key as either **Toggled** or **Normal**. In the **Toggle** mode the function key DDB signal output will remain in the set state until a reset command is given, by activating the function key on the next key press. In the **Normal** mode, the function key DDB signal will remain energized for as long as the function key is pressed and will then reset automatically. A minimum pulse duration can be programmed for a function key by adding a minimum pulse timer to the function key DDB output signal.

The **Fn. Key n Status** cell is used to enable/unlock or disable the function key signals in PSL. The **Lock** setting has been specifically provided to allow the locking of a function key thus preventing further activation of the key on consequent key presses.

This allows function keys that are set to **Toggled** mode and their DDB signal active ‘high’, to be locked in their active state thus preventing any further key presses from deactivating the associated function. Locking a function key that is set to the **Normal** mode causes the associated DDB signals to be permanently off. This safety feature prevents any inadvertent function key presses from activating or deactivating critical relay functions.

The **Fn. Key Labels** cell makes it possible to change the text associated with each individual function key. This text will be displayed when a function key is accessed in the function key menu, or it can be displayed in the PSL.

The status of the function keys is stored in flash memory. In the event that the auxiliary supply is interrupted the status of all the function keys will be recorded. Therefore, in the event that the auxiliary supply is interrupted, the status of the function keys is recorded even if the battery is missing or discharged. Once the auxiliary supplied is restored, the function key is set to the same status as before the auxiliary supplied failed. Please also note the relay will only recognize a single function key press at a time and minimum key press duration of approximately 200 msec. is required before the key press is recognized in PSL. This de-glitching feature avoids accidental double key presses.

APPLICATION NOTES

CHAPTER NO 6

Date:	12/2013
Hardware Suffix:	J (P642) K (P643/P645)
Software Version:	04
Connection Diagrams:	10P642xx (xx = 1 to 10) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9)

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Notes:

1 INTRODUCTION

1.1 Transformer Protection

1.1.1 Introduction

The development of modern power systems has been reflected in the advances in transformer design. This has resulted in a wide range of transformers with power rating from a few kVA to several hundred MVA being available for use in a wide variety of applications.

The considerations for transformer protection vary with the application and importance of the transformer. To reduce the effects of thermal stress and electrodynamic forces, the overall protection should minimize the time that a fault is present within a transformer.

On smaller distribution transformers, effective and economically justifiable protection can be achieved by using either fuse protection or IDMT/instantaneous overcurrent relays. Due to the requirements of co-ordination with the downstream power system protection, this results in time-delayed fault clearance for some low-level faults. Time delayed clearance of major faults is unacceptable on larger distribution, transmission and generator transformers, where the effects on system operation and stability must be considered. High speed protection is desirable for all faults.

Transformer faults are generally classified into these categories:

- Winding and terminal faults
- Core faults
- Abnormal operating conditions such as overvoltage, overfluxing and overload
- Sustained or uncleared external faults

All of the above conditions must be considered individually and the transformer protection designed accordingly.

To provide effective protection for faults within a transformer and security for normal operation and external faults, the design and application of transformer protection must consider factors such as:

- Magnetizing inrush current
- Winding arrangements
- Winding connections
- Connection of protection secondary circuits

The way that the protection of larger transformers is typically achieved is best illustrated by examining the protective devices associated with common applications.

1.1.2 Transformer Connections

There are several possible transformer connections but the more common connections are divided into the main groups shown in Table 1:

Group	Phase displacement	Transformer connections
Group 1	0° Phase displacement	Yy0 or Dz0 or Dd0
Group 2	180° Phase displacement	Yy6 or Dd6 or Dz6
Group 3	30° lag Phase displacement	Dy1 or Yz1 or Yd1
Group 4	30° lead Phase displacement	Yd11 or Dy11 or Yz11

Table 1 - Four main transformer connection groups

High voltage windings are indicated by capital letters and low voltage windings by lower-case letters (reference to high and low is relative). The numbers refer to positions on a clock face and indicate the phase displacement of the low voltage phase to neutral vector with respect to the high voltage phase to neutral vector. For example, Yd1 indicates that the low voltage phase vectors lag the high voltage phase vectors by 30° (-30° phase shift).

Determining transformer connections is best shown with a particular example. These points should be noted:

- The line connections are normally made to the end of the winding which carries the subscript 2, such as: A2, B2, C2 and a2, b2, c2.
- The line terminal designation (both letter and subscript) are the same as those of the phase winding to which the line terminal is connected.

Consider the Yd1 connection. The transformer windings shown in Figure 1 should be connected in Yd1 configuration.

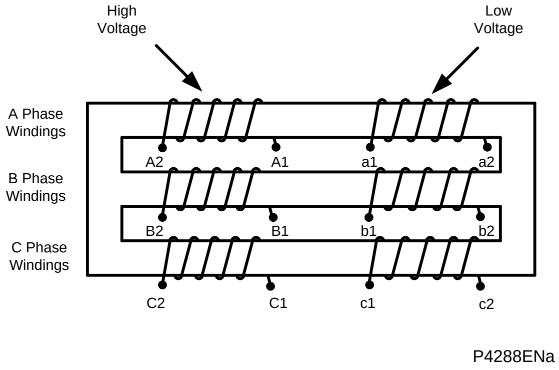


Figure 1 - Transformer windings to be connected in Yd1 configuration

Follow these steps to connect the transformer windings:

1. Draw the primary and secondary phase to neutral vectors showing the required phase displacement.

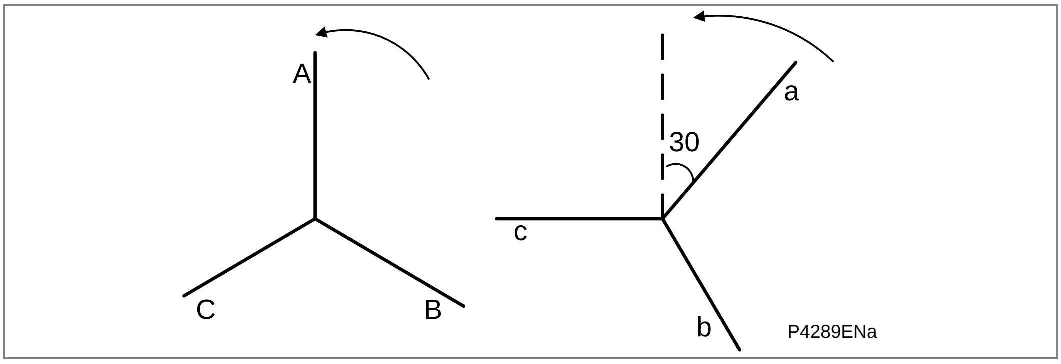

A
C
B
a
30
c
b
P4289ENa

Figure 2 - Phase-neutral voltage vectors

2. Complete the delta winding connection on the secondary side and indicate the respective vector directions. Magnetically coupled windings are drawn in parallel, winding “A” in the star side is parallel to winding “a” in the delta side. The same applies for the other two phases.

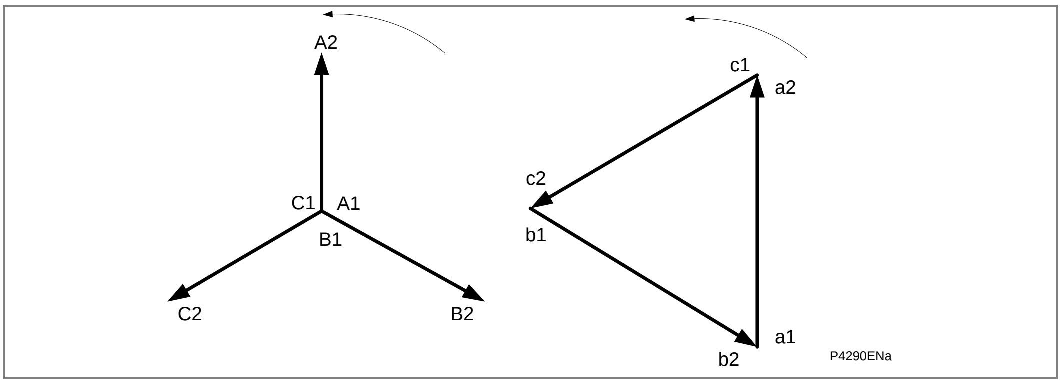

A2
C1
A1
B1
C2
B2
c1
a2
c2
b1
a1
b2
P4290ENa

Figure 3 - Draw the delta

3. It is now possible to indicate the winding subscript numbers, bearing in mind that if the direction of induced voltage in the high voltage winding at a given instant is from A1 to A2 (or vice versa) then the direction of the induced voltage in the low voltage winding at the same instant will also be from a1 to a2.

4. It can now be seen that the delta connection should be made by connecting a2 to c1, b2 to a1 and c2 to b1:

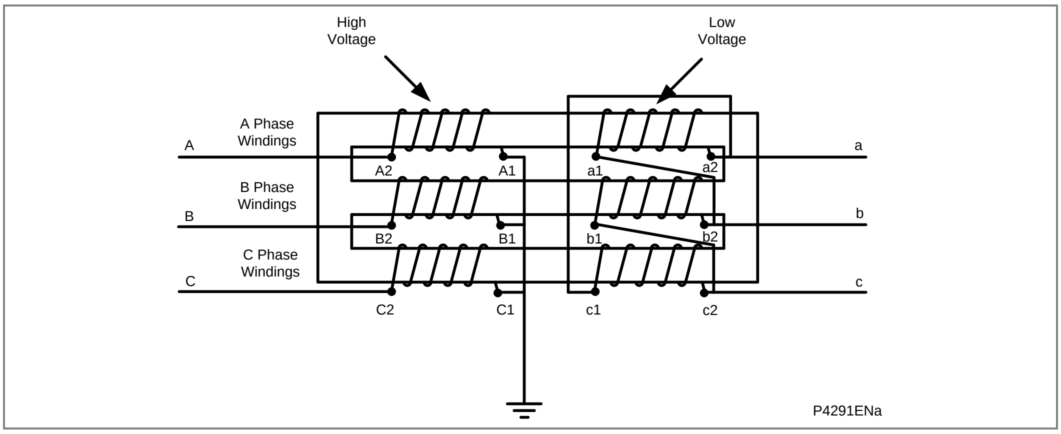

High Voltage
Low Voltage
A Phase Windings
A
B Phase Windings
B
C Phase Windings
C
A2
A1
a1
a2
B2
B1
b1
b2
C2
C1
c1
c2
a
b
c
P4291ENa

Figure 4 - Yd1 transformer configuration

1.1.3 Overview of Existing Practices

Figure 5 shows typical protection functions for a sub-transmission or large distribution transformer.

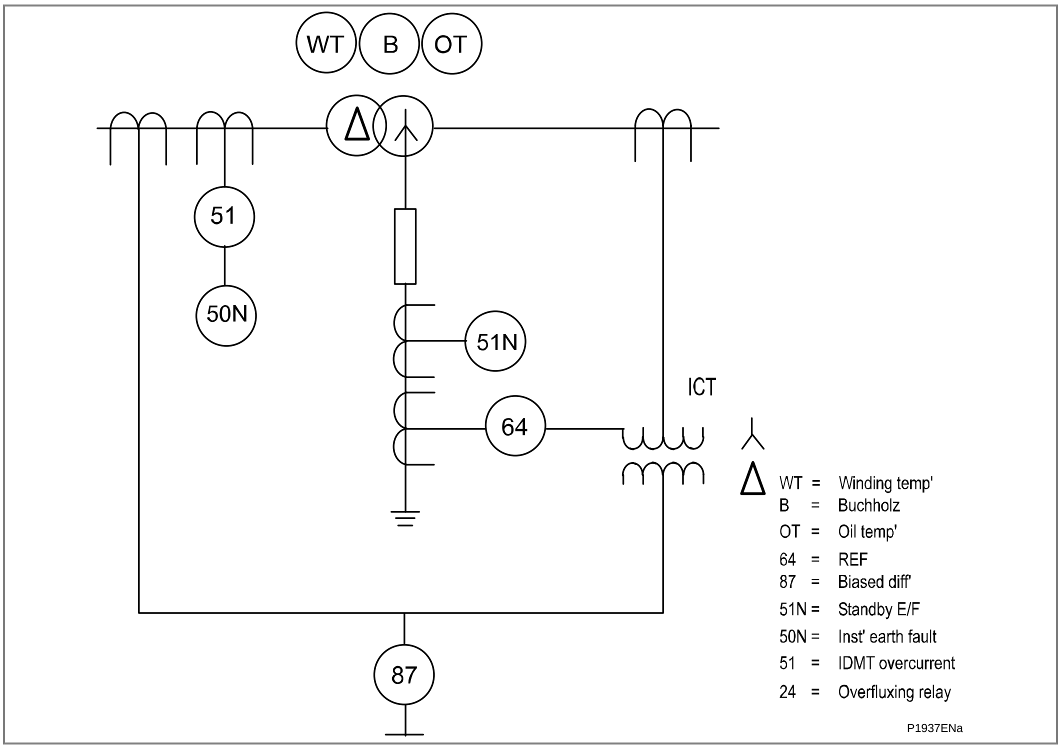


Figure 5 - Typical transformer protection package

High speed protection is provided for faults on both the HV and LV windings by biased differential protection (87). The relay operates on the basic differential principle that HV and LV CT secondary currents entering and leaving the zone of protection can be balanced under load and through fault conditions, whereas under internal fault conditions balance will be lost and a differential current will cause the relay to trip. The zone of protection is clearly defined by the CT locations and, as the protection is stable for through faults, it can be set to operate without any intentional time delay.

Figure 6 shows the application of the P64x differential relay with software vector group and amplitude matching. This provides phase and ratio correction of CT signals in addition to filtering LV zero sequence current to prevent maloperation of the differential element for external LV earth faults. Interposing CTs (ICTs) are no longer required.

More sensitive high speed earth fault protection for the LV winding is provided by restricted earth fault protection (64). Due to the limitation of phase fault current on the HV side for LV winding earth faults, and the fact that any unrestricted earth fault protection in the transformer earth path requires a discriminative time delay, restricted earth fault protection is widely applied.

Earth fault protection is provided on the HV winding by the inherently restricted earth fault element associated with the HV overcurrent protection (50N). The delta winding of the transformer draws no HV zero sequence current for LV earth faults and passes no zero sequence current to upstream HV earth faults. Therefore there is no requirement to grade this element with other earth fault protection and it can be set to operate without any intentional time delay. For delta windings this is known as balanced earth fault protection.

Sustained external LV faults are cleared by the IDMT overcurrent protection on the HV winding (51) or by the standby earth fault protection (51N) in the transformer earth connection. The extent of backup protection used will vary according to the transformer installation and application.

The protection scheme may be further enhanced by the use of other protective devices associated with the transformer, such as the Buchholz, pressure relief and winding temperature devices. These devices can act as another main protective system for large transformers. They may also provide clearance for some faults which might be difficult to detect by protection devices operating from line current transformers, for example, winding inter turn faults or core lamination faults. These devices are connected to directly trip the breaker in addition to operating auxiliary relays for indication purposes.

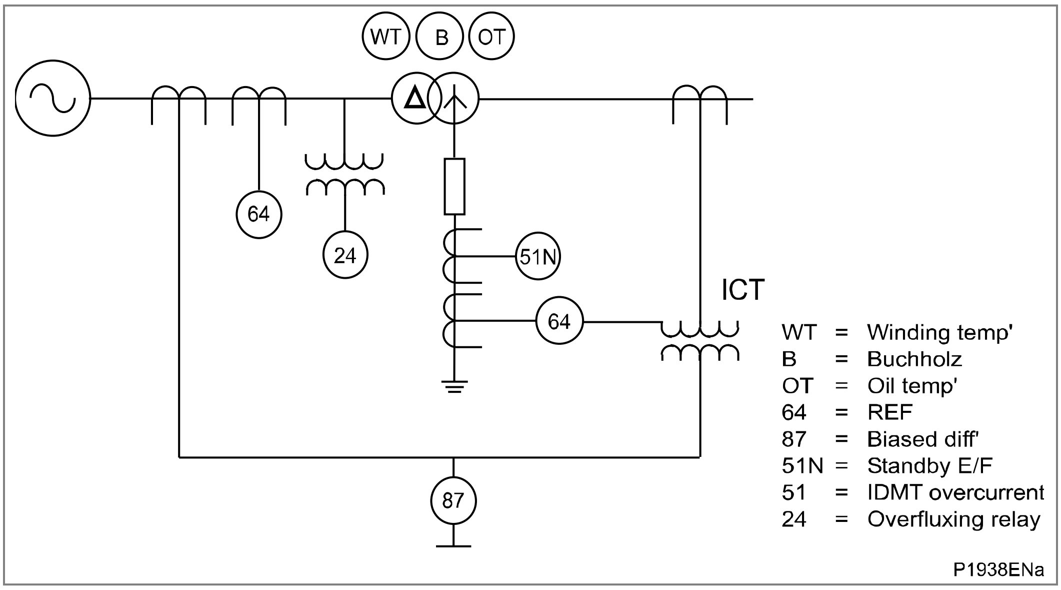


Figure 6 - Typical protection package for a transformer

The protection of a generator transformer is similar to that for any other large transformer.

High speed protection is provided for phase to phase faults by the provision of biased differential protection. In addition, for large generators, the transformer is commonly included within an overall second main differential arrangement, which incorporates the generator and transformer within the overall zone of protection. Earth fault protection is provided by a restricted earth fault element on the star winding.

Overfluxing protection is commonly applied to generator circuits to prevent generator or transformer damage from prolonged overfluxing conditions.

Other protection devices will again complement the main relay protection.

Auto-transformers are commonly used to couple EHV and HV power networks if the ratio of their voltages is moderate. The protection arrangements for an auto-transformer are similar in most respects to the protection of a two-winding transformer. Protection of all windings can be offered by a biased differential relay such as the P64x.

1.2 P64x Protection Relay

The P64x relay has been designed to bring the latest numerical technology to the protection of power transformers. The increased functionality of numerical relays allows enhanced protection functions to be offered for a wide variety of applications, which, when combined with a host of non-protective features, can provide power system control and monitoring requirements.

1.2.1 Protection Functions

The main protection functions offered by the P64x are listed below:

- Biased differential protection (87)
- Restricted earth fault protection for individual transformer windings (64)
- Directional/non-directional instantaneous/time delayed phase overcurrent protection (50/51)
- Derived/measured, directional/non-directional, instantaneous/time delayed earth fault protection (50N/51N)
- Directional/non-directional, instantaneous/time delayed negative phase sequence overcurrent protection (46)
- Thermal overload protection (49)
- Under/overvoltage and residual overvoltage protection (27/59/59N)
- Under/overfrequency protection (81)
- Overfluxing protection (24)
- Stub bus/Winding overcurrent. It is only available in P643/P645.
- Breaker failure
- Opto-isolated inputs and programmable logic for alarm/trip indication of external devices

Note	*Directional overcurrent elements, under/overvoltage and residual overvoltage elements are available on request of the three-phase VT input.*

The biased differential element has a triple slope bias characteristic to ensure sensitivity, with load current, to internal faults and stability under heavy through-fault conditions.

The differential element can be blocked for magnetizing inrush conditions, based on the ratio of second harmonic to fundamental current. Also the differential element can be blocked during transient overfluxing conditions, based on the ratio of fifth harmonic to fundamental current. Fast operating times for heavy internal faults can be achieved using the unrestrained instantaneous differential high set elements.

Restricted earth fault protection, based on the low/high impedance principle, is available for up to three transformer windings to offer increased sensitivity to low-level winding earth faults.

Three four-stage overcurrent protection elements are provided for each transformer winding. Three four-stage earth fault protection elements are provided based on the neutral current of every winding. Therefore each winding has its dedicated earth fault protection elements. The user can select between measured neutral current and derived neutral current. Three four-stage negative phase sequence overcurrent protection elements are provided for each transformer winding.

Thermal overload protection can be used to prevent equipment from operating at temperatures in excess of the designed maximum withstand. Prolonged overloading causes excessive heating, which may result in premature ageing of the insulation, or in extreme cases, insulation failure. The thermal overload protection is based on IEEE Standard C57.91-1995. The trip command is based on either the hot spot temperature or the top oil temperature, each one with three time-delayed stages.

Transformer loads are becoming increasingly non-linear, causing increased current harmonics. Since increased harmonics content raise the winding temperature, the relay incorporates a current based thermal replica, using rms load current to model heating and cooling of the protected transformer. The element can be set with both alarm and trip stages.

The V/f overfluxing element provides protection against transformer damage which may result from prolonged operation at increased voltages or decreased frequency, or both. Independent alarm and trip characteristics are provided to enable corrective action to be undertaken before tripping is initiated.

Stub bus protection is used in a one and a half breaker scheme. When the disconnector associated to a winding is open, the differential, REF, breaker failure and differential CTS elements related to the open winding are affected. The output of the stub bus detection logic can be used to change the trip logic and to trigger an indication if necessary.

It is common practice to install Circuit Breaker Failure (CBF) protection to monitor that the circuit breaker has opened within a reasonable time after the main protection has tripped. If the fault current has not been interrupted following a set time delay from circuit breaker trip initiation, CBF protection will operate. CBF operation can be used to backtrip upstream circuit breakers to ensure that the fault is isolated correctly. CBF operation can also reset all start output contacts, ensuring that any blocks asserted on upstream protection are removed.

Use of the opto-inputs as trip repeat and alarm paths for other transformer protection devices, (Buchholz, Oil pressure, winding temperature) allows operation of these devices to be event-logged. Interrogation of the relay fault, event and disturbance records offers an overall picture of an event or fault, of the transformer protection performance and sequences of operation.

All models of the P64x are three phase units with internal phase compensation, CT ratio correction and zero sequence filtering, eliminating the need for external interposing transformers. Up to five biased inputs can be provided to cater for power transformers with more than two windings or more than one set of CTs associated with each winding, such as in mesh or one-and-a-half circuit breaker substation arrangements.

The variety of protective functions offered by the P64x makes it ideal not only for the protection of power transformers but also for a variety of applications where biased differential is commonly applied, these include:

- Overall generator/transformer protection
- Generators
- Reactors
- Motors

1.2.2 Non-Protection Features

In addition to providing all of the common relaying requirements for a transformer protection package, the P64x relay shares many common features with the other relays in the MiCOM range.

The P64x offers this variety of additional features due to its digital design and standardization of hardware. These features are listed below:

- Loss of life statistic
- Through-fault monitoring
- CT and VT supervision
- Pole dead. It is only available in P643/P645 on request of the 3 phase VT input
- Fault records (summary of reasons for tripping)
- Event records (summary of alarms and relay events)

- Disturbance records (record of analogue waveforms and operation of opto-inputs and output relays)
- Date and time tagging of all records
- Setting aids
- Remote communications
- High level of continuous self monitoring and diagnostic information

2 APPLICATION OF INDIVIDUAL PROTECTION FUNCTIONS

The following sections detail the individual protection functions in addition to where and how they may be applied. Each section also gives an extract from the respective menu columns to demonstrate how the settings are actually applied to the relay.

2.1 Overall Differential Protection (87)

In applying the well established principles of differential protection to transformers, a variety of considerations have to be taken into account. These include compensation for any phase shift across the transformer, possible unbalance of signals from current transformers either side of the windings and the effects of the variety of earthing (grounding) and winding arrangements. In addition to these factors, which can be compensated for by correct application of the relay, the effects of normal system conditions on relay operation must also be considered. The differential element must be blocked for system conditions which could result in maloperation of the relay, such as high levels of magnetizing current during inrush conditions or during transient overfluxing.

In traditional transformer differential schemes, the requirements for phase and ratio correction were met by the application of external interposing current transformers, as a secondary replica of the main transformer winding arrangements, or by a delta connection of main CTs (phase correction only). The P64x has settings to allow flexible application of the protection to a wide variety of transformer configurations, or to other devices where differential protection is required, without the need for external interposing CTs or delta connection of secondary circuits.

2.1.1 Biased Elements

The P64x percentage bias calculation is performed 8 times per cycle. A triple slope percentage bias characteristic is implemented. Both the flat and the lower slope provide sensitivity for internal faults. Under normal operation steady state magnetizing current and the use of tap changers result in unbalanced conditions and hence differential current. To accommodate these conditions the initial slope, K1, may be set to 30%. This ensures sensitivity to faults while allowing for mismatch when the power transformer is at the limit of its tap range and CT ratio errors. At currents above rated, extra errors may be gradually introduced as a result of CT saturation, Hence, the higher slope may be set to 80% to provide stability under through fault conditions, during which there may be transient differential currents due to saturation effect of the CTs. The through fault current, in all but ring bus or mesh fed transformers, is given by the inverse of the per unit reactance of the transformer. For most transformers, the reactance varies between 0.05 to 0.2 pu, therefore typical through fault current is given by 5 to 20 I_n.

The number of biased differential inputs required for an application depends on the transformer and its primary connections. It is recommended that, where possible, a set of biased CT inputs is used for each set of current transformers. According to IEEE Std. C37.110-2007 separate current inputs should be used for each power source to the transformer. If the secondary windings of the current transformers from two or more supply breakers are connected in parallel, under heavy through fault conditions, differential current resulting from the different magnetizing characteristics of the current transformers flows in the relay. This current only flows through one current input in the relay and can cause misoperation. If each CT is connected to a separate current input, the total fault current in each breaker provides restraint. It is only advisable to connect CT secondary windings in parallel when both circuits are outgoing loads. In this condition, the maximum through fault level is restricted solely by the power transformer impedance.

There are three basic models of the P64x relay:

- P642 Two biased differential inputs
- P643 Three biased differential inputs

- P645 Five biased differential inputs

Where a P643 or P645 is chosen, it can be programmed to provide 2 or 3 biased inputs.

Table 2 shows the variety of connections which can be catered for by the range of P64x relays.

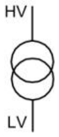
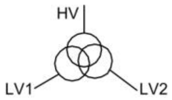
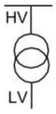
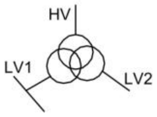
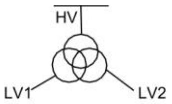
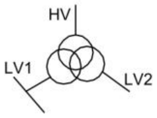
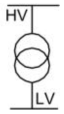
Configuration	No. of CT sets	Recommended relay
	2	P642
	3	P643
	3	P643
	3	P643
	4 or 5	P645
	4 or 5	P645
	4 or 5	P645

Table 2 - Applications of the P64x transformer differential protection relay

The P64x relay achieves stability for through faults in two ways, both of which are essential for correct relay operation. The first consideration is the correct sizing of the current transformers; the second is by providing a relay bias characteristic as shown in Figure 7:

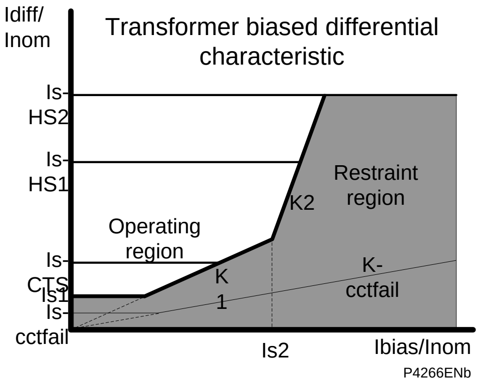


Figure 7 - P64x triple slope (flat, K1, K2) biased differential protection

The flat and lower slope, K1, provides sensitivity for internal faults. The higher slope, K2, provides stability under through fault conditions, during which there may be transient differential currents due to asymmetric CT saturation.

The differential and biased current calculations are done on a per phase basis after amplitude, vector group matching and zero sequence filtering are performed. The following equations are valid for uniformly defined current directions relative to the protected equipment, such that the current directions of all windings are either towards the protected object or away from it.

The differential current, I_{diff}, and the bias current I_{bias} are defined by these expressions:

$$I_{diff} = \left|\vec{I}_1 + \vec{I}_2 + \vec{I}_3 + \vec{I}_4 + \vec{I}_5\right| \qquad I_{bias} = \frac{\left|\vec{I}_1\right| + \left|\vec{I}_2\right| + \left|\vec{I}_3\right| + \left|\vec{I}_4\right| + \left|\vec{I}_5\right|}{2}$$

The differential current, I_{diff}, is the vector sum of the phase currents measured at all ends of the transformer. The mean bias current, I_{bias} is the scalar mean of the magnitude of the currents at all ends of the transformer.

To provide stability for external faults the following measures are taken on the bias calculations:

- **Delayed bias**: the bias quantity is the maximum of the bias quantities calculated within the last cycle. This is to maintain the bias level, providing stability during the time when an external fault is cleared. This feature is implemented on a per phase basis.
- **Transient bias**: an additional bias quantity is introduced into the bias calculation, on a per phase basis, if there is a sudden increase in the mean-bias measurement. This quantity will decay exponentially afterwards. The transient bias is reset to zero once the relay has tripped or if the mean-bias quantity is below the Is1 setting. The transient bias algorithm is executed 8 times per cycle.
- **Maximum bias**: the bias quantity used per phase for the percentage bias characteristic is the maximum delayed bias current calculated from all three phases.

$$Ibias_{(\max)} = Maximum[Ia_{bias}, Ib_{bias}, Ic_{bias}]$$

For the P64x relays the restraining effect (bias current) never disappears when there is an internal fault; the restraining effect is even reinforced. However, the restraining current factor ½ means that the differential current I_d has twice the value of the restraining current I_{bias}, so that safe and reliable tripping is also guaranteed in the case of multi-end infeed for internal faults.

As shown in Figure 7, the tripping characteristic of the differential protection has two knees. The first knee is dependent on the setting of the basic threshold value Is1. The second knee of the tripping characteristic is defined by the setting Is2.

The basic pick up level of the low set differential element, Is1, is dependant on the item of the plant being protected and by the amount of differential current that might be seen during normal operating conditions. A setting of 0.2 pu is generally recommended when the P64x is used to protect a transformer. When protecting generators and other items of the plant, where shunt magnetizing current is not present, a lower differential setting can be used and 0.1 pu is more typical.

The flat section of the tripping curve represents the most sensitive region of the tripping characteristic in the form of the settable basic threshold value Is1. The default setting of 0.2 pu takes into account the steady state magnetizing current of the transformer, which flows even in a no-load condition and is generally less than 5% of the nominal transformer current.

Characteristic equation:

For $Ibias < \frac{Is1}{K1}$

$$Idiff \geq Is1$$

The flat and K1 slopes of the tripping curve cover the load current range, so that in these sections we must account for not only the transformer steady state magnetizing current, which appears as differential current, but also with differential currents that can be attributed to the transformation errors of the current transformer sets and on load tap changers.

If we calculate the worst case with IEC class 10P current transformers, the maximum allowable amplitude error according to IEC 60044-1 is 3 % for nominal current. The phase-angle error can be assumed to be 2° for nominal current. The maximum allowable total error for nominal current is then obtained, in approximation, as
$(0.03 + \sin 2°) \approx 6.5$ %. If the current is increased to the nominal accuracy limit current, the total error for Class 10P current transformers can be 10 % maximum, as may be the case under heavy fault conditions. Beyond the nominal accuracy limit current, the transformation error can be of any magnitude.

The dependence of the total error of a current transformer on current is therefore non-linear. In the operating current range (the current range below the nominal accuracy limit current) we can expect a worst case total error of approximately 10 % per current transformer set.

The first slope section of the tripping characteristic forms a straight line, the slope of which should correspond to the cumulative total error of the participating current transformer sets and on load tap changer. The curve slope, K1, can be set. The default setting for K1 is 30%.

Characteristic equation:

For $Idiff > Is1$

$$Ibias < Is2$$

$$Idiff \geq K1 \times Ibias$$

The second knee point, Is2, is settable. It has a default setting of 1 pu and must be set in accordance with the maximum possible operating current.

Restraining currents that go beyond the set knee point (Is2) are typically considered as through fault currents. For through fault currents, the third section of the tripping characteristic could therefore be given an infinitely large slope. However, a fault can occur in the transformer differential protected zone, therefore a finite slope K2 is provided for the third section of the tripping curve. The default setting for K2 is 80%.

Characteristic equation:

For $Idiff \geq Is2$

$$Idiff \geq K1 \times Is2 + K2(Ibias - Is2)$$

2.1.2 Ratio Correction

To ensure correct operation of the differential element, it is important that under load and through fault conditions the currents into the differential element of the relay balance. In many cases, the HV and LV current transformer primary ratings will not exactly match the transformer winding rated currents. Ratio correction factors are therefore provided. The CT ratio correction factors are applied to ensure that the signals to the differential algorithm are correct.

A reference power, identical for all windings, is defined in the **S_{ref}** setting cell under the **SYSTEM CONFIG** menu heading. For two-winding arrangements, the nominal power is usually the reference power. For three-winding transformers, the nominal power of the highest-power winding should be set as the reference power. The ratio correction factor for each winding of the transformer is calculated by the P64x on the basis of the set reference power, the set primary nominal voltages of the transformer and the set primary nominal currents of the current transformers.

$$K_{amp,n} = \frac{I_{primCT,nom,n}}{\dfrac{S_{prim,ref}}{\sqrt{3}V_{primCT,nom,n}}}$$

Where:
$K_{amp,n}$ = amplitude matching factor for the respective CT input
$I_{primCT,nom,n}$: primary nominal current for the respective CT input
$V_{primCT,nom,n}$: nominal voltage for the respective CT input. Where on-load tap changing is used, the nominal voltage chosen should be that for the mid tap position.
$S_{prim,ref}$: common primary reference value of S for all windings

Therefore, the only data needed for ratio correction or amplitude matching calculations done by the relay are the nominal values read from the transformer nameplate.

For the two winding transformer shown in Figure 8, the phase C amplitude matched currents of the HV and LV windings are the same.

$$I_{amp,HV,C} = K_{amp,HV} \times I_{HV,C}$$
$$I_{amp,LV,C} = K_{amp,LV} \times I_{LV,C}$$

Where:
$I_{amp,\ HV,C}$; HV side phase C amplitude matched current
$K_{amp,HV}$: HV side calculated ratio correction factor
$I_{HV,C}$: HV side phase C current magnitude
$I_{amp,\ LV,C}$; LV side phase C amplitude matched current
$K_{amp,LV}$: LV side calculated ratio correction factor
$I_{LV,C}$: LV side phase C current magnitude

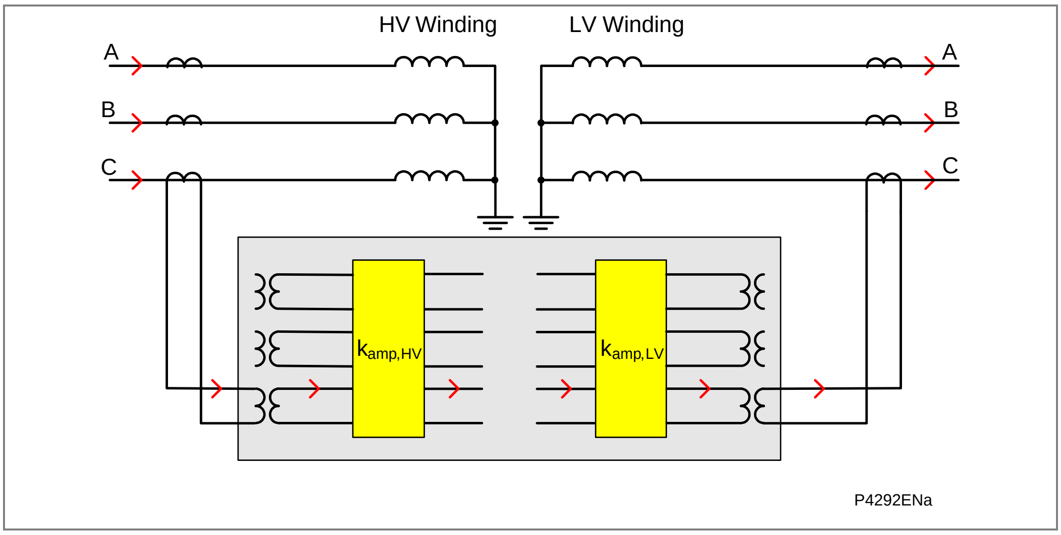


Figure 8 - Ratio correction or amplitude matching factor

Matching factors are displayed by the P64x in the **Match Factor CT1**, **Match Factor CT2**, **Match Factor CT3**, **Match Factor CT4** and **Match Factor CT5** data cells under the **SYSTEM CONFIG** menu heading. The P64x derives amplitude matching factors automatically so that all biased currents are compared on a like for like basis. The range of the calculated matching factors is from 0.05 to 20.

Caution	**Amplitude matching factors above 20 are not recommended as the probability of tripping due to electrical noise is very high.**

2.1.3 Vector Group Correction

To compensate for any phase shift between two windings of a transformer it is necessary to provide vector group correction. This was traditionally provided by the appropriate connection of physical interposing current transformers, as a replica of the main transformer winding arrangements, or by a delta connection of main CTs.

This matching operation can be carried out regardless of the phase winding connections, since the phase relationship is described unambiguously by the characteristic vector group number.

Vector group matching is therefore performed by mathematical phasor operations on the amplitude-matched phase currents of the *low-voltage side* in accordance with the characteristic vector group number. The vector group is the clock-face hour position of the LV A-phase voltage, with respect to the A-phase HV voltage at 12-o'clock (zero) reference. Phase correction is provided in the P64x using **SYSTEM CONFIG** then **LV Vector Group** for phase shift between HV and LV windings and **SYSTEM CONFIG** then **TV Vector Group** for phase shift between HV and TV windings. This is shown in Figure 9 for vector group characteristic number 5, where vector group Yd5 is used as the example:

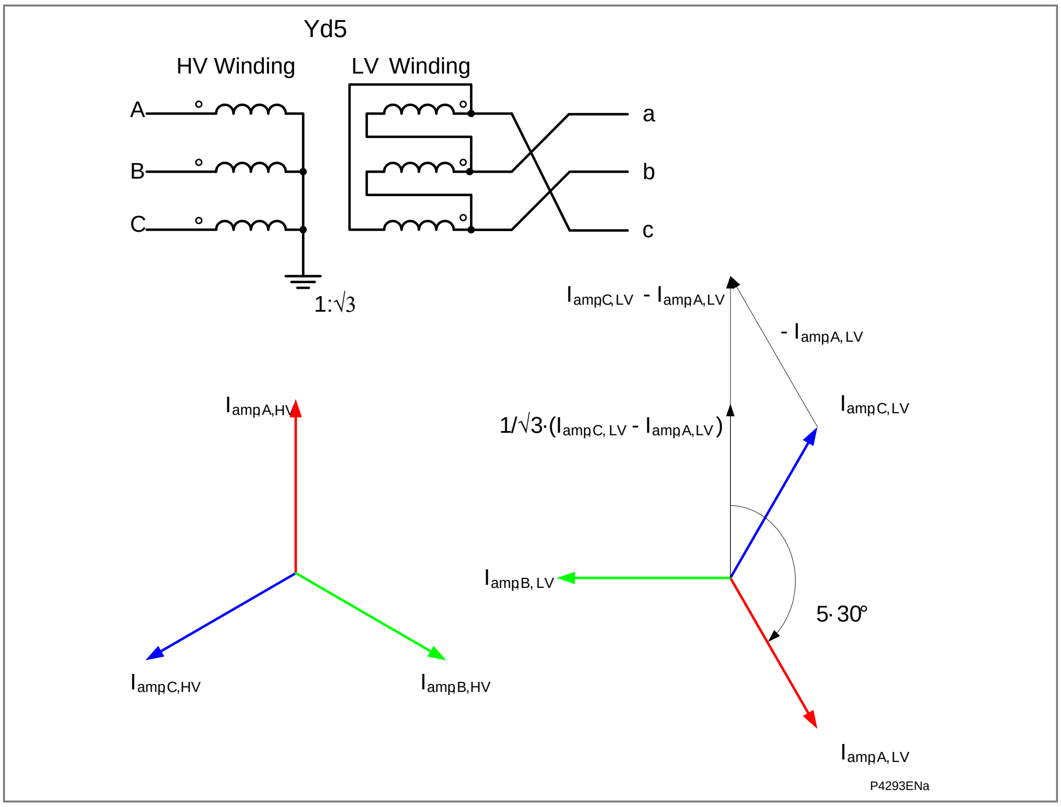


Figure 9 - Yd5 transformer example

The angle of positive sequence primary current is used as a default; therefore no vector correction is applied to the high voltage side.

As shown in Figure 9, the positive sequence current at the low voltage end is shifted by 150° clockwise for ABC (anti-clockwise) rotation. Therefore, the relay setting, **LV Vector Group**, equal to "5" rotates back the current at the low side for 150° in an anti-clockwise direction. This assures that the primary and secondary currents are in phase for load and external fault conditions. The vector correction also considers amplitude matching. If the vector group is any odd number, the calculated current will be greater by $\sqrt{3}$; therefore this current will be automatically divided by $\sqrt{3}$. Hence, this effect does not need to be taken into account when CT correction compensation is automatically calculated or set.

Setting the vector group matching function is very simple and does not require any calculations. Only the characteristic vector group number needs to be set in **LV Vector Group** and **TV Vector Group**.

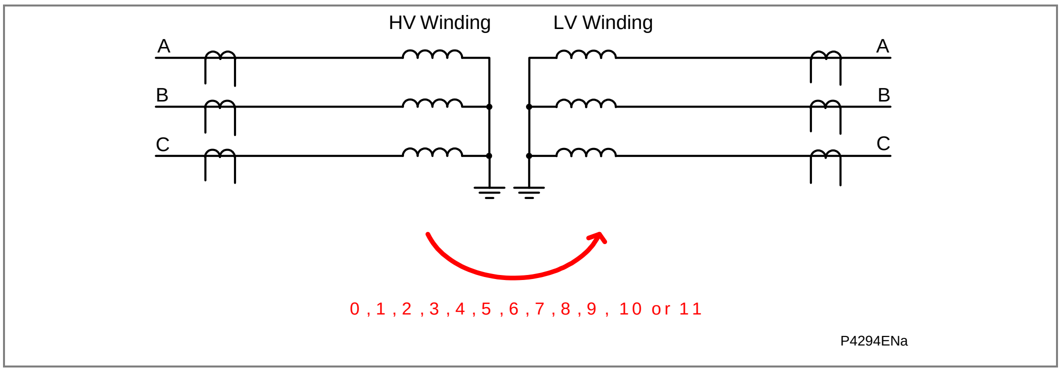


Figure 10 - Vector group selection

Other nameplate designations may be used instead of the clock notation. Common examples are:

Alternatives		Equivalent standard	LV group setting
D_{AB}/Y	D_{AB} – Y	Dy1	1
D_{AC}/Y	D_{AC} – Y	Dy11	11
Y/Y	Y_0 - Y0	Yy0	0
Y/Y ‾	Y_0 - Y6	Yy6	6

Table 3 - Examples of nameplate designations

2.1.4 Zero Sequence Filter

In addition to mimicking the phase shift of the protected transformer, it is also necessary to mimic the distribution of primary zero sequence current in the protection scheme. The necessary filtering of zero sequence current has also been traditionally provided by appropriate connection of interposing CTs or by delta connection of main CT secondary windings. In the P64x, the user does not need to decide which windings need zero sequence filtering. The user just needs to set which windings are grounded using a Yn, Zn or in zone-earthing transformer. The relay will adjust itself accordingly. In the advanced setting mode, it is possible to override the self adaptive setting with the zero sequence filtering enabled/disabled setting.

Where a transformer winding can pass zero sequence current to an external earth fault, it is essential that some form of zero sequence current filtering is used. This ensures that out of zone earth faults will not cause the relay to maloperate.

An external earth fault on the star side of a Dyn11 transformer will result in zero sequence current flowing in the current transformers associated with the star winding. However, due to the effect of the delta winding, there will be no corresponding zero sequence current in the current transformers associated with the delta winding.

To ensure stability of the protection, the LV zero sequence current must be eliminated from the differential current. Traditionally this has been achieved by either delta connected line CTs or by the inclusion of a delta winding in the connection of an interposing current transformer.

In accordance with its definition, the zero-sequence current is determined as follows from vector and amplitude matched phase currents:

$$\vec{I}_0 = \frac{1}{3} \cdot \left(\vec{I}_{A,vector\_comp} + \vec{I}_{B,vector\_comp} + \vec{I}_{C,vector\_comp} \right)$$

The current that is used in the differential equation is the filtered current per phase:

$$\vec{I}_{A,filtered} = \vec{I}_{A,vector\_comp} - \vec{I}_0$$

$$\vec{I}_{B,filtered} = \vec{I}_{B,vector\_comp} - \vec{I}_0$$

$$\vec{I}_{C,filtered} = \vec{I}_{C,vector\_comp} - \vec{I}_0$$

Setting the zero-sequence current filtering function is very simple and does not require any calculations. Zero-sequence current filtering should only be activated for those ends where there is operational earthing (grounding) of a neutral point:

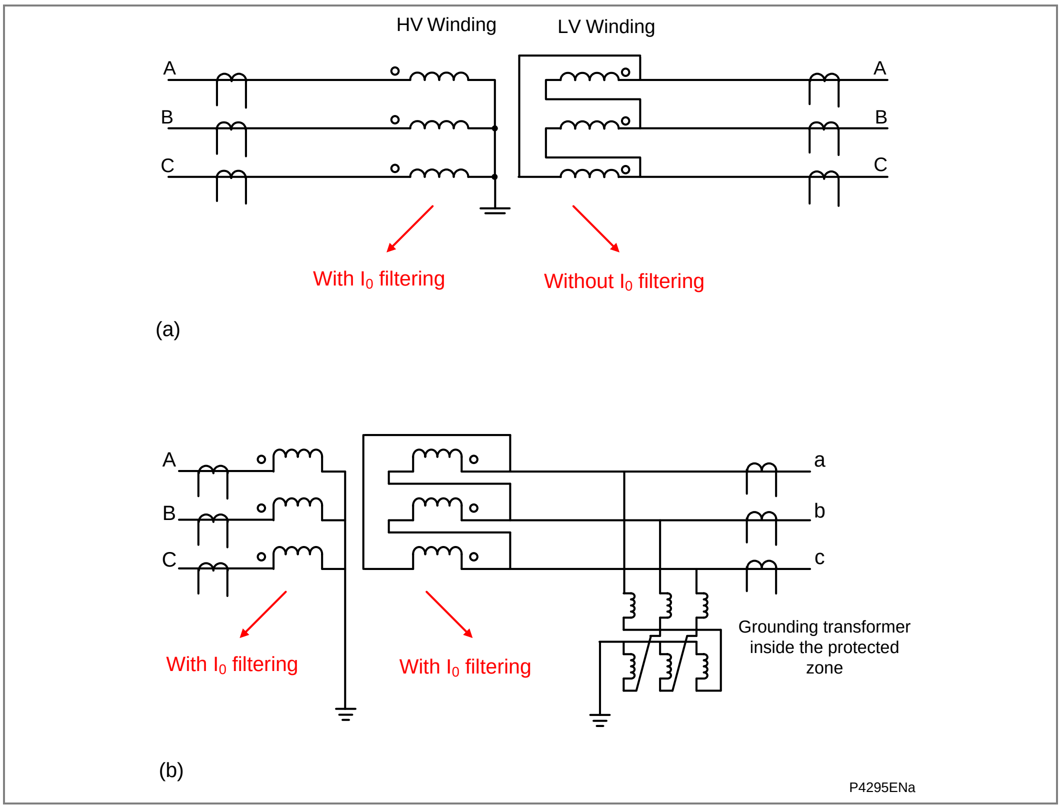

HV Winding
LV Winding
A
B
C
A
B
C
With I$_0$ filtering
Without I$_0$ filtering
(a)
A
B
C
a
b
c
With I$_0$ filtering
With I$_0$ filtering
Grounding transformer inside the protected zone
(b)
P4295ENa

Figure 11 - Zero sequence current filtering

Figure 12 shows the current distribution for an AN fault on the delta side of a Yd1 transformer with a grounding transformer inside the protected zone.

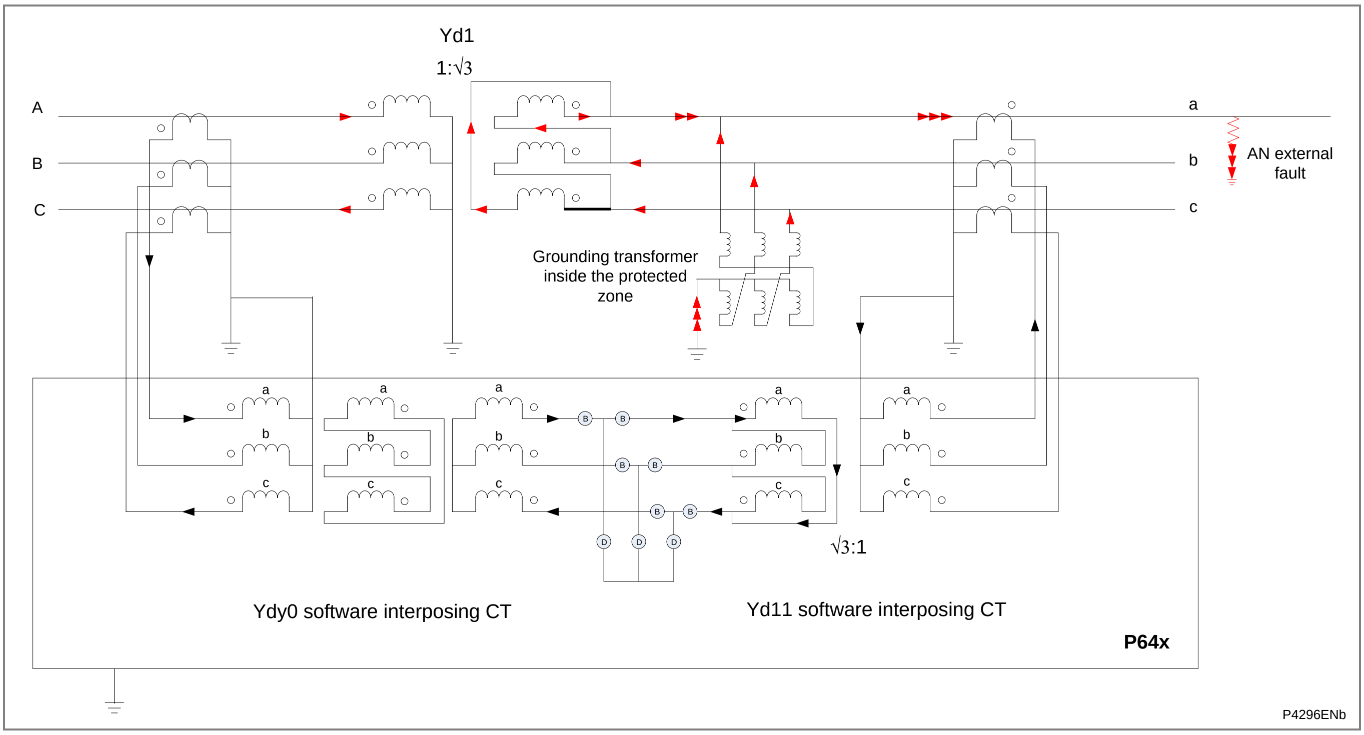

Yd1
1:√3
A
B
C
a
b
c
AN external fault
Grounding transformer inside the protected zone
a
b
c
√3:1
Ydy0 software interposing CT
Yd11 software interposing CT
P64x
P4296ENb

Figure 12 - Current distribution for AN external fault on delta side of Yd1 transformer

2.1.5 Magnetizing Inrush Stabilization

When a transformer is first energized, a transient magnetizing current flows, which may reach instantaneous peaks of 8 to 30 times the full load current. The factors controlling the duration and magnitude of the magnetizing inrush are:

- Size of the transformer bank
- Size of the power system
- Resistance in the power system from the source to the transformer bank
- Residual flux level
- Type of iron used for the core and its saturation level.

These conditions can produce a magnetizing inrush effect:

- First energization
- Voltage recovery following external fault clearance
- Sympathetic inrush due to a parallel transformer being energized.

As shown in Figure 13, under normal steady state conditions the flux in the core changes from maximum negative value to maximum positive value during one half of the voltage cycle, which is a change of 2.0 maximum.

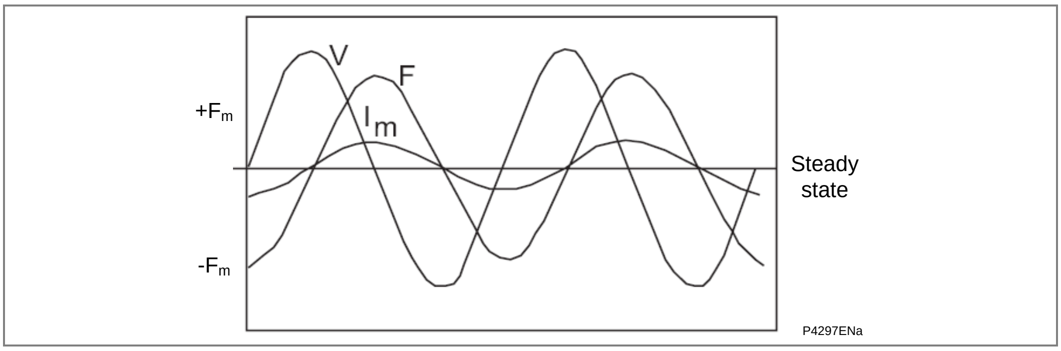
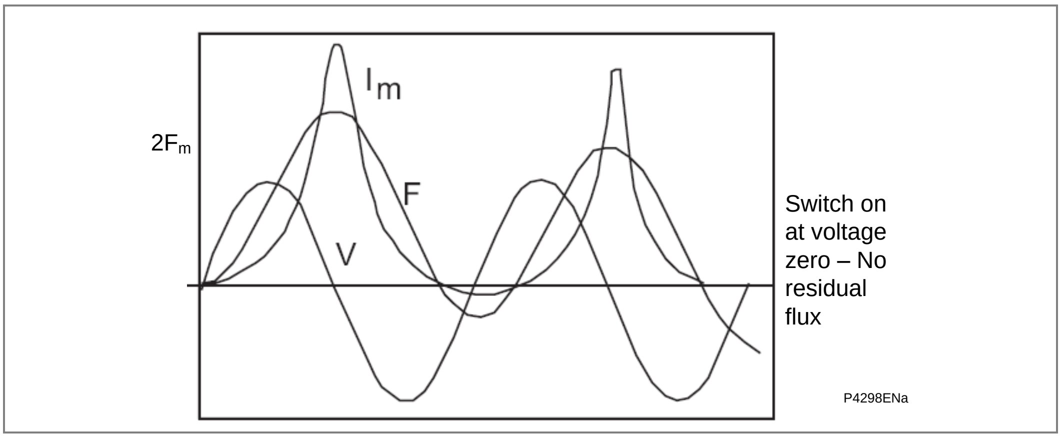


Figure 13 - Steady state magnetizing inrush current

If the transformer is energized at a voltage zero when the flux would normally be at its maximum negative value, the flux would rise to twice its normal value over the first half cycle of voltage. To establish this flux, a high magnetizing inrush current is required. The first peak of this current can be as high as 30 times the transformer rated current. This initial rise could be further increased if there was any residual flux in the core at the moment the transformer was energized.



Switch on at voltage zero – No residual flux

Figure 14 - Magnetizing inrush current during energization

As the flux enters the highly saturated portion of the magnetizing characteristic, the inductance falls and the current rises rapidly. Magnetizing impedance is of the order of 2000% but under heavily saturated conditions this can reduce to around 40%, which is an increase in magnetizing current of 50 times normal. This figure can represent 5 or 6 times normal full load current.

Analysis of a typical magnitude inrush current wave shows (fundamental = 100%):

Component	-DC	2nd H	3rd H	4th H	5th H	6th H	7th H
	55%	63%	26.8%	5.1%	4.1%	3.7%	2.4%

The offset in the wave is only restored to normal by the circuit losses. The time constant of the transient can be quite long, typically 0.1 second for a 100 KVA transformer and up to 1 second for larger units. The initial rate of decay is high due to the low value of air core reactance. When below saturation level, the rate of decay is much slower. Figure 15 shows the rate of decay of the DC offset in a 50 Hz or 60 Hz system in terms of amplitude reduction factor between successive peaks.

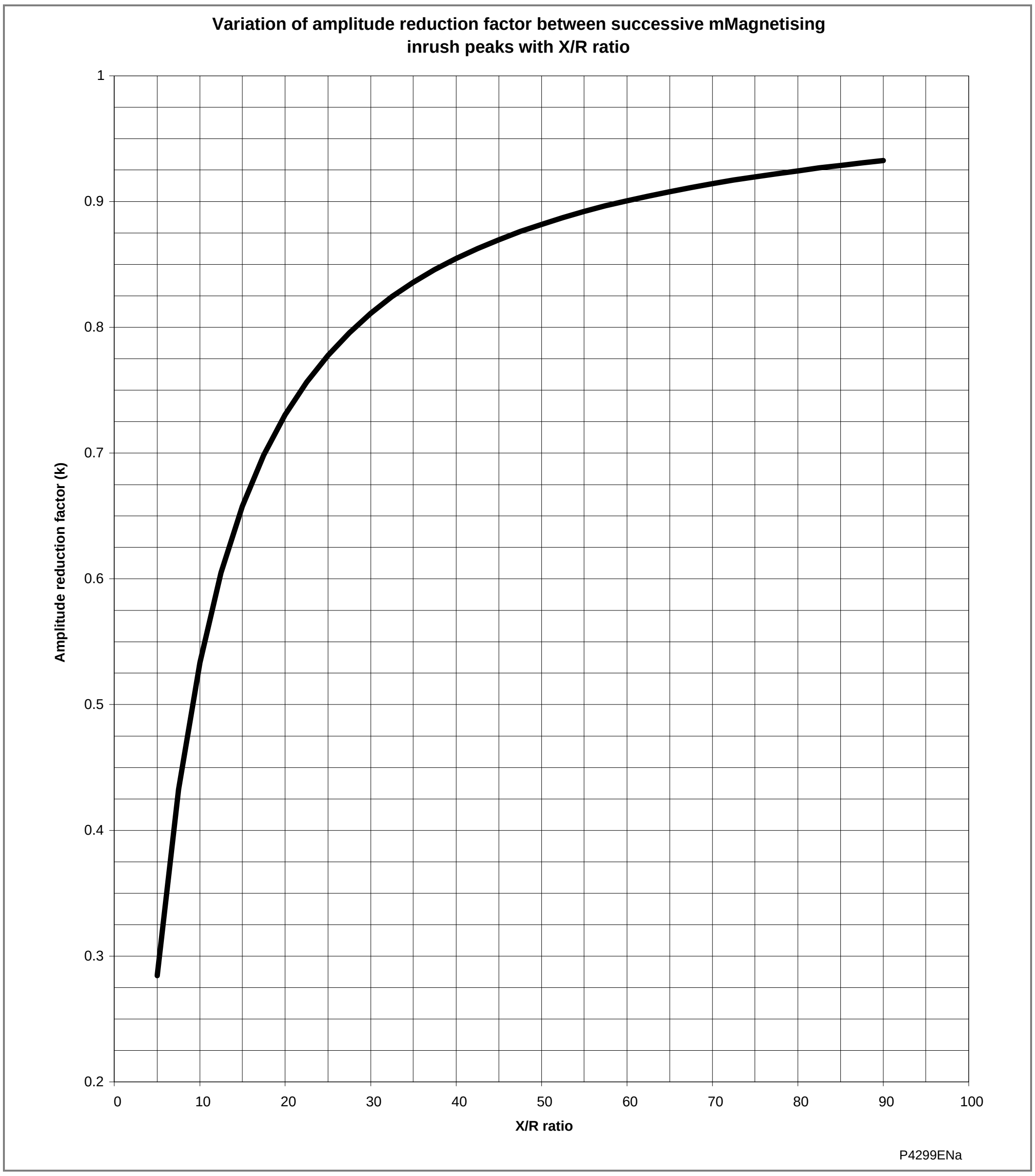


Figure 15 - Variation of amplitude reduction factor

The magnitude of the inrush current is limited by the air core inductance of the windings under extreme saturation conditions. A transformer with concentric windings will draw a higher magnetizing current when energized from the LV side, since this winding is usually on the inside and has a lower air core inductance. Sandwich windings have approximately equal magnitude currents for both LV and HV. Resistance in the source will reduce the magnitude current and increase the rate of decay.

The magnetizing inrush phenomenon is associated with a transformer winding which is being energized where no balancing current is present in the other winding(s). This current appears as a large operating signal for the differential protection. Therefore, special measures are taken with the relay design to ensure that no maloperation occurs during inrush. The fact that the inrush current has a high proportion of harmonics having twice the system frequency offers a possibility of stabilization against tripping by the inrush current. The second harmonic blocking may not be effective in all applications with all types of transformers. The P64x filters the differential current. The fundamental $I_{diff}(f_0)$ and second harmonic components $I_{diff}(2*f_0)$ of the differential current are determined. If the ratio $I_{diff}(2*f_0)/I_{diff}(f_0)$ exceeds a specific adjustable value (typical setting 20%) in at least one phase, the low-set differential element is blocked optionally in one of these modes:

- Across all three phases if cross blocking is selected
- Selectively for one phase because the harmonic blocking is phase segregated
- There is no blocking if the differential current exceeds the high set thresholds Is-HS1 or Is-HS2.

2.1.6 CT Saturation and no Gap Detection

No settings are required by the CT saturation and no gap detection features. It is only possible to either enable or disable them on the **CTSat and NoGap** setting cell. It is recommended to enable **CTSat and NoGap** because faster operating times are achievable under CT saturation with fault levels below Is-HS1 threshold. The assertion of CTSat and NOGap prevents the second harmonic element from blocking the low set differential element. Therefore, at fault levels below Is-HS1 threshold fast fault clearance is achievable even with CT saturation.

Figure 16 and Figure 17 are the same AN internal fault. Figure 16 shows the disturbance record from a P64x with CT saturation and No gap detection enabled. The second harmonic blocking is asserted due to CT saturation. Therefore, the operation of the low set differential element (bias element trip) is prevented. Once the No gap detection is asserted the low set differential element is allowed to operate. The operating time is 32 ms.

Figure 17 shows the disturbance record from a P64x with CT saturation and no gap detection disabled. The second harmonic blocking is asserted due to CT saturation. Therefore, the operation of the low set differential element (bias element trip) is prevented until the second harmonic blocking de-asserts. In this case, the operating time is 56 ms.

Enabling the CT saturation and no gap detection logics enhance the relay operating time. In this example, the relay is 24 ms faster if the CT saturation and no gap detection logics are enabled.

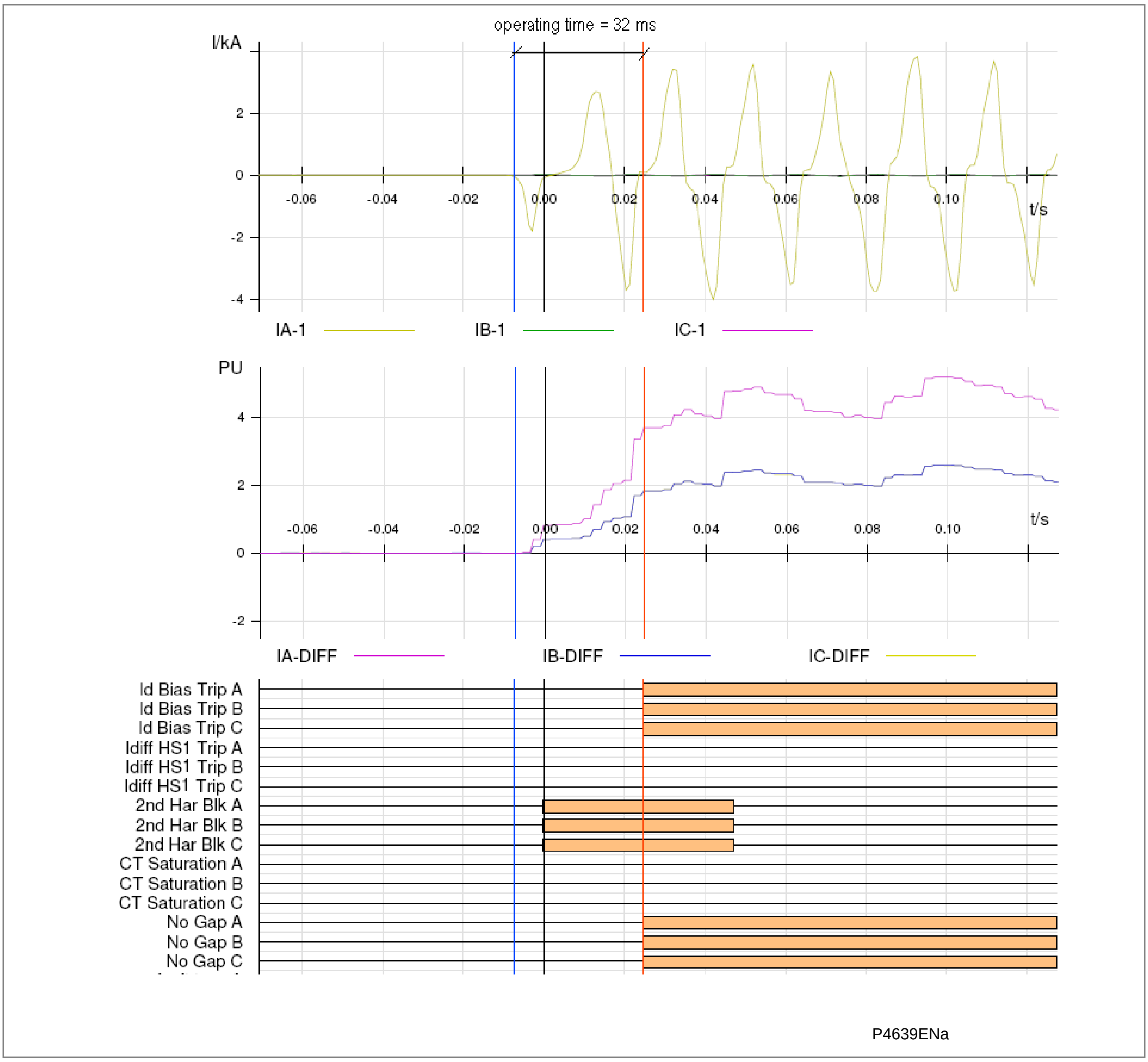


Figure 16 - CT saturation and no gap detection enabled

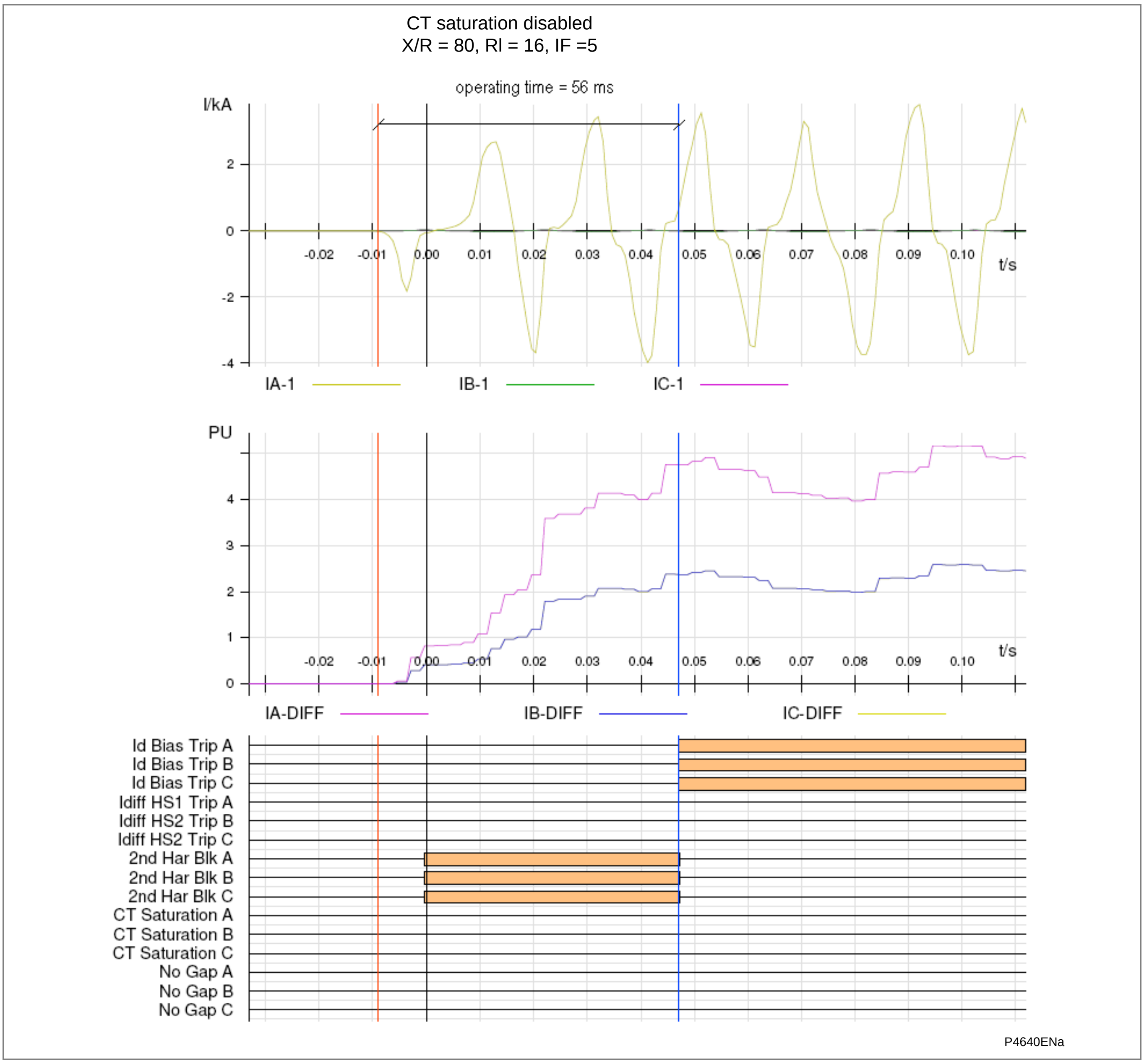


Figure 17 - CT saturation and no gap detection disabled

Figure 18 and Figure 19 are the same AN internal fault.

Figure 18 is the disturbance record from a P64x with CT saturation and No gap detection enabled, the operating time of the low set differential element is 28 ms. It can be observed that both the CT saturation logic and the no gap detection logic are asserted. The CT saturation and No gap detection logics complement each other.

Figure 19 is the disturbance record from a P64x with CT saturation and No gap detection disabled. The operating time is 57 ms. The P64x is 29 ms faster if the CT saturation and No gap detection is enabled.

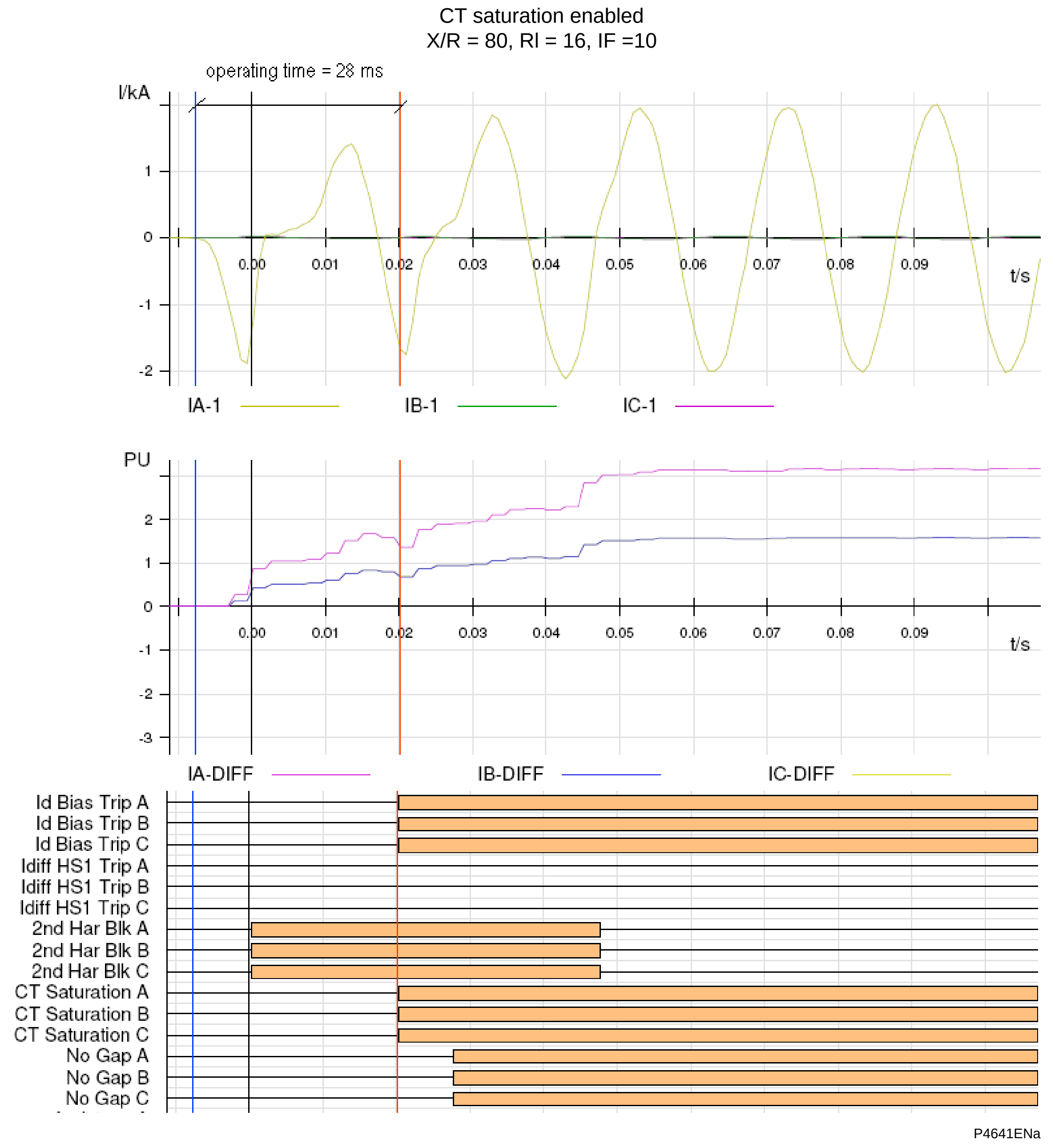


Figure 18 - CT saturation and no gap detection enabled

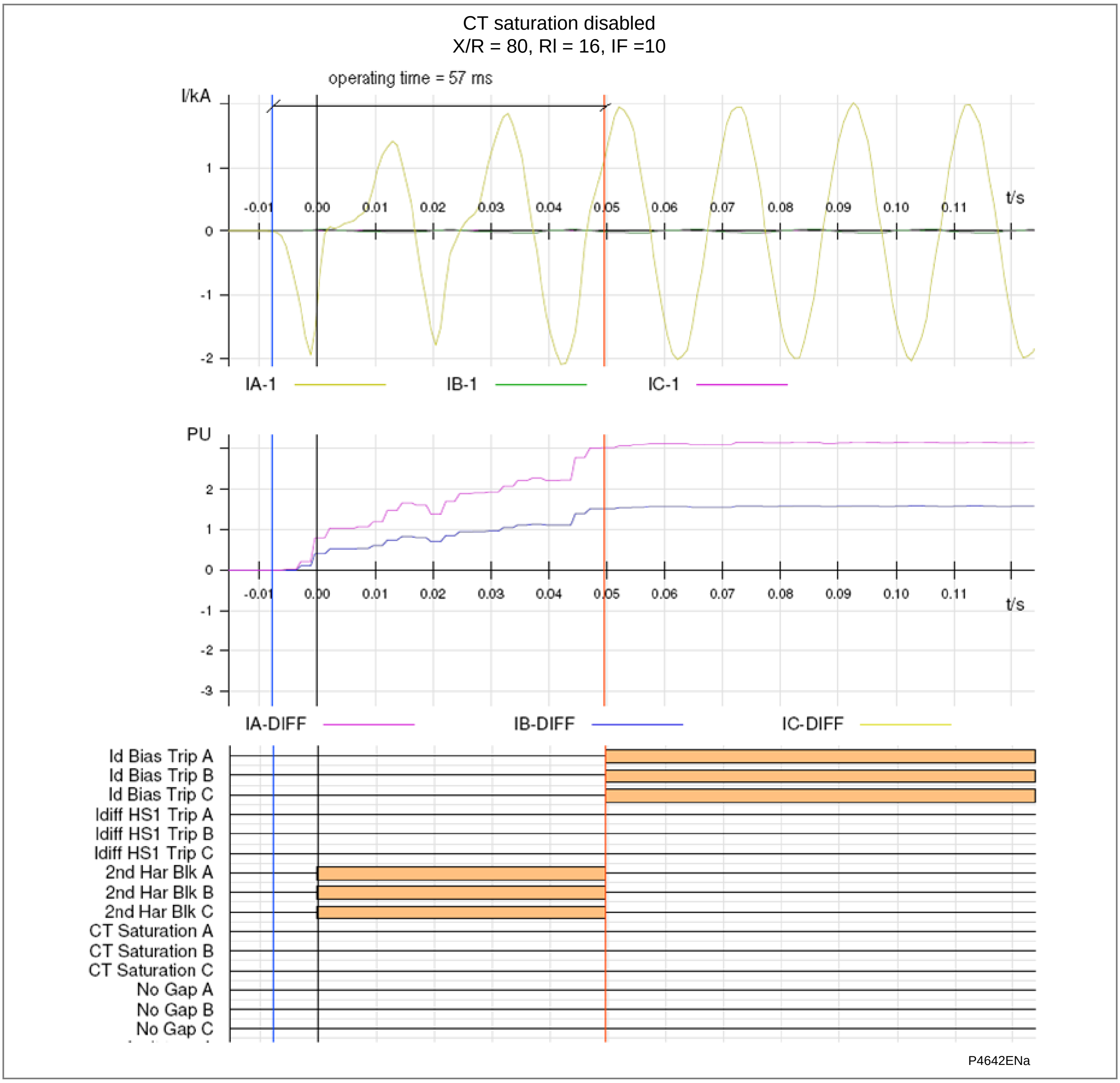


Figure 19 - CT saturation and no gap detection disabled

2.1.7 High Set Operation

The P64x relay incorporates independent differential high set elements, Is-HS1 and Is-HS2 to complement the protection provided by the biased differential low set element. The instantaneous high set offers faster clearance for heavy internal faults and it is not blocked for magnetizing inrush or transient overfluxing conditions.

Stability is provided for heavy external faults, but the operating threshold of the high set differential element must be set to avoid operation with inrush current.

When a transformer is energized, a high magnetizing inrush current is drawn. The magnitude and duration of this inrush current is dependant on several factors including:

- Size and impedance of the transformer
- Point on wave of switching
- Remnant flux in the transformer
- Number of transformers connected in parallel

It is difficult to accurately predict the maximum anticipated level of inrush current. Typical waveform peak values are of the order of 8x to 30x rated current. A worst-case estimation of inrush could be made by dividing the transformer full load current by the per-unit leakage reactance quoted by the transformer manufacturer. In the simple mode, the relay calculates the setting for Is-HS1 as the reciprocal of the transformer reactance.

A setting range of 2.5 to 32 pu is provided on the P64x relay for Is-HS1 and Is-HS2. Both elements should be set in excess of the anticipated or estimated peak value of inrush current after ratio correction.

The Is-HS2 element uses the fundamental component of the differential current. This element is not restrained by the bias characteristic, so the P64x will trip regardless of the restraining current. Is-HS2 should be set so that the relay will not maloperate during external faults. When through fault current is limited by the transformer impedance, Is-HS2 can be set as $1.3 \times (1/X_t)$. In breaker and a half, ring bus or mesh applications, the through fault current is not limited by the transformer impedance but by the system source impedance. This current can be higher than $1.3 \times (1/X_t)$, therefore the user should consider the actual through fault current when setting Is-HS2. To avoid high values of spurious differential current due to CT saturation during through fault conditions, it is important to equalize the burden on the CT secondary circuits.

2.1.8 Setting Guidelines for Transformer Biased Differential Protection

The differential setting, **Configuration/Diff Protection**, should be set to **Enable**.

The basic pick up level of the low set differential element, Is1, is variable between 0.1 pu and 2.5 pu in 0.01 pu steps. The setting chosen is dependant on the item of plant being protected and by the amount of differential current that might be seen during normal operating conditions. When the P64x is used to protect a transformer, a setting of 0.2 In is generally recommended.

When protecting generators and other items of plant, where shunt magnetizing current is not present, a lower differential setting can be used and 0.1 pu would be more typical.

The biased low-set differential protection is blocked under magnetizing inrush conditions and during transient over fluxing conditions if the appropriate settings are enabled. The second harmonic measurement and blocking are phase segregated. If cross blocking is set to enabled, phases A, B and C of the low set differential element are blocked when an inrush condition is detected. The fifth harmonic measurement and blocking are also phase segregated, but no cross blocking is available.

As shown in Figure 20, the first slope is flat and depends on the Is1 setting. It ensures sensitivity to internal faults. The second slope, K1, is user settable. K1 ensures sensitivity to internal faults up to full load current. It allows for the 15% mismatch which can occur at the limit of the transformer’s tap-changer range and an additional 5% for any CT ratio errors. The K1 slope should be set above the errors due to CT mismatch, load tap changers and steady state magnetizing current. The errors slope, which is the combined tap changer (T/C) and current transformer (CT) error, should always be below the K1 slope to avoid mal operations. It is recommended to set K1 to 30%, as long as the errors slope is below the K1 slope by a suitable margin. The second slope, K2, is also user settable, and it is used for bias currents above the rated current. To ensure stability under heavy through fault conditions, which could lead to increased differential current due to asymmetric saturation of CTs, K2 is **recommended to be** set to 80%.

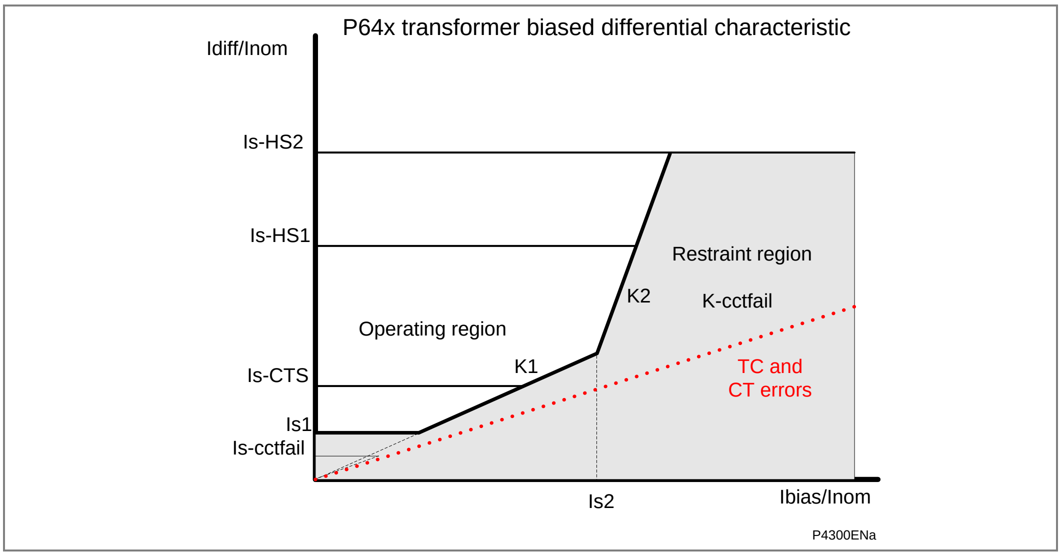


Figure 20 - Tap changer and CT combined errors

2.1.8.1 Example 1: Two Winding Transformer (P642) - no Tap Changer

Figure 21 shows the application of P642 to protect a two winding transformer. The power transformer data has been given: 90 MVA Transformer, Ynd9, 132/33 kV. The current transformer ratios are as follows: HV CT ratio - 400/1, LV CT ratio - 2000/1.

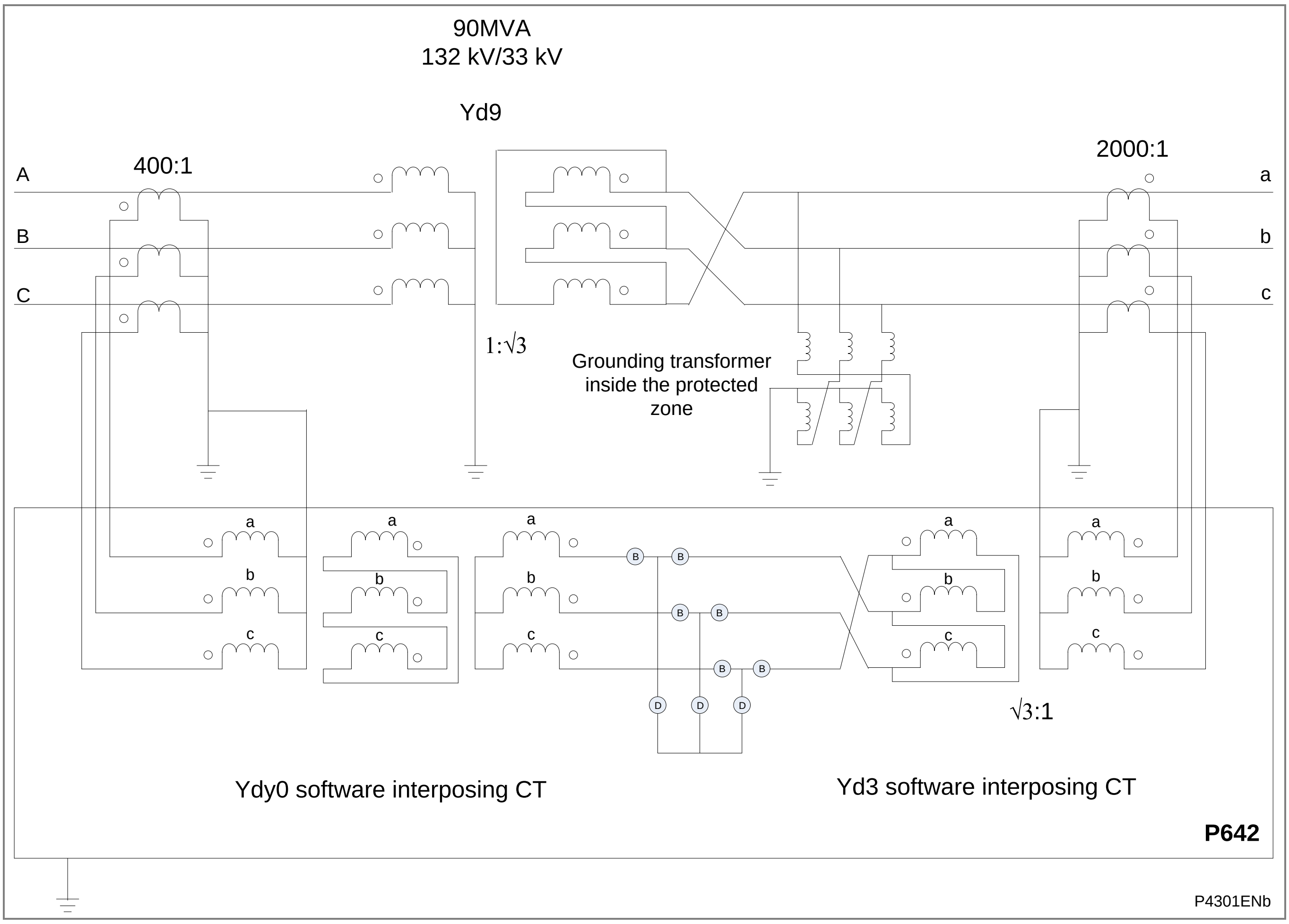
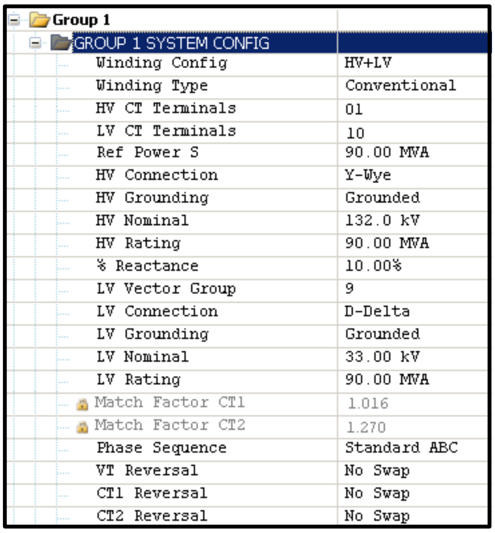

90MVA
132 kV/33 kV
Yd9
400:1
2000:1
A
B
C
a
b
c
1:√3
Grounding transformer inside the protected zone
a
b
c
B
D
√3:1
Ydy0 software interposing CT
Yd3 software interposing CT
P642
P4301ENb

Figure 21 - P642 used to protect a two winding transformer

The relay always calculates and sets the amplitude matching factors. As explained previously no vector correction is applied to the high voltage side. Vector correction is done by setting **SYSTEM CONFIG** then **LV Vector Group** to **9**. The zero sequence filtering is done by setting **SYSTEM CONFIG** then **HV Grounding** to **Grounded** and **SYSTEM CONFIG** then **LV Grounding** to **Grounded**. The following screenshot shows the SYSTEM CONFIG settings for the P642.



Group 1	
GROUP 1 SYSTEM CONFIG	
Winding Config	HV+LV
Winding Type	Conventional
HV CT Terminals	01
LV CT Terminals	10
Ref Power S	90.00 MVA
HV Connection	Y-Wye
HV Grounding	Grounded
HV Nominal	132.0 kV
HV Rating	90.00 MVA
% Reactance	10.00%
LV Vector Group	9
LV Connection	D-Delta
LV Grounding	Grounded
LV Nominal	33.00 kV
LV Rating	90.00 MVA
Match Factor CT1	1.016
Match Factor CT2	1.270
Phase Sequence	Standard ABC
VT Reversal	No Swap
CT1 Reversal	No Swap
CT2 Reversal	No Swap

Figure 22 - P642 System Config settings

The ratio correction factors are calculated by the relay as follows:

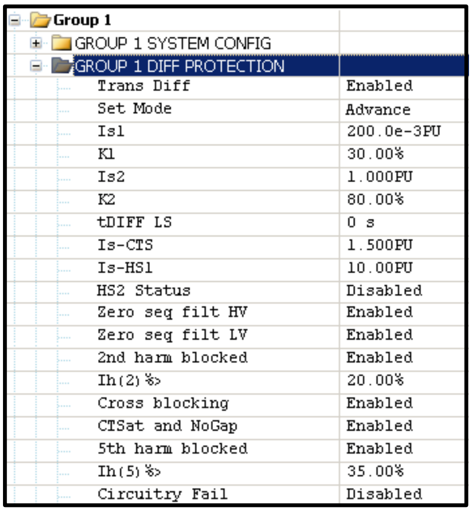
$$K_{amp,T1CT} = \frac{I_{nom,T1CT}}{\dfrac{S_{ref}}{\sqrt{3}V_{nom,HV}}} = \frac{400}{\dfrac{90\times10^6}{\sqrt{3}\times132\times10^3}} = 1.016$$

$$K_{amp,T2CT} = \frac{I_{nom,T2CT}}{\dfrac{S_{ref}}{\sqrt{3}V_{nom,LV}}} = \frac{2000}{\dfrac{90\times10^6}{\sqrt{3}\times33\times10^3}} = 1.270$$

Where:

S_{ref}:	common reference power for all ends
$K_{am,\ T1CT,\ T2CT}$:	ratio correction factor of T1 CT or T2 CT windings
$I_{nom,\ T1CT,\ T2CT}$:	primary nominal currents of the main current transformers
$V_{nom,\ HV,LV}$:	primary nominal voltage of HV or LV windings

The recommended settings for the differential function (Is1, Is2, K1, K2, second and fifth harmonic blocking) were discussed in previous sections. See Figure 23.



Group 1	
GROUP 1 SYSTEM CONFIG	
GROUP 1 DIFF PROTECTION	
Trans Diff	Enabled
Set Mode	Advance
Is1	200.0e-3PU
K1	30.00%
Is2	1.000PU
K2	80.00%
tDIFF LS	0 s
Is-CTS	1.500PU
Is-HS1	10.00PU
HS2 Status	Disabled
Zero seq filt HV	Enabled
Zero seq filt LV	Enabled
2nd harm blocked	Enabled
Ih(2)%>	20.00%
Cross blocking	Enabled
CTSat and NoGap	Enabled
5th harm blocked	Enabled
Ih(5)%>	35.00%
Circuitry Fail	Disabled

Figure 23 - P642 Diff Protection settings

2.1.8.2 Example 2: Autotransformer (P645) - Load Tap Changer

Figure 24 shows the application of a P645 to protect an autotransformer. The power transformer data has been given: 175/175/30 MVA Autotransformer, YNyn0d1, 230/115/13.8 kV. The current transformer ratios are as follows: HV CT ratio - 800/5, LV CT ratio - 1200/5 and TV CT ratio 2000/5.

Since the transformer has an on load tap changer on the HV side, the nominal voltage of the HV winding must be set to the mid tap voltage level. According to the nameplate data, the mid tap voltage is 218.5 kV. The mid tap voltage can also be calculated as follows:

$$\text{Mid tap position} = \frac{100 + \frac{(5-15)}{2}}{100} \times 230 = 218.5kV$$

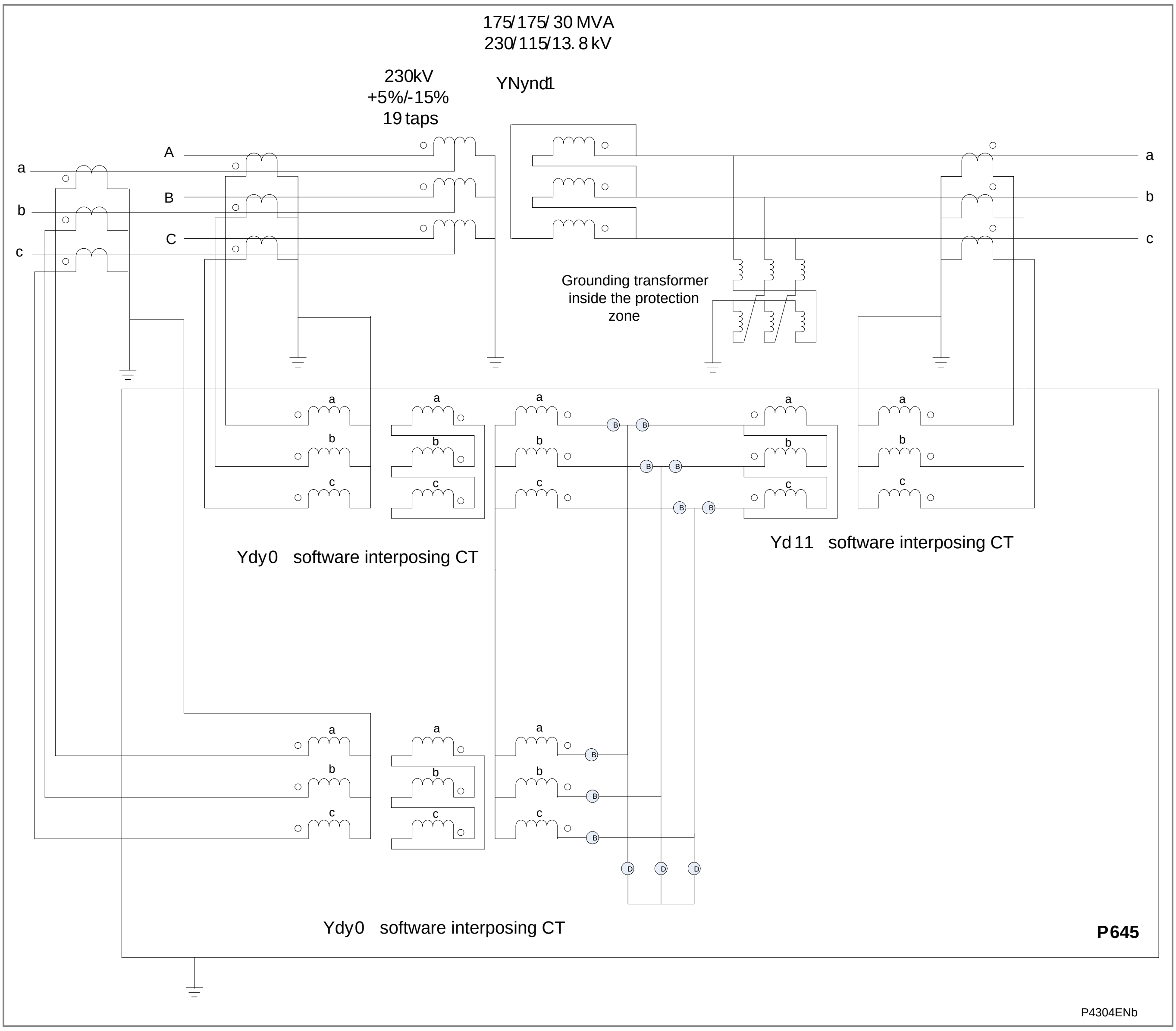

175/175/30 MVA
230/115/13.8 kV
230kV
+5%/-15%
19 taps
YNynd1
A
B
C
a
b
c
a
b
c
Grounding transformer inside the protection zone
a
b
c
B
D
Ydy0 software interposing CT
Yd11 software interposing CT
Ydy0 software interposing CT
P645
P4304ENb

Figure 24 - P645 used to protect an autotransformer with load tap changer

Ratio correction:

The relay calculates the ratio correction factors as follows:

$$K_{amp,T1CT} = \frac{I_{nom,T1CT}}{\frac{S_{ref}}{\sqrt{3}V_{nom,HV}}} = \frac{800}{\frac{175 \times 10^6}{\sqrt{3} \times 218.5 \times 10^3}} = 1.730$$

$$K_{amp,T5CT} = \frac{I_{nom,T5CT}}{\frac{S_{ref}}{\sqrt{3}V_{nom,LV}}} = \frac{1200}{\frac{175 \times 10^6}{\sqrt{3} \times 115 \times 10^3}} = 1.366$$

$$K_{amp,T3CT} = \frac{I_{nom,T3CT}}{\frac{S_{ref}}{\sqrt{3}V_{nom,TV}}} = \frac{2000}{\frac{175 \times 10^6}{\sqrt{3} \times 13.8 \times 10^3}} = 0.273$$

To check that the differential protection does not misoperate due to errors introduced by the on load tap changer, the user may perform the following calculations.

Transformer nominal rating

Calculate HV full load current at both tap extremities and LV and TV full load current.

$$\text{HV full load current on tap}\,1\,(5\%) = \frac{175 \times 10^6}{\sqrt{3} \times 241500} = 418.37A \ \ \text{primary}$$

$$\text{HV full load current on tap}\,1\,(5\%) = \frac{418.37}{160} = 2.615A \ \ \text{secondary}$$

$$\text{HV corrected current on tap}\,1 = 1.730 \times 2.615 = 4.524A \ \ \text{secondary}$$

$$\text{HV full load current on tap 19 (-15\%)} = \frac{175 \times 10^6}{\sqrt{3} \times 195.510^3} = 516.810A \ \ \text{primary}$$

$$\text{HV full load current on tap 19 (-15\%)} = \frac{516.810}{160} = 3.230A \ \ \text{secondary}$$

$$\text{HV corrected current on tap 19} = 1.730 \times 3.230 = 5.588A \ \ \text{secondary}$$

$$\text{LV full load current} = \frac{145 \times 10^6}{\sqrt{3} \times 115 \times 10^3} = 727.963A \ \ \text{primary}$$

$$\text{LV full load current} = \frac{727.963}{240} = 3.033A \ \ \text{secondary}$$

$$\text{TV full load current} = \frac{30 \times 10^6}{\sqrt{3} \times 13.8 \times 10^3} = 1255.109A \ \ \text{primary}$$

$$\text{TV full load current} = \frac{1255.109}{400} = 3.138A \ \ \text{secondary}$$

Determine Idiff at both tap extremities (with mid tap correction).

$$\text{LV corrected current} = 1.366 \times 3.033 = 4.143$$

$$\text{TV corrected current} = 0.273 \times 3.138 = 0.857$$

$$\text{Idiff at tap } 1 = \left|4.524 - 4.143 - 0.857\right| = 0.476A = \frac{0.476}{5} = 0.095pu$$

$$\text{Idiff at tap } 19 = \left|5.588 - 4.143 - 0.857\right| = 0.588A = \frac{0.588}{5} = 0.118pu$$

Determine Ibias at both tap extremities (with mid tap correction). The currents used in the Ibias calculation are the currents after ratio and vector correction.

$$\text{Ibias at tap } 1 = \frac{4.524 + 4.143 + 0.857}{2} = 4.762A = \frac{4.762}{5} = 0.9524pu$$

$$\text{Ibias at tap } 19 = \frac{5.588 + 4.143 + 0.857}{2} = 5.294A = \frac{5.294}{5} = 1.059pu$$

Determine relay differential current.

Iop = Is1, (Ibias ≤ Is1/K1)

Iop = K1× Ibias, (Is1/K1 ≤ Ibias ≤ Is2)

Iop = K1 × Is2 + K2 × (Ibias - Is2), (Ibias ≥ Is2)

Ibias at tap 1 is less than 5 A (1 pu) and greater than 3.33 A (0.667 pu); since Is_2 is set to the rated current (5 A), Iop is calculated as follows:

Iop = 0.3 × 4.762 = 1.429 A

Ibias at tap 19 is greater than 5 A; since Is_2 is set to the rated current (5 A), Iop is calculated as follows:

Is2 = 1 pu = 1 × 5 = 5 A

Iop = 0.3 × 5 + 0.8 × (5.294 - 5) = 1.735 A

Check Idiff < Iop by a 10% margin for each tap extremity and adjust Is1 and/or K1 as necessary.

Tap 1: Since Idiff = 0.476A and 0.9Iop at tap 1 = 0.9 x 1.429 = 1.286 A

Therefore there is sufficient safety margin with K1 = 30% and Is1 = 0.2 pu.

Tap 19: Since Idiff = 0.588A and 0.9Iop at tap 19 = 0.9 x 1.735 = 1.562 A

Therefore there is sufficient safety margin with K1 = 30% and Is1 = 0.2 pu.

66.7% of transformer nominal rating

Calculate HV, LV and TV load current at 66.7% of the nominal MVA rating. The 66.7% is the interception between Is1 and K1. It is determined as Is1/K1 × 100% = (0.2/0.3) × 100 = 66.7%.

$$\text{HV full load current on tap } 1(5\%) = 0.667 \times \frac{175 \times 10^6}{\sqrt{3} \times 241500} = 279.05A \quad \text{primary}$$

$$\text{HV full load current on tap } 1(5\%) = \frac{279.05}{160} = 1.744A \quad \text{secondary}$$

$$\text{HV corrected current on tap1} = 1.730 \times 1.744 = 3.017A \quad \text{sec}ondary$$

$$\text{HV full load current on tap 19 (-15\%)} = 0.667 \times \frac{175 \times 10^6}{\sqrt{3} \times 195.510^3} = 344.71A \quad \text{primary}$$

$$\text{HV full load current on tap 19 (-15\%)} = \frac{344.71}{160} = 2.154A \quad \text{secondary}$$

$$\text{HV corrected current on tap 19} = 1.730 \times 2.154 = 3.727A \quad \text{sec}ondary$$

$$\text{LV full load current} = 0.667 \times \frac{145 \times 10^6}{\sqrt{3} \times 115 \times 10^3} = 485.551A \quad \text{primary}$$

$$\text{LV full load current} = \frac{485.551}{240} = 2.023A \quad \text{secondary}$$

$$\text{TV full load current} = 0.667 \times \frac{30 \times 10^6}{\sqrt{3} \times 13.8 \times 10^3} = 837.158A \quad \text{primary}$$

$$\text{TV full load current} = \frac{837.158}{400} = 2.093A \quad \text{secondary}$$

Determine Idiff at both tap extremities (with mid tap correction).

$$\text{LV corrected current} = 1.366 \times 2.023 = 2.763A$$

$$\text{TV corrected current} = 0.273 \times 2.093 = 0.571A$$

$$\text{Idiff at tap 1} = |3.017 - 2.763 - 0.571| = 0.317A = \frac{0.317}{5} = 0.063pu$$

$$\text{Idiff at tap 19} = |3.727 - 2.763 - 0.571| = 0.393A = \frac{0.393}{5} = 0.0786pu$$

Determine Ibias at both tap extremities (with mid tap correction). The currents used in Ibias calculation are the currents after ratio and vector correction.

$$\text{Ibias at tap 1} = \frac{3.017 + 2.763 + 0.571}{2} = 3.176A = \frac{3.176}{5} = 0.635pu$$

$$\text{Ibias at tap 19} = \frac{3.727 + 2.763 + 0.571}{2} = 3.531A = \frac{3.531}{5} = 0.706pu$$

Determine relay differential current.

Iop = Is1, (Is1/K1 ≤ Ibias)

Iop = K1× Ibias, (Is1/K1 ≤ Ibias ≤ Is2)

Iop = K1 × Is2 + K2 × (Ibias - Is2), (Ibias ≥ Is2)

Ibias at tap 1 is less than 3.33 A (0.667 pu); then Iop = 0.2 pu = 1 A

Ibias at tap 1 is less than 5 A (1 pu) and greater than 3.33 A (0.667 pu); since Is_2 is set to the rated current (5 A), Iop is calculated as follows:

$Iop = 0.3 \times 3.531 = 1.059$ A

Check Idiff < Iop by a 10% margin for each tap extremity and adjust Is1 and/or K1 as necessary:

Tap 1: Since Idiff = 0.317 A and 0.9Iop at tap 1 = 0.9 x 1 = 0.9 A

Therefore there is sufficient safety margin with K1 = 30% and Is1 = 0.2 pu.

Tap 19: Since Idiff = 0.393 A and 0.9Iop at tap 19 = 0.9 x 1.059 = 0.953 A

Therefore there is sufficient safety margin with K1 = 30% Is1 = 0.2 pu.

Figure 25 shows the bias characteristic, the CT and tap changer errors (assumed as 20%), and the bias, differential coordinates corresponding to full load current and 66.7% of full load current. It can also be seen that it is necessary to check the safety margin at the two knee-points of the bias characteristic.

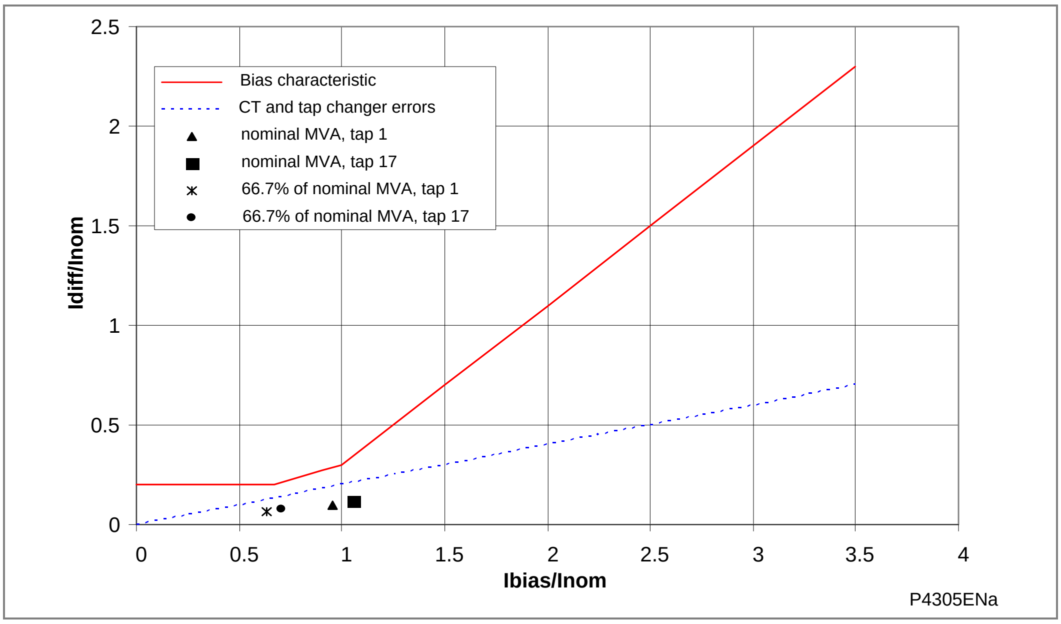
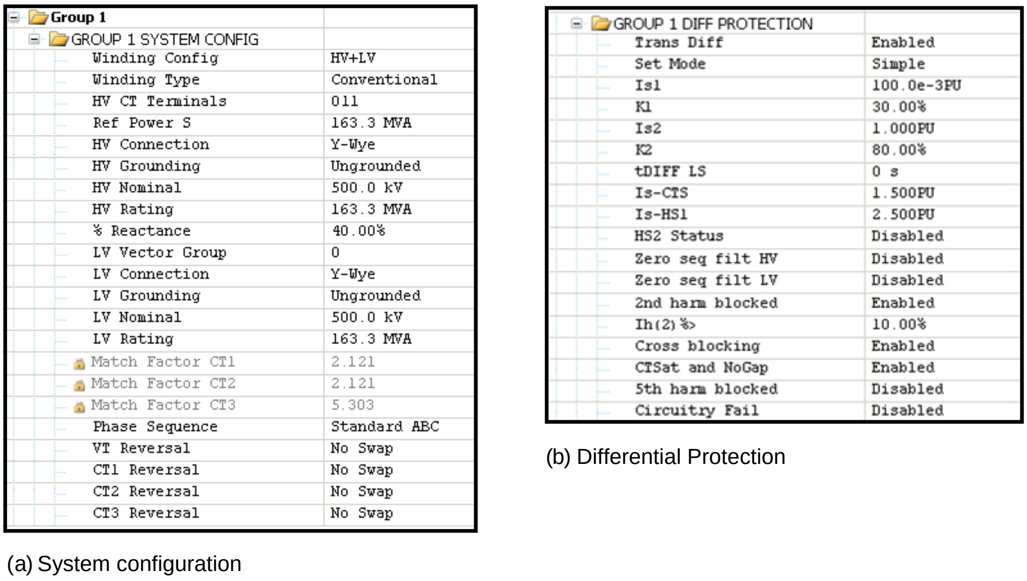


Figure 25 - Safety margin at the two knee-points of the bias characteristic

Vector correction and zero sequence filtering

Vector correction is done by setting **LV Vector Group** in **SYSTEM CONFIG** to **0** and **TV Vector Group** in **SYSTEM CONFIG** to **1**. The zero sequence filtering is done by setting **HV Grounding**, **LV Grounding** and **TV Grounding** in **SYSTEM CONFIG** to **Grounded**. The TV winding is grounded using a grounding transformer inside the protected zone.

The system configuration and differential protection settings are shown in Figure 26:



Group 1	
GROUP 1 SYSTEM CONFIG	
Winding Config	HV+LV
Winding Type	Conventional
HV CT Terminals	011
Ref Power S	163.3 MVA
HV Connection	Y-Wye
HV Grounding	Ungrounded
HV Nominal	500.0 kV
HV Rating	163.3 MVA
% Reactance	40.00%
LV Vector Group	0
LV Connection	Y-Wye
LV Grounding	Ungrounded
LV Nominal	500.0 kV
LV Rating	163.3 MVA
Match Factor CT1	2.121
Match Factor CT2	2.121
Match Factor CT3	5.303
Phase Sequence	Standard ABC
VT Reversal	No Swap
CT1 Reversal	No Swap
CT2 Reversal	No Swap
CT3 Reversal	No Swap

(a) System configuration

GROUP 1 DIFF PROTECTION	
Trans Diff	Enabled
Set Mode	Simple
Is1	100.0e-3PU
K1	30.00%
Is2	1.000PU
K2	80.00%
tDIFF LS	0 s
Is-CTS	1.500PU
Is-HS1	2.500PU
HS2 Status	Disabled
Zero seq filt HV	Disabled
Zero seq filt LV	Disabled
2nd harm blocked	Enabled
Ih(2)%>	10.00%
Cross blocking	Enabled
CTSat and NoGap	Enabled
5th harm blocked	Disabled
Circuitry Fail	Disabled

(b) Differential Protection

P4645ENa

Figure 26 - P645 System Config (a) and Diff Protection settings (b) - Autotransformer

2.1.8.3 Example 3: Autotransformer (P643) - Delta Not Connected

Figure 27 shows the application of a P645 to protect an autotransformer. The power transformer data has been given: 175/175/30 MVA Autotransformer, YNyn0d1, 230/115/13.8 kV. The delta winding is not loaded. The current transformer ratios are as follows: HV CT ratio - 1200/5, LV CT ratio - 1200/5, CTs in each phase at the neutral end of the winding 1200/5.

The winding configuration is set to HV + LV + TV. The CT on the HV line side is connected to T1 CT, the CT on the HV neutral side is connected to T2 CT, and the CT on the LV side is connected to T3 CT.

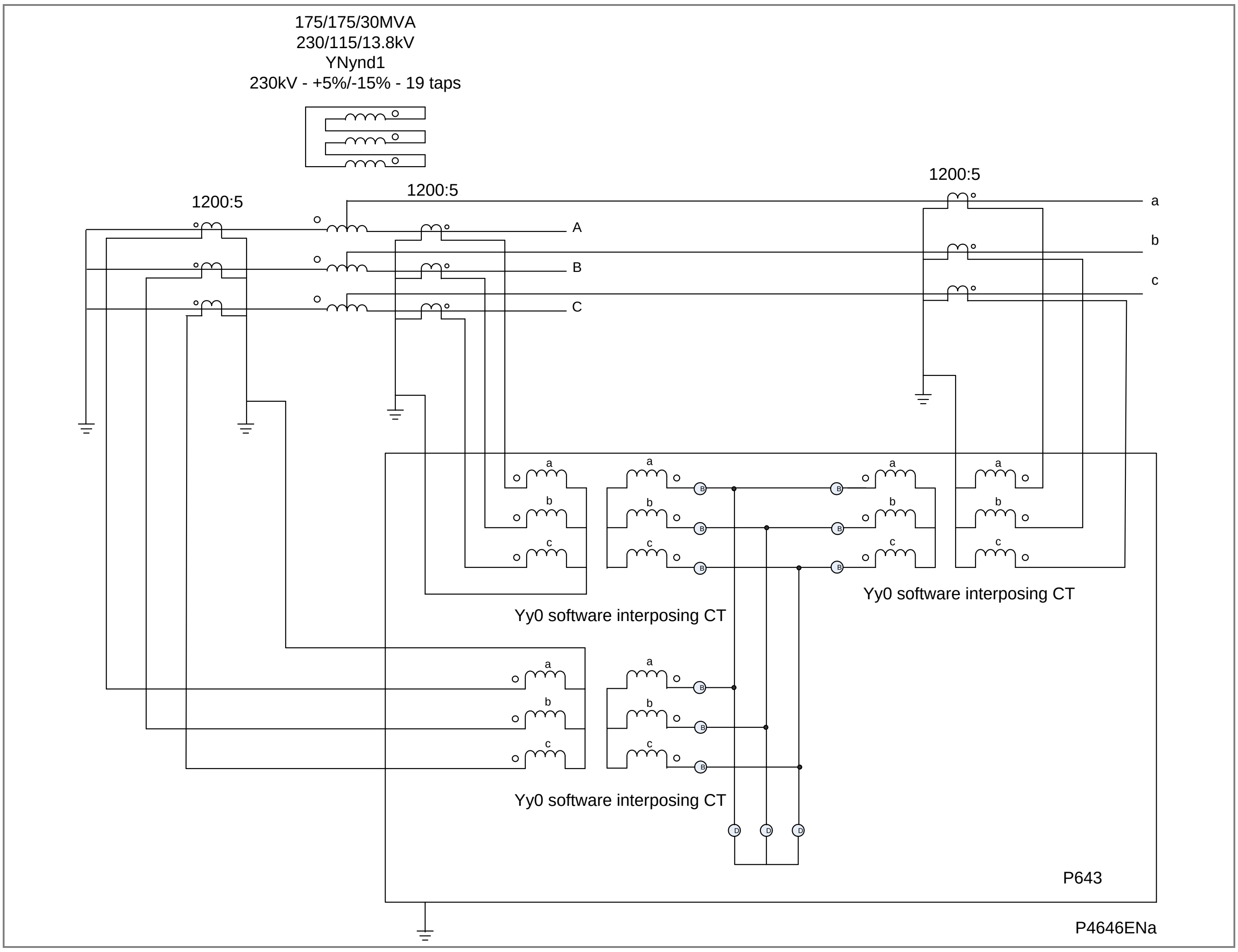

175/175/30MVA
230/115/13.8kV
YNynd1
230kV - +5%/-15% - 19 taps
1200:5
1200:5
1200:5
A
B
C
a
b
c
Yy0 software interposing CT
Yy0 software interposing CT
Yy0 software interposing CT
P643
P4646ENa

Figure 27 - P643 used to protect an autotransformer - delta not connected

Ratio correction:

It is preferred that the ratio correction factors are close or equal to 1. In this example, it is possible to achieve ratio correction factors equal to 1 because current transformers are available in each phase at the neutral end and all the current transformer ratios are the same. This configuration is studied applying Kirchoff's current law. Consider that full load current is flowing and that an equivalent source is connected to the HV winding and an equivalent load is connected to the LV winding. The current distribution is as follows:

$$I_{FLC-HV} = \frac{S}{\sqrt{3}V_{nom,HV}} = \frac{175\times10^{6}}{\sqrt{3}\times230\times10^{3}} = 439A$$

$$I_{FLC-LV} = \frac{S}{\sqrt{3}V_{nom,LV}} = \frac{175 \times 10^6}{\sqrt{3} \times 115 \times 10^3} = 878A$$

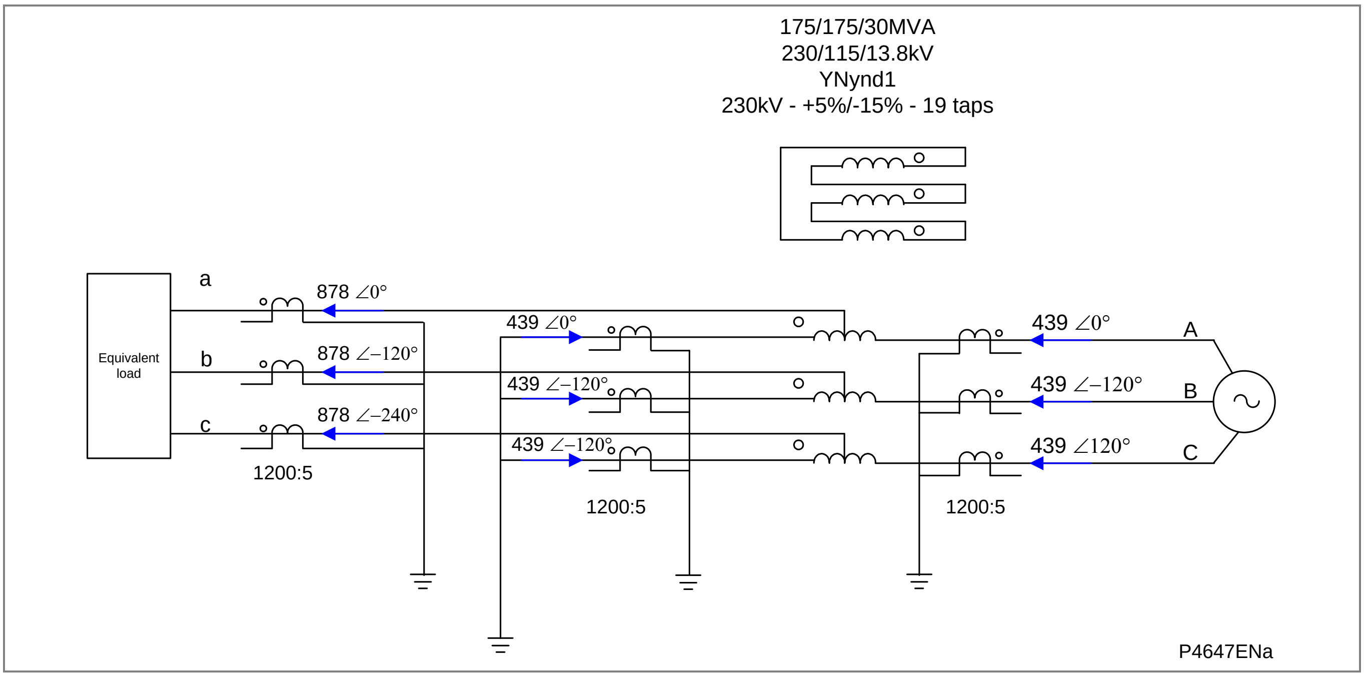

175/175/30MVA
230/115/13.8kV
YNynd1
230kV - +5%/-15% - 19 taps
Equivalent load
a
b
c
878 ∠0°
878 ∠−120°
878 ∠−240°
1200:5
439 ∠0°
439 ∠−120°
439 ∠−120°
1200:5
439 ∠0°
439 ∠−120°
439 ∠120°
1200:5
A
B
C
P4647ENa

Figure 28 - P643 protect an autotransformer – delta not connected – current distribution

The reference power is set to 478 MVA and the nominal voltage in HV, LV and TV windings is set to 230 kV. Note that in this application, even though, there is an on-load tap changer on the HV side, it is not required to consider the mid-tap voltage. It is appropriate to set the reference power to a value other than the one given in the transformer nameplate data because the reference power is used to convert the currents to a common base.

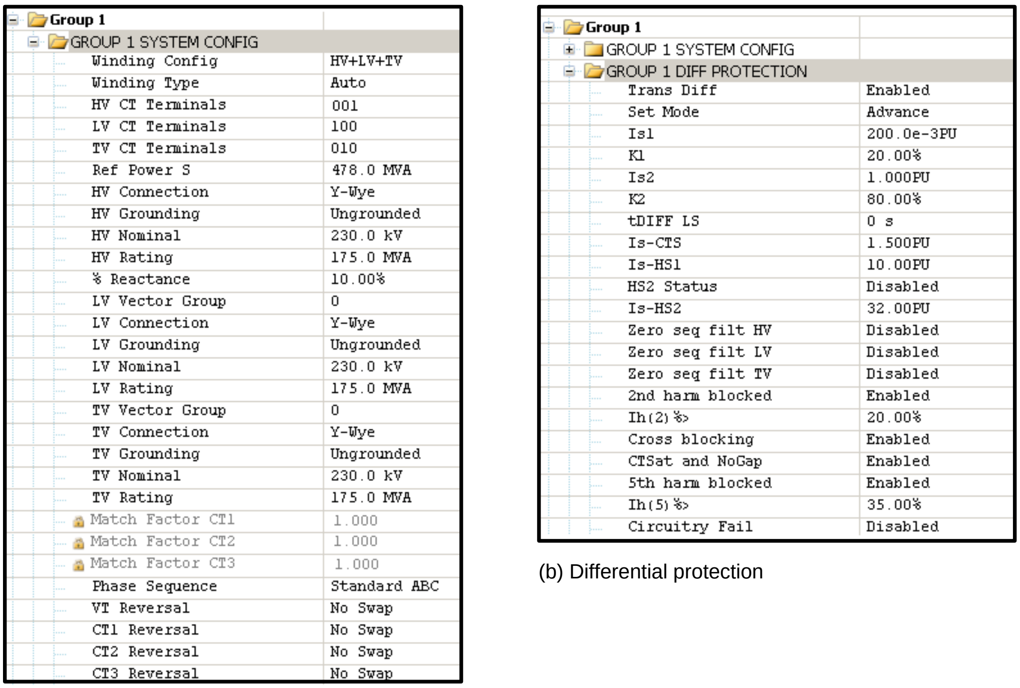
The relay calculates the ratio correction factors as follows:

$$K_{amp,T1CT} = K_{amp,T2CT} = K_{amp,T3CT} = \frac{I_{nom,T1CT}}{\dfrac{S_{ref}}{\sqrt{3}V_{nom}}} = \frac{1200}{\dfrac{478 \times 10^6}{\sqrt{3} \times 230 \times 10^3}} = 1$$

Vector Correction and Zero Sequence Filtering

Vector correction is done by setting **LV Vector Group** in **SYSTEM CONFIG** to **0** and then **TV Vector Group** in **SYSTEM CONFIG** to 0. The zero sequence filtering is done by setting **HV Grounding**, **LV Grounding** and **TV Grounding** in **SYSTEM CONFIG** to **ungrounded**.

The system configuration and differential protection settings are shown in Figure 29:



Winding Config	HV+LV+TV
Winding Type	Auto
HV CT Terminals	001
LV CT Terminals	100
TV CT Terminals	010
Ref Power S	478.0 MVA
HV Connection	Y-Wye
HV Grounding	Ungrounded
HV Nominal	230.0 kV
HV Rating	175.0 MVA
% Reactance	10.00%
LV Vector Group	0
LV Connection	Y-Wye
LV Grounding	Ungrounded
LV Nominal	230.0 kV
LV Rating	175.0 MVA
TV Vector Group	0
TV Connection	Y-Wye
TV Grounding	Ungrounded
TV Nominal	230.0 kV
TV Rating	175.0 MVA
Match Factor CT1	1.000
Match Factor CT2	1.000
Match Factor CT3	1.000
Phase Sequence	Standard ABC
VT Reversal	No Swap
CT1 Reversal	No Swap
CT2 Reversal	No Swap
CT3 Reversal	No Swap

(a) System configuration

Trans Diff	Enabled
Set Mode	Advance
Is1	200.0e-3PU
K1	20.00%
Is2	1.000PU
K2	80.00%
tDIFF LS	0 s
Is-CTS	1.500PU
Is-HS1	10.00PU
HS2 Status	Disabled
Is-HS2	32.00PU
Zero seq filt HV	Disabled
Zero seq filt LV	Disabled
Zero seq filt TV	Disabled
2nd harm blocked	Enabled
Ih(2)%>	20.00%
Cross blocking	Enabled
CTSat and NoGap	Enabled
5th harm blocked	Enabled
Ih(5)%>	35.00%
Circuitry Fail	Disabled

(b) Differential protection

P4648ENa

Figure 29 - P643 System Config (a) and Diff Protection settings (b) – Autotransformer

The differential element does not protect the tertiary winding. Unloaded delta-connected tertiary windings are often not protected. If protection is required, the delta winding can be earthed at one point through a current transformer used to provide instantaneous overcurrent protection for the tertiary winding.

2.1.9 Setting Guidelines for Short-Interconnector Biased Differential Protection

The P645 can be used to protect short interconnectors. Consider the five feeders - single bus scheme and its differential protection zone shown in Figure 30.

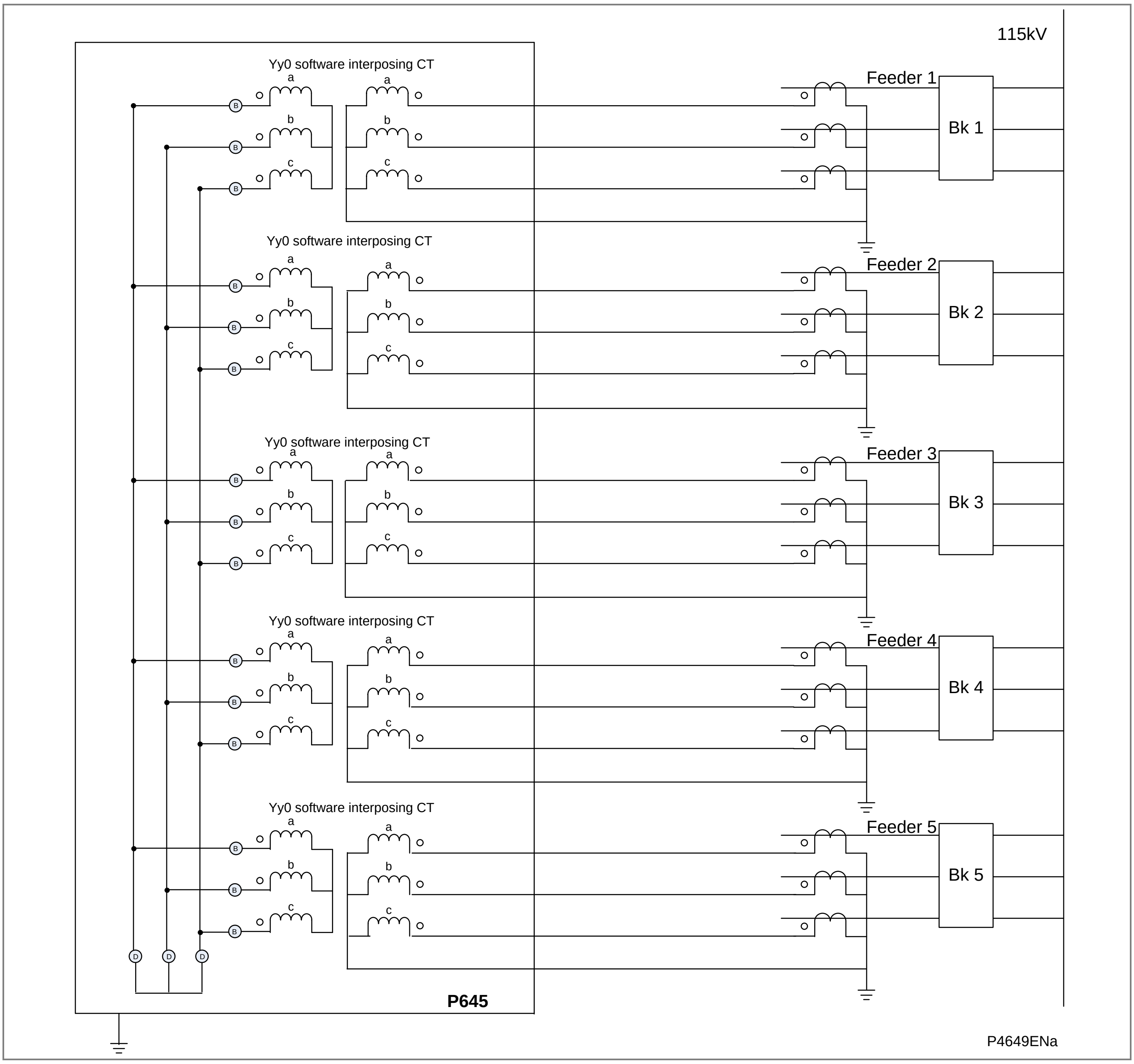

115kV
Yy0 software interposing CT
a
b
c
B
D
Feeder 1
Feeder 2
Feeder 3
Feeder 4
Feeder 5
Bk 1
Bk 2
Bk 3
Bk 4
Bk 5
P645
P4649ENa

Figure 30 - Single bus differential protection zone

- Five biased current inputs are required. Consider that feeder 1 CT is connected to biased current input 1 (T1 CT), feeder 2 CT is connected to biased current input 2 (T2 CT), feeder 3 CT is connected to biased current input 3 (T3 CT), feeder 4 CT is connected to biased current input 4 (T4 CT), feeder 5 CT is connected to biased current input 5 (T5 CT).
- Set the Reference power **Ref Power S** equal to the maximum load (including overloads) in MVA that would be handled by the busbar.

- Set HV Connection, LV Connection and TV Connection as Y-Wye.
  Set HV Grounding, LV Grounding and TV Grounding as Ungrounded, so that the zero sequence filters are disabled.
- Set **HV Nominal**, **LV Nominal** and **TV Nominal** to the system voltage.
- Set **HV Rating**, **LV Rating** and **TV Rating** equal to the Reference power **Ref Power S**. This setting has no impact on the differential protection; it is used by other functions such as the thermal and through-fault monitoring elements which are not required for busbar protection.
- Set the LV Vector Group and TV Vector Group to 0.
- It is highly recommended to use the following settings:
  - Is1 = 1.2pu
  - K1 = 20%
  - K2 = 80%
  - Is2 = 0.4pu
  - Is-HS1 = 10pu
  - Is-HS2 = disabled
  - 2nd harmonic blocked = disabled
  - 5th harmonic blocked = disabled
- Is1 should be set to $1.2 \times \text{highest load} \leq \text{Is1} \leq 0.8 \times \text{minimum fault level}$.
- Set the **Circuitry Fail** alarm to **Enabled**. Set **K-cctfail** to **15%** to allow the maximum composite error of 10% that may be introduced by class 10P current transformers. **Is-cctfail** is typically set between 5 to 20% to prevent detecting noise coming from the CTs and spurious differential current that may be caused by the maximum load unbalance. This element is typically delayed by 5 s.
- It is recommended to apply CT supervision to prevent maloperation of the biased differential protection when there is an open circuited CT secondary. The CTS feature can be used to desensitize the biased differential protection. Desensitization is achieved by raising the differential current pickup setting Is1 to the value of Is-CTS.

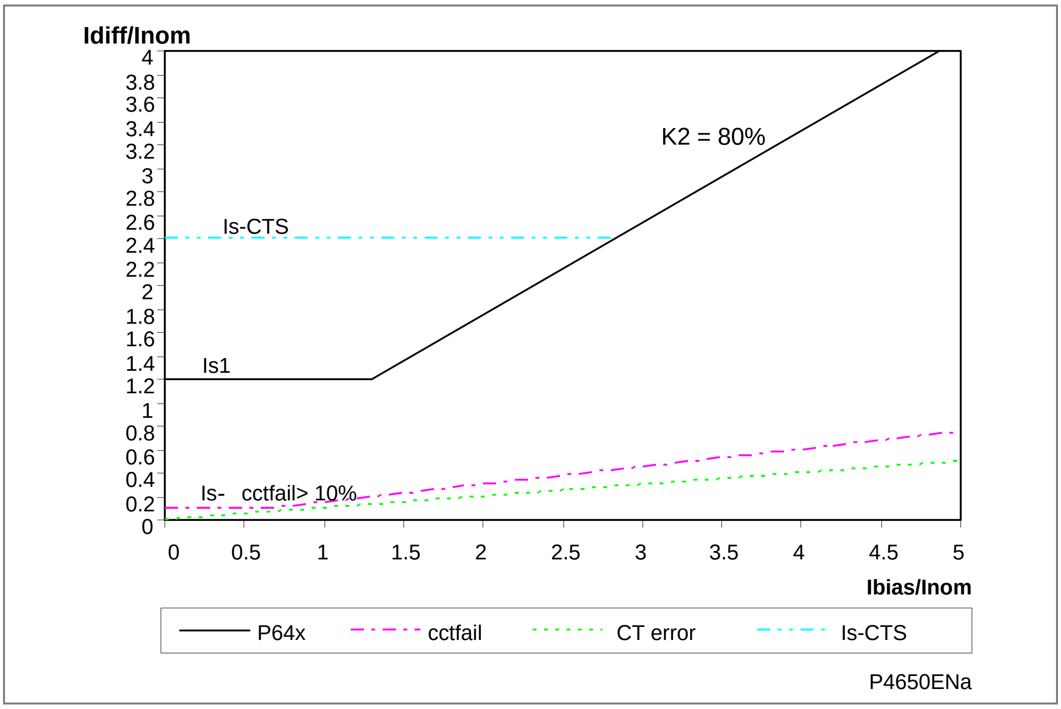
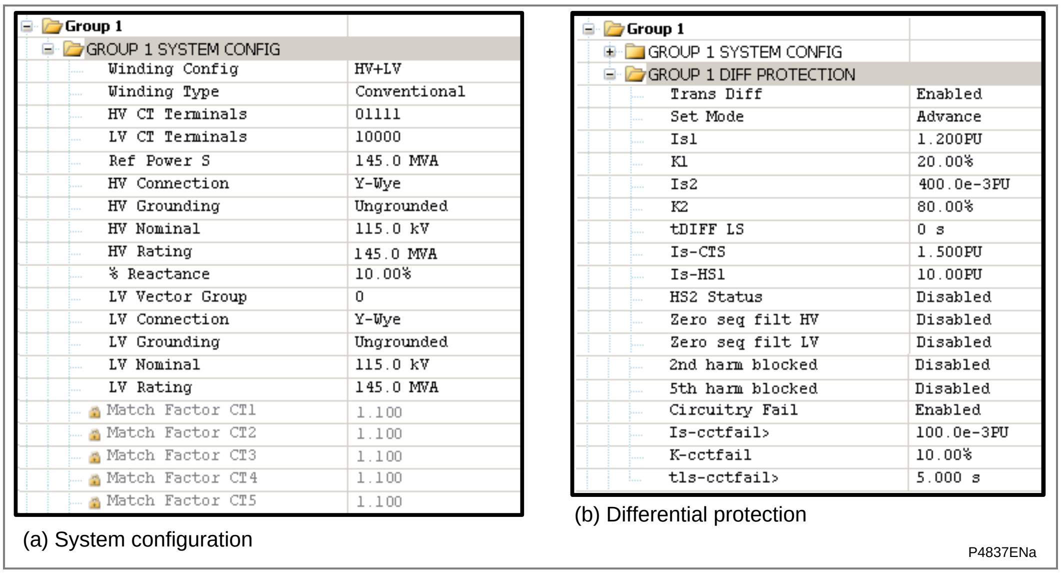


Figure 31 - Busbar biased differential protection



Group 1	
GROUP 1 SYSTEM CONFIG	
Winding Config	HV+LV
Winding Type	Conventional
HV CT Terminals	01111
LV CT Terminals	10000
Ref Power S	145.0 MVA
HV Connection	Y-Wye
HV Grounding	Ungrounded
HV Nominal	115.0 kV
HV Rating	145.0 MVA
% Reactance	10.00%
LV Vector Group	0
LV Connection	Y-Wye
LV Grounding	Ungrounded
LV Nominal	115.0 kV
LV Rating	145.0 MVA
Match Factor CT1	1.100
Match Factor CT2	1.100
Match Factor CT3	1.100
Match Factor CT4	1.100
Match Factor CT5	1.100

(a) System configuration

Group 1	
GROUP 1 SYSTEM CONFIG	
GROUP 1 DIFF PROTECTION	
Trans Diff	Enabled
Set Mode	Advance
Is1	1.200PU
K1	20.00%
Is2	400.0e-3PU
K2	80.00%
tDIFF LS	0 s
Is-CTS	1.500PU
Is-HS1	10.00PU
HS2 Status	Disabled
Zero seq filt HV	Disabled
Zero seq filt LV	Disabled
2nd harm blocked	Disabled
5th harm blocked	Disabled
Circuitry Fail	Enabled
Is-cctfail>	100.0e-3PU
K-cctfail	10.00%
tls-cctfail>	5.000 s

(b) Differential protection

Figure 32 - P645 System Config (a) and Diff Protection settings (b) - Short Interconnector

2.1.10 Setting Guidelines for Short-Interconnector Biased Differential Protection

Reactors are commonly used in the power system:

- To reduce the fault current level in grounded neutrals
- To reduce the phase fault current level when the reactor is connected in series to a line.
- To compensate for the capacitive reactance of long transmission lines or cables when the reactor is connected in shunt. The shunt reactor absorbs the VARs

generated by the line capacitive reactance as the power system generally cannot absorb it.

According to IEEE Std. C37.109-2006 one of the main difficulties with shunt reactor protection is that the relay may mal-operate during iron-core reactor energization and de-energization. A shunt reactor is typically switched in and out regularly depending on the power system load. The iron-core shunt reactor energization current contains dc offset with long time constant and low frequency components as shown in Figure 33. These current waveforms cause a certain level of remanent flux in the CT magnetic core. During normal reactor operation the current is generally the nominal current which is not high enough to reduce the flux level in the CT. In the next switch in operation, the flux may either increase or decrease depending on the point on energization. The regular switch in and out of the reactor causes CT saturation; therefore, it is recommended that the current transformers on both sides of the reactor have similar excitation characteristics to reduce the risk of unwanted operations. A high impedance differential scheme is generally recommended over a low impedance differential scheme, because it is not affected by CT saturation.

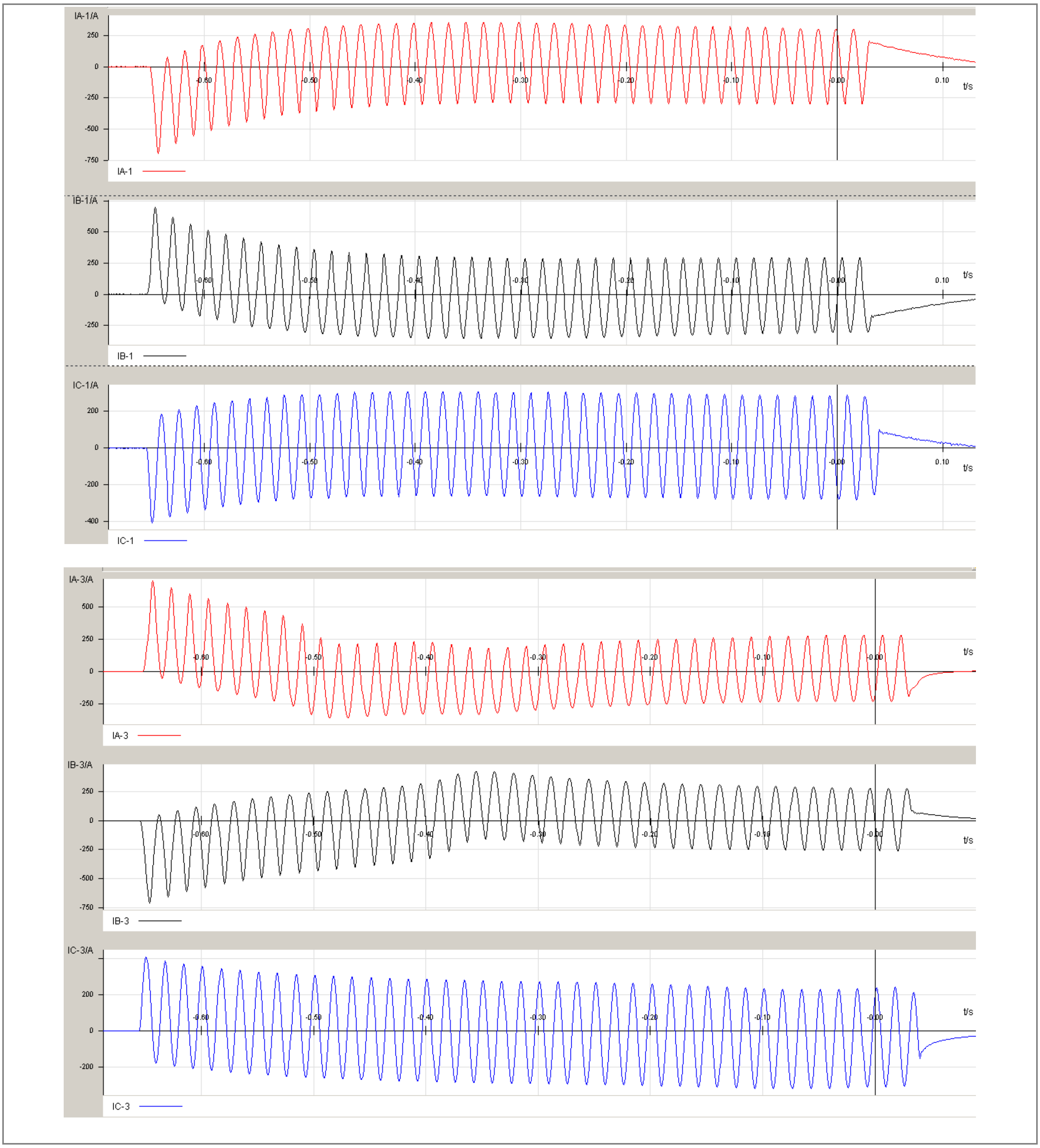


Figure 33 - Reactor energization current

As per the IEEE Std. C37.109-2006 the properties of shut reactors can be summarized as follows:

- Dry air-air core type reactors: no magnetizing inrush during energization as there is no iron core. The peak current during energization might be as high as $2 \times \sqrt{2} \times I_{nominal}$ due to transient offset.

- Oil-immersed type reactors: the gapped iron-core type might experience severe energizing inrush. The coreless type experiences less severe magnetizing inrush.

2.1.10.1 Example 1: Shunt Reactor Differential Protection

Consider the shunt reactor shown in Figure 34.

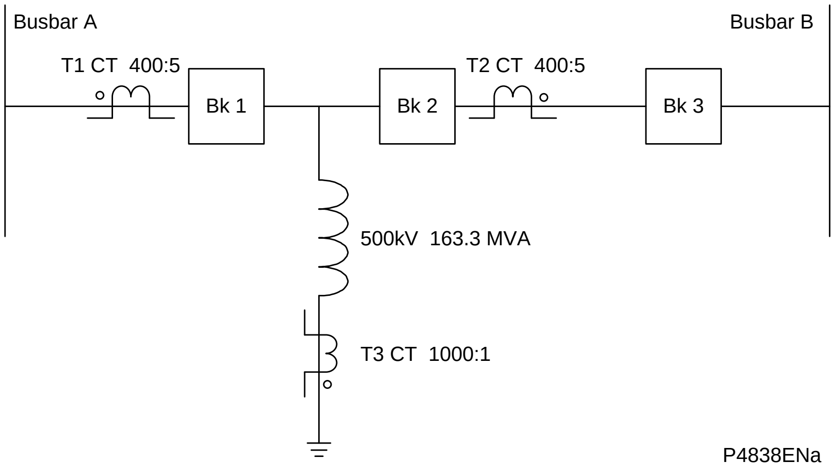
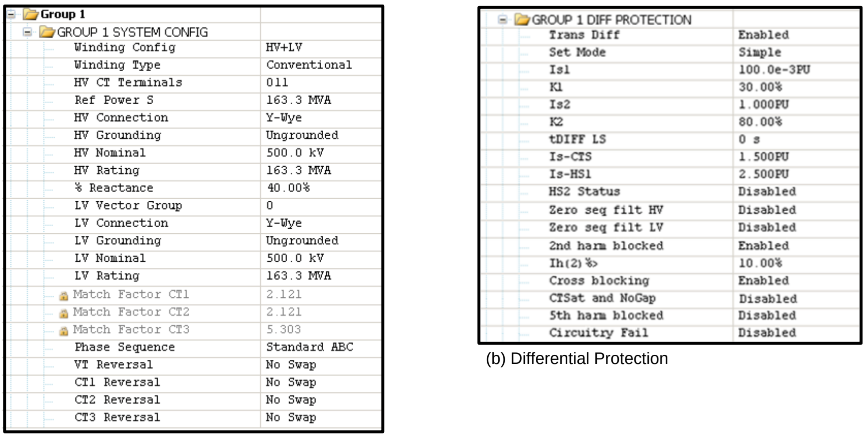


Figure 34 - Reactor single line diagram

The bias differential element in the P643 would be used to protect the reactor. In a reactor application the low set differential element, Is1, should be set between 10%-15%. The second harmonic blocking can be set as low as 10%. This is to enhance the relay stability during energization. The high set 1 differential element, Is-HS1, can be set to 250% of the reactor current at rated voltage.



Group 1	
GROUP 1 SYSTEM CONFIG	
Winding Config	HV+LV
Winding Type	Conventional
HV CT Terminals	011
Ref Power S	163.3 MVA
HV Connection	Y-Wye
HV Grounding	Ungrounded
HV Nominal	500.0 kV
HV Rating	163.3 MVA
% Reactance	40.00%
LV Vector Group	0
LV Connection	Y-Wye
LV Grounding	Ungrounded
LV Nominal	500.0 kV
LV Rating	163.3 MVA
Match Factor CT1	2.121
Match Factor CT2	2.121
Match Factor CT3	5.303
Phase Sequence	Standard ABC
VT Reversal	No Swap
CT1 Reversal	No Swap
CT2 Reversal	No Swap
CT3 Reversal	No Swap

(a) System configuration

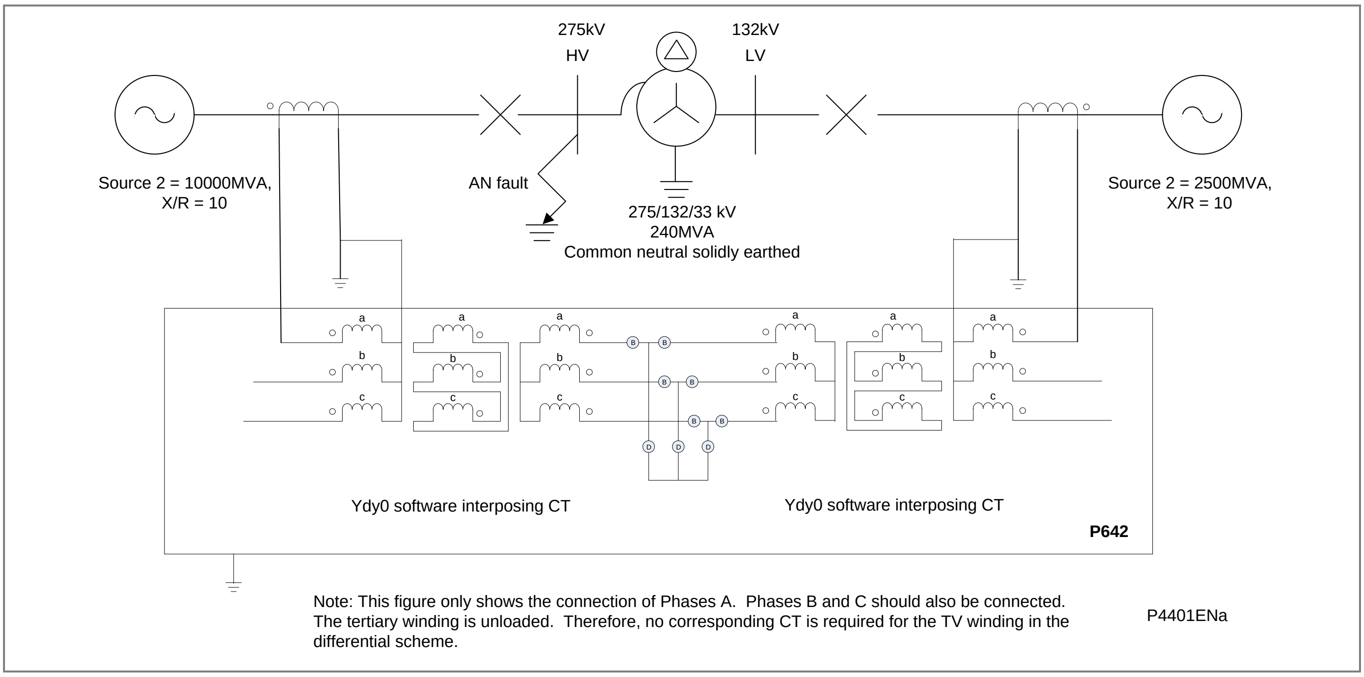
GROUP 1 DIFF PROTECTION	
Trans Diff	Enabled
Set Mode	Simple
Is1	100.0e-3PU
K1	30.00%
Is2	1.000PU
K2	80.00%
tDIFF LS	0 s
Is-CTS	1.500PU
Is-HS1	2.500PU
HS2 Status	Disabled
Zero seq filt HV	Disabled
Zero seq filt LV	Disabled
2nd harm blocked	Enabled
Ih(2)%>	10.00%
Cross blocking	Enabled
CTSat and NoGap	Disabled
5th harm blocked	Disabled
Circuitry Fail	Disabled

(b) Differential Protection

P4839ENa

Figure 35 - P643 system config (a) and diff protection settings (b) – Reactor

2.2 Possible Misindication of the Unfaulted Phases due to Fault Current Distribution


275kV
HV
132kV
LV
Source 2 = 10000MVA,
X/R = 10
AN fault
275/132/33 kV
240MVA
Common neutral solidly earthed
Source 2 = 2500MVA,
X/R = 10
a
b
c
B
D
Ydy0 software interposing CT
Ydy0 software interposing CT
P642
P4401ENa

Note: This figure only shows the connection of Phases A. Phases B and C should also be connected. The tertiary winding is unloaded. Therefore, no corresponding CT is required for the TV winding in the differential scheme.

Figure 36 - AN fault in the HV side of an autotransformer

The positive, negative and zero sequence impedances of the transformer windings using 240 MVA as base are as follows:

	HV	LV	TV
Positive Sequence	j 0.134 pu	j 0.075 pu	-j 0.024 pu
Negative Sequence	j 0.134 pu	j 0.075 pu	-j 0.024 pu
Zero Sequence	j 0.067 pu	j 0.0375 pu	-j 0.012 pu

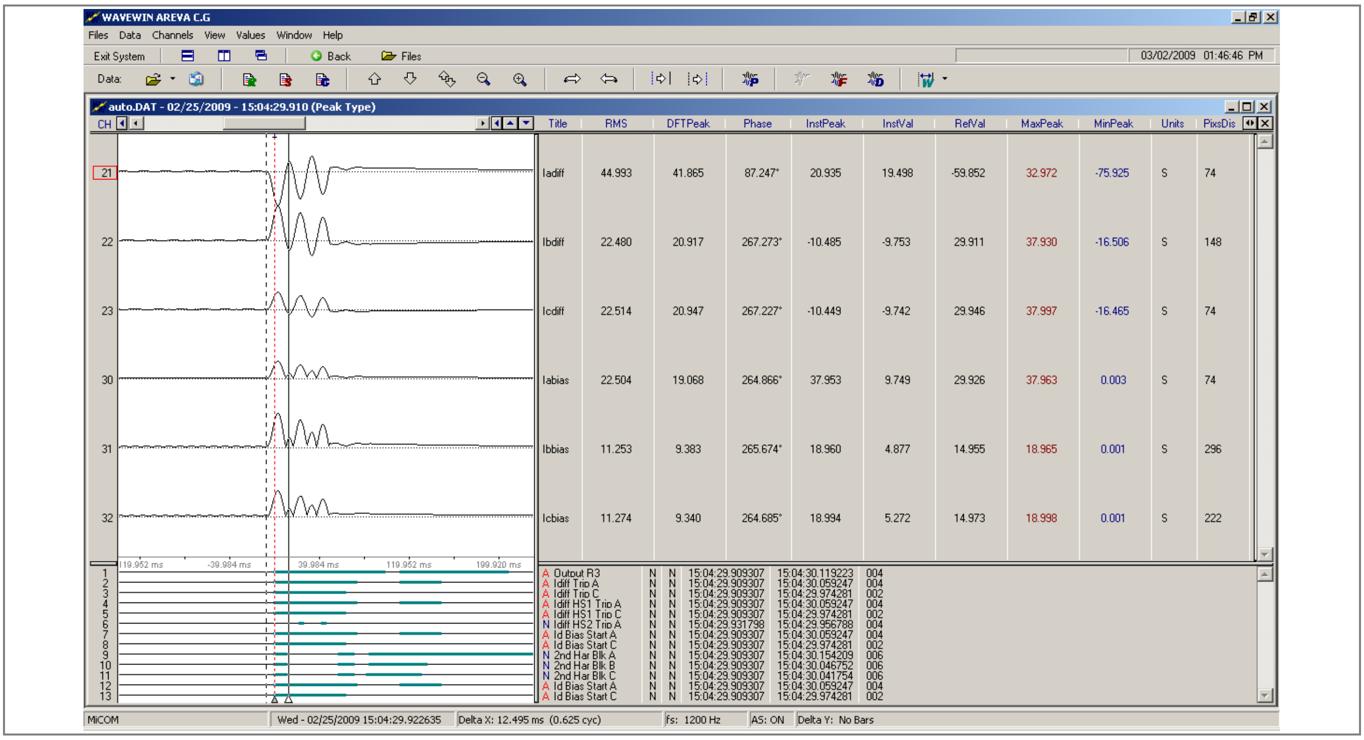
Table 4 - Positive, negative and zero sequence impedances of transformer windings

The X/R ratio determines the angle of the source impedances, so this angle is $\tan^{-1}(10) = 84^\circ$.

The magnitude of source 1 impedance is $1 \times \frac{240}{10000} = 0.024\text{pu}$.

The magnitude of source 2 impedance is $1 \times \frac{240}{2500} = 0.096\text{pu}$

Consider the internal AN fault on the HV side of the autotransformer shown in Figure 36. The disturbance record and events obtained from the relay indicate that the phase C also tripped, even though the fault was on phase A.


WAVEWIN AREVA C.G
Files Data Channels View Values Window Help
Exit System
Back
Files
Data:
03/02/2009 01:46:46 PM
auto.DAT - 02/25/2009 - 15:04:29.910 (Peak Type)
CH
21
22
23
30
31
32
-119.952 ms
-39.984 ms
39.984 ms
119.952 ms
199.920 ms
1
2
3
4
5
6
7
8
9
10
11
12
13

Title	RMS	DFTPeak	Phase	InstPeak	InstVal	RefVal	MaxPeak	MinPeak	Units	PixsDis
Iadiff	44.993	41.865	87.247°	20.935	19.498	-59.852	32.972	-75.925	S	74
Ibdiff	22.480	20.917	267.273°	-10.485	-9.753	29.911	37.930	-16.506	S	148
Icdiff	22.514	20.947	267.227°	-10.449	-9.742	29.946	37.997	-16.465	S	74
Iabias	22.504	19.068	264.866°	37.953	9.749	29.926	37.963	0.003	S	74
Ibbias	11.253	9.383	265.674°	18.960	4.877	14.955	18.965	0.001	S	296
Icbias	11.274	9.340	264.685°	18.994	5.272	14.973	18.998	0.001	S	222

A	Output R3	N	N	15:04:29.909307	15:04:30.119223	004
A	Idiff Trip A	N	N	15:04:29.909307	15:04:30.059247	004
A	Idiff Trip C	N	N	15:04:29.909307	15:04:29.974281	002
A	Idiff HS1 Trip A	N	N	15:04:29.909307	15:04:30.059247	004
A	Idiff HS1 Trip C	N	N	15:04:29.909307	15:04:29.974281	002
N	Idiff HS2 Trip A	N	N	15:04:29.931798	15:04:29.956788	004
A	Id Bias Start A	N	N	15:04:29.909307	15:04:30.059247	004
A	Id Bias Start C	N	N	15:04:29.909307	15:04:29.974281	002
N	2nd Har Blk A	N	N	15:04:29.909307	15:04:30.154209	006
N	2nd Har Blk B	N	N	15:04:29.909307	15:04:30.046752	006
N	2nd Har Blk C	N	N	15:04:29.909307	15:04:30.041754	006
A	Id Bias Start A	N	N	15:04:29.909307	15:04:30.059247	004
A	Id Bias Start C	N	N	15:04:29.909307	15:04:29.974281	002

MiCOM | Wed - 02/25/2009 15:04:29.922635 | Delta X: 12.495 ms (0.625 cyc) | fs: 1200 Hz | AS: ON | Delta Y: No Bars

Figure 37 - Relay disturbance record

The following analysis explains why the phase C differential element also tripped. The sequence networks for an AN fault are shown in Figure 38. All the quantities are in pu.

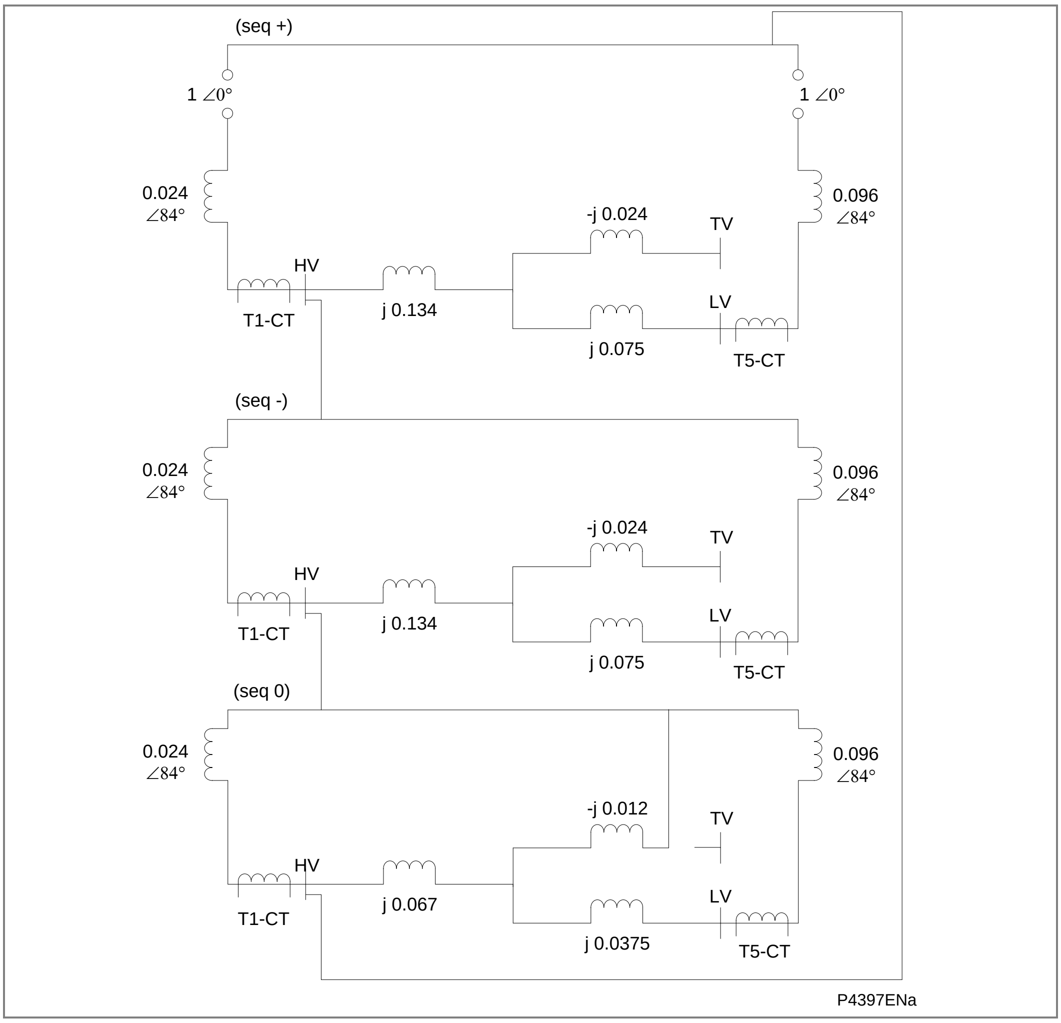

(seq +)
1 ∠0°
1 ∠0°
0.024
∠84°
0.096
∠84°
-j 0.024
TV
HV
j 0.134
LV
T1-CT
j 0.075
T5-CT
(seq -)
0.024
∠84°
0.096
∠84°
-j 0.024
TV
HV
j 0.134
LV
T1-CT
j 0.075
T5-CT
(seq 0)
0.024
∠84°
0.096
∠84°
-j 0.012
TV
HV
j 0.067
LV
T1-CT
j 0.0375
T5-CT
P4397ENa

Figure 38 - Sequence networks

The positive sequence network is simplified as follows:

$$0.096\angle 84^\circ + j0.075 + j0.0134 = 0.305\angle 88.1^\circ \text{pu}$$

The negative sequence network is simplified as follows:

$$0.096\angle 84^\circ + j0.075 + j0.0134 = 0.305\angle 88.1^\circ \text{pu}$$

The zero sequence network is simplified as follows:

$$0.096\angle 84^\circ + j0.0375 = 0.133\angle 85.7^\circ \text{pu}$$

$$\frac{\left(0.133\angle 85.7^\circ\right)\left(-j0.012\right)}{0.133\angle 85.7^\circ + \left(-j0.012\right)} = 0.013\angle -89.6^\circ \text{pu}$$

$$j0.067 + 0.013\angle -89.6^\circ = 0.054\angle 89.9^\circ \text{pu}$$

Therefore the sequence networks in Figure 38 are simplified as follows:

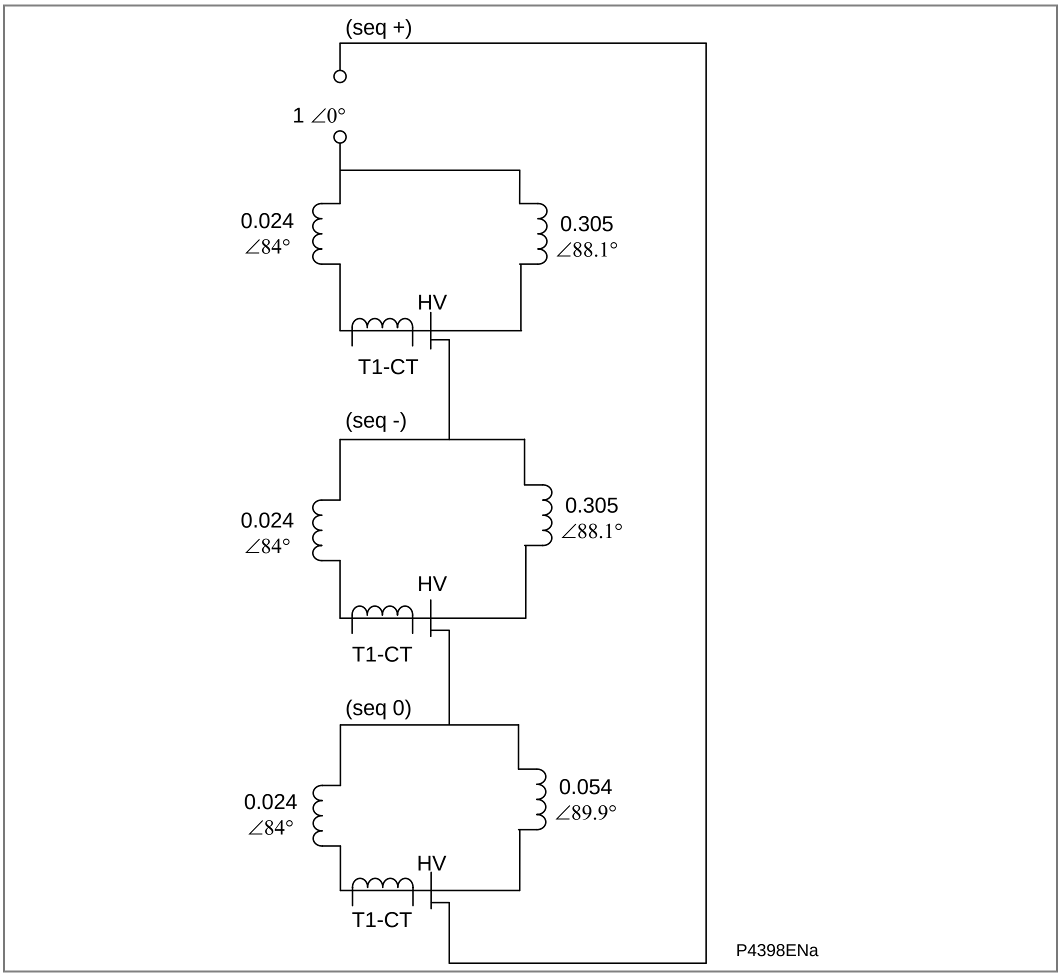

(seq +)
1 ∠0°
0.024
∠84°
0.305
∠88.1°
HV
T1-CT
(seq -)
0.024
∠84°
0.305
∠88.1°
HV
T1-CT
(seq 0)
0.024
∠84°
0.054
∠89.9°
HV
T1-CT
P4398ENa

Figure 39 - Simplified sequence networks

From Figure 39, the equivalent sequence networks impedances are calculated as follows:

Positive sequence equivalent impedance:

$$\frac{(0.024\angle 84^{\circ})(0.305\angle 88.1^{\circ})}{0.024\angle 84^{\circ}+0.305\angle 88.1^{\circ}}=0.022\angle 84.3^{\circ}\,\text{pu}$$

The negative sequence equivalent impedance is the same as the positive sequence equivalent impedance:

$$\frac{(0.024\angle 84^{\circ})(0.305\angle 88.1^{\circ})}{0.024\angle 84^{\circ}+0.305\angle 88.1^{\circ}}=0.022\angle 84.3^{\circ}\,\text{pu}$$

Zero sequence equivalent impedance:

$$\frac{(0.024\angle 84^{\circ})(0.054\angle 89.9^{\circ})}{0.024\angle 84^{\circ}+0.054\angle 89.9^{\circ}}=0.017\angle 85.8^{\circ}\,\text{pu}$$

The sequence networks are now represented by the equivalent impedances in series:

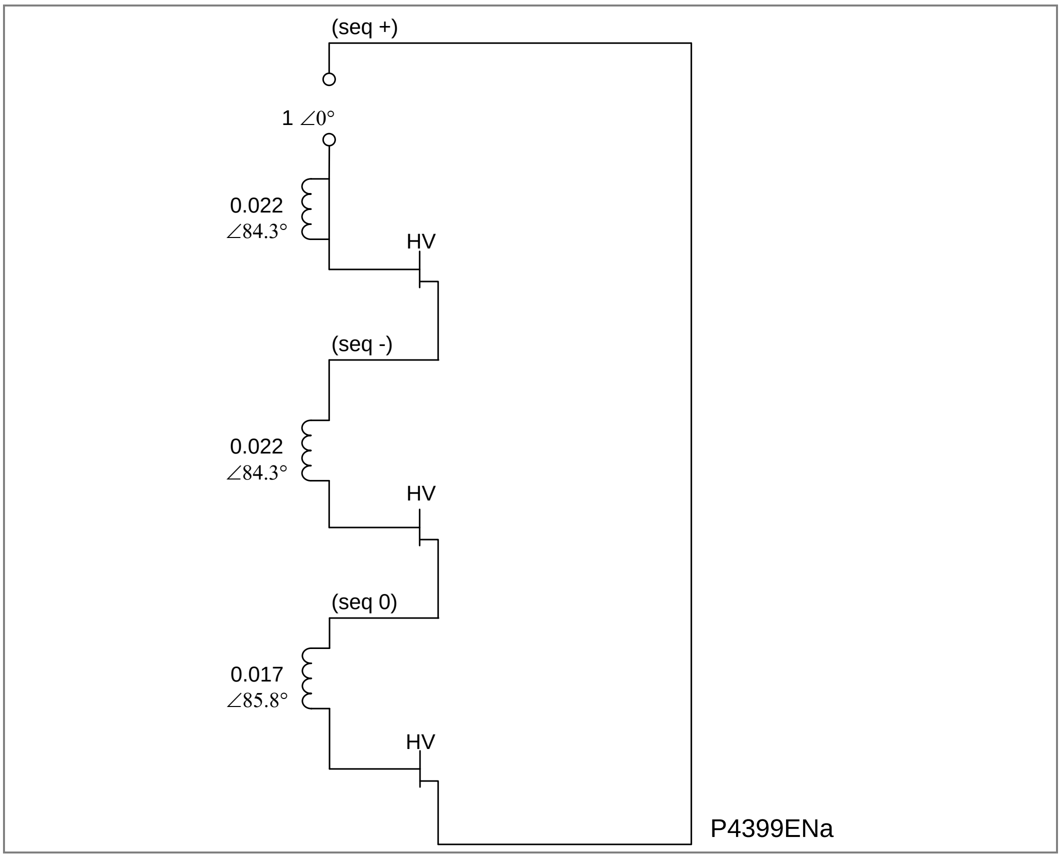


Figure 40 - Sequence networks

The equivalent impedance is:

$$0.022\angle 84.3^\circ + 0.022\angle 84.3^\circ + 0.017\angle 85.8^\circ = 0.061\angle 84.7^\circ \text{pu}$$

The positive, negative and zero sequence currents are:

$$I_0 = I_1 = I_2 = \frac{1}{0.061\angle 84.7^\circ} = 16.4\angle -84.7^\circ \text{pu}$$

The positive sequence currents on the HV side are calculated using a current division:

$$16.4\angle -84.7^\circ \times \frac{0.305\angle 88.1^\circ}{0.024\angle 84^\circ + 0.305\angle 88.1^\circ} = 15.21\angle -84.4^\circ \text{pu}$$

The positive sequence currents on the LV side are calculated using a current division:

$$16.4\angle -84.7^\circ \times \frac{0.024\angle 84^\circ}{0.024\angle 84^\circ + 0.305\angle 88.1^\circ} = 1.2\angle -88.5^\circ \text{pu}$$

The negative sequence currents on the HV and LV side are the same as the positive sequence currents on the HV and LV side respectively.

The zero sequence currents on the HV side are calculated using a current division:

$$16.4\angle -84.7^\circ \times \frac{0.054\angle 89.9^\circ}{0.024\angle 84^\circ + 0.054\angle 89.9^\circ} = 11.4\angle -82.9^\circ \text{pu}$$

The zero sequence currents on the LV side are calculated using a current division:

$$16.4\angle -84.7^\circ \times \frac{0.024\angle 84^\circ}{0.024\angle 84^\circ + 0.054\angle 89.9^\circ} = 5.1\angle -88.8^\circ \text{pu}$$

$$5.1\angle -88.8^\circ \times \frac{-j0.012}{-j0.012 + 0.133\angle 85.7^\circ} = 0.51\angle 95.9^\circ \text{pu}$$

The current distribution in the sequence networks is shown in Figure 41.

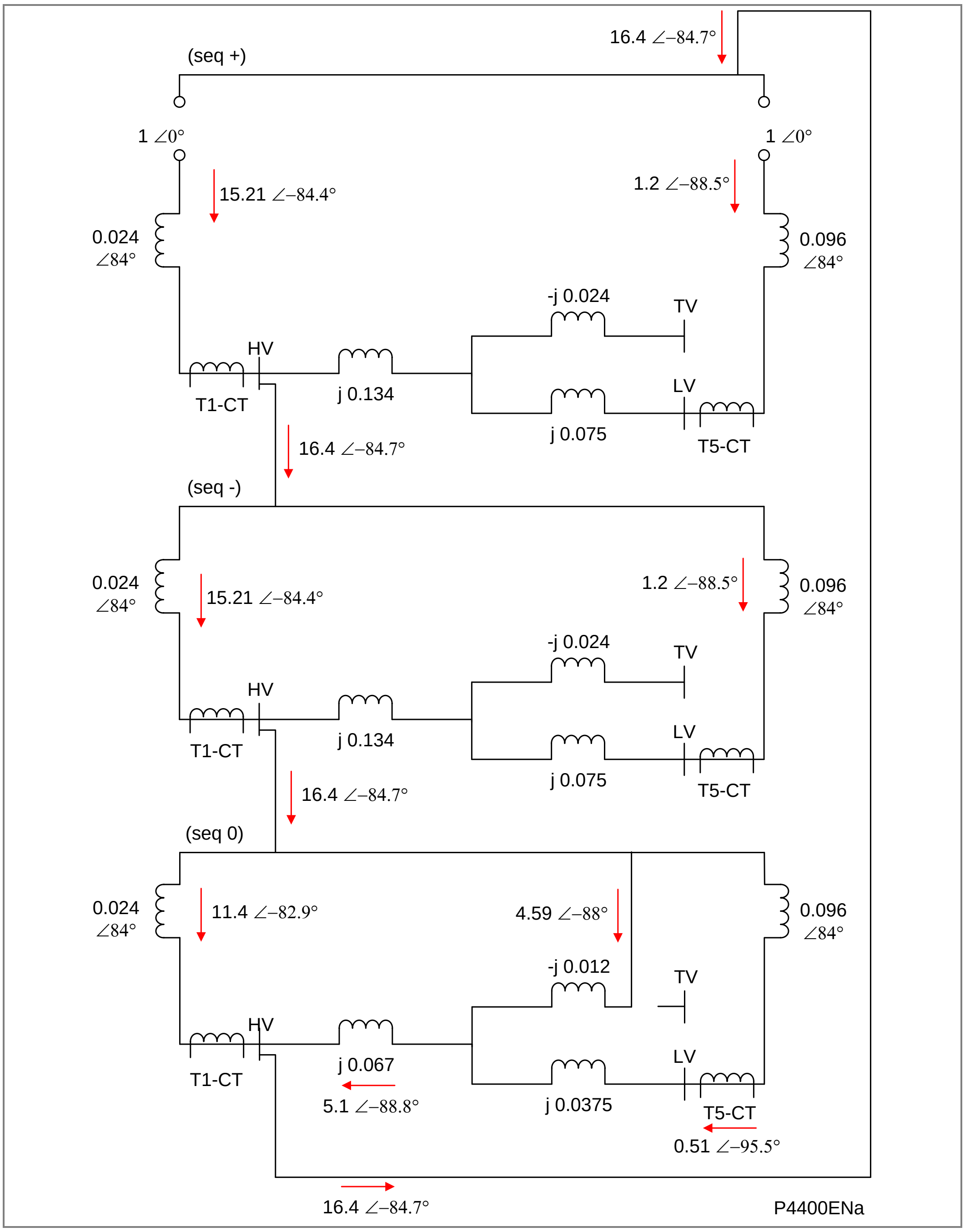

16.4 ∠–84.7°
(seq +)
1 ∠0°
1 ∠0°
15.21 ∠–84.4°
1.2 ∠–88.5°
0.024 ∠84°
0.096 ∠84°
-j 0.024
TV
HV
T1-CT
j 0.134
LV
j 0.075
T5-CT
16.4 ∠–84.7°
(seq -)
0.024 ∠84°
15.21 ∠–84.4°
1.2 ∠–88.5°
0.096 ∠84°
-j 0.024
TV
HV
T1-CT
j 0.134
LV
j 0.075
T5-CT
16.4 ∠–84.7°
(seq 0)
0.024 ∠84°
11.4 ∠–82.9°
4.59 ∠–88°
0.096 ∠84°
-j 0.012
TV
HV
T1-CT
j 0.067
5.1 ∠–88.8°
LV
j 0.0375
T5-CT
0.51 ∠–95.5°
16.4 ∠–84.7°
P4400ENa

Figure 41 - Current distribution in the sequence networks

The currents on the HV and LV side seen by the current transformers T1-CT and T5-CT are calculated as follows using the following matrix:

$$\begin{bmatrix} Ia \\ Ib \\ Ic \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \times \begin{bmatrix} I_0 \\ I_1 \\ I_2 \end{bmatrix}$$

Current calculations on the HV side:

$$Ia = I_0 + I_1 + I_2 = 11.4\angle -82.9^\circ + 15.21\angle -84.4^\circ + 15.21\angle -84.4^\circ = 41.8\angle -84^\circ \text{pu}$$

$$Ib = I_0 + a^2 \times I_1 + a \times I_2$$

$$Ib = 11.4\angle -82.9^\circ + 1\angle 240^\circ \times 15.21\angle -84.4^\circ + 1\angle 120^\circ \times 15.21\angle -84.4^\circ = 3.82\angle 91.1^\circ \text{pu}$$

$$Ic = I_0 + a \times I_1 + a^2 \times I_2$$

$$Ib = 11.4\angle -82.9^\circ + 1\angle 120^\circ \times 15.21\angle -84.4^\circ + 1\angle 240^\circ \times 15.21\angle -84.4^\circ = 3.82\angle 91.1^\circ \text{pu}$$

Current calculations on the LV side:

$$Ia = I_0 + I_1 + I_2 = 0.51\angle 95.9^\circ + 1.2\angle -88.5^\circ + 1.2\angle -88.5^\circ = 1.89\angle -89.7^\circ \text{pu}$$

$$Ib = I_0 + a^2 \times I_1 + a \times I_2$$

$$Ib = 0.51\angle 95.9^\circ + 1\angle 240^\circ \times 1.2\angle -88.5^\circ + 1\angle 120^\circ \times 1.2\angle -88.5^\circ = 1.71\angle 92.8^\circ \text{pu}$$

$$Ic = I_0 + a \times I_1 + a^2 \times I_2$$

$$Ib = 0.51\angle 95.9^\circ + 1\angle 120^\circ \times 1.2\angle -88.5^\circ + 1\angle 240^\circ \times 1.2\angle -88.5^\circ = 1.71\angle 92.8^\circ \text{pu}$$

The ratio correction factors as calculated by the relay are 2.382 on the HV side, and 1.143 on the LV side. These factors can be calculated by the user taking into consideration the CT primary nominal current and the winding full load current at the reference power.

$$\text{HV ratio correction factor } = \frac{1200}{\dfrac{240 \times 10^6}{\sqrt{3} \times 275 \times 10^3}} = 2.382$$

$$\text{LV ratio correction factor } = \frac{1200}{\dfrac{240 \times 10^6}{\sqrt{3} \times 132 \times 10^3}} = 1.143$$

Since it is an autotransformer, HV and LV winding are effectively grounded star. The software interposing CTs are Ydy on each winding as shown in Figure 36. Therefore the zero sequence current is filtered on the HV and LV sides.

Note	*In this example, since the currents have been calculated in pu at the transformer base MVA, the differential calculation has been simplified by comparing the HV and LV pu currents. Therefore the ratio correction factors are not needed for this example.*

The differential currents on each phase is calculated as follows:

$$\text{Iadiff} = \left(\overrightarrow{\text{Ia}}_{\text{HV}} - \overrightarrow{\text{I}}_{0-\text{HV}}\right) + \left(\overrightarrow{\text{Ia}}_{\text{LV}} - \overrightarrow{\text{I}}_{0-\text{LV}}\right)$$

$$\text{Iadiff} = \left(41.8\angle -84^\circ - 11.4\angle -82.9^\circ\right) + \left(1.89\angle -89.7^\circ - 0.51\angle 95.9^\circ\right) = 32.8\angle -84.7^\circ \text{pu}$$

$$\text{Ibdiff} = \left(\overrightarrow{\text{Ib}}_{\text{HV}} - \overrightarrow{\text{I}}_{0-\text{HV}}\right) + \left(\overrightarrow{\text{Ib}}_{\text{LV}} - \overrightarrow{\text{I}}_{0-\text{LV}}\right)$$

$$\text{Ibdiff} = \left(3.82\angle 91.1^\circ - 11.4\angle -82.9^\circ\right) + \left(1.71\angle 92.8^\circ - 0.51\angle 95.9^\circ\right) = 16.4\angle -95.3^\circ \text{pu}$$

$$\text{Icdiff} = \left(\overrightarrow{\text{Ic}}_{\text{HV}} - \overrightarrow{\text{I}}_{0-\text{HV}}\right) + \left(\overrightarrow{\text{Ic}}_{\text{LV}} - \overrightarrow{\text{I}}_{0-\text{LV}}\right)$$

$$\text{Icdiff} = \left(3.82\angle 91.1^\circ - 11.4\angle -82.9^\circ\right) + \left(1.71\angle 92.8^\circ - 0.51\angle 95.9^\circ\right) = 16.4\angle -95.3^\circ \text{pu}$$

The mean bias currents are calculated as follows:

$$\text{Iabias} = 0.5 \times \left(\left|\overrightarrow{\text{Ia}}_{\text{HV}} - \overrightarrow{\text{I}}_{0-\text{HV}}\right| + \left|\overrightarrow{\text{Ia}}_{\text{LV}} - \overrightarrow{\text{I}}_{0-\text{LV}}\right|\right)$$

$$\text{Iabias} = 0.5 \times \left(\left|41.8\angle -84^\circ - 11.4\angle -82.9^\circ\right| + \left|1.89\angle -89.7^\circ - 0.51\angle 95.9^\circ\right|\right) = 16.4\text{pu}$$

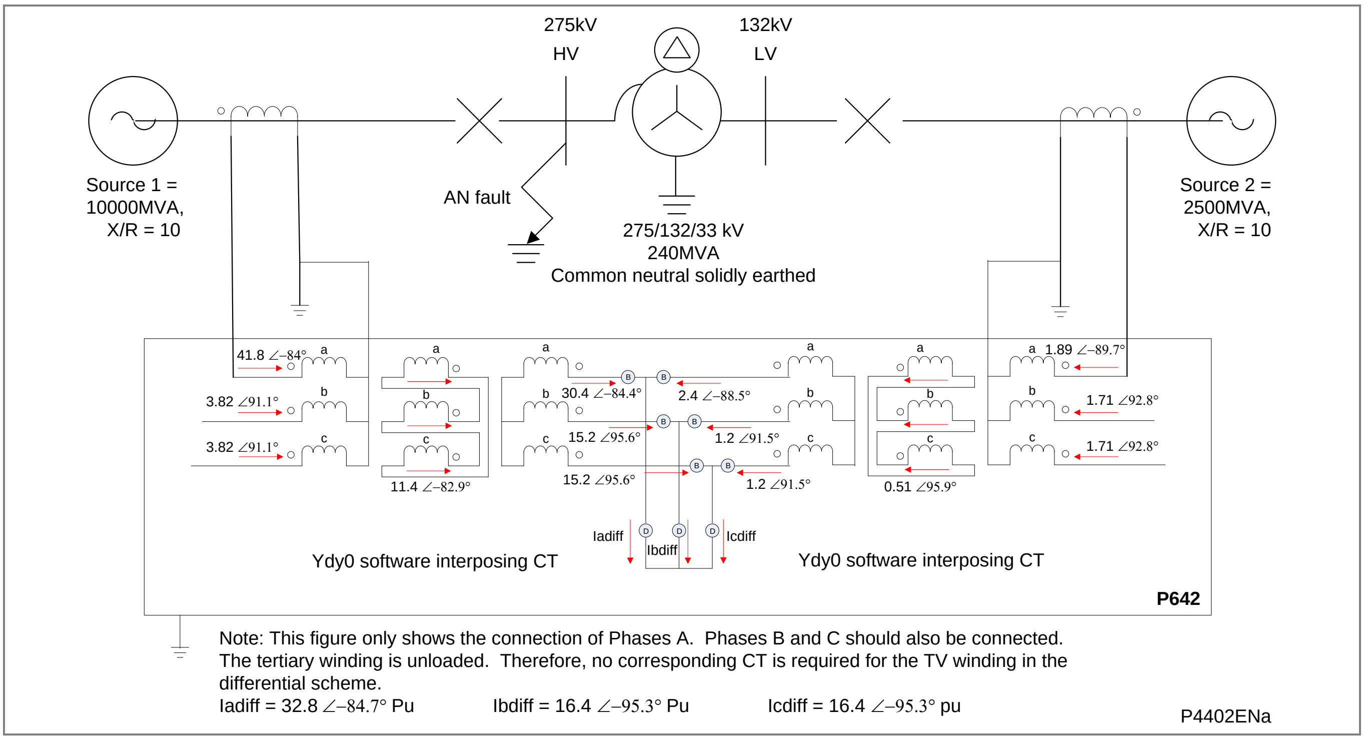
$$\text{Ibbias} = 0.5 \times \left(\left|\overrightarrow{\text{Ib}}_{\text{HV}} - \overrightarrow{\text{I}}_{0-\text{HV}}\right| + \left|\overrightarrow{\text{Ib}}_{\text{LV}} - \overrightarrow{\text{I}}_{0-\text{LV}}\right|\right)$$

$$\text{Ibbias} = 0.5 \times \left(\left|3.82\angle 91.1^\circ - 11.4\angle -82.9^\circ\right| + \left|1.71\angle 92.8^\circ - 0.51\angle 95.9^\circ\right|\right) = 8.2\text{pu}$$

$$\text{Icbias} = 0.5 \times \left(\left|\overrightarrow{\text{Ic}}_{\text{HV}} - \overrightarrow{\text{I}}_{0-\text{HV}}\right| + \left|\overrightarrow{\text{Ic}}_{\text{LV}} - \overrightarrow{\text{I}}_{0-\text{LV}}\right|\right)$$

$$\text{Icbias} = 0.5 \times \left(\left|3.82\angle 91.1^\circ - 11.4\angle -82.9^\circ\right| + \left|1.71\angle 92.8^\circ - 0.51\angle 95.9^\circ\right|\right) = 8.2\text{pu}$$

The current distribution within the P642 is shown in Figure 42.


275kV
HV
132kV
LV
Source 1 =
10000MVA,
X/R = 10
AN fault
275/132/33 kV
240MVA
Common neutral solidly earthed
Source 2 =
2500MVA,
X/R = 10
41.8 ∠−84°
a
3.82 ∠91.1°
b
3.82 ∠91.1°
c
a
b
c
11.4 ∠−82.9°
a
b
30.4 ∠−84.4°
c
15.2 ∠95.6°
15.2 ∠95.6°
B
B
B
B
B
B
2.4 ∠−88.5°
1.2 ∠91.5°
1.2 ∠91.5°
a
b
c
a
b
c
0.51 ∠95.9°
a
1.89 ∠−89.7°
b
1.71 ∠92.8°
c
1.71 ∠92.8°
Iadiff
Ibdiff
Icdiff
D
D
D
Ydy0 software interposing CT
Ydy0 software interposing CT
P642
P4402ENa

Note: This figure only shows the connection of Phases A. Phases B and C should also be connected. The tertiary winding is unloaded. Therefore, no corresponding CT is required for the TV winding in the differential scheme.

Iadiff = 32.8 ∠−84.7° Pu Ibdiff = 16.4 ∠−95.3° Pu Icdiff = 16.4 ∠−95.3° pu

Figure 42 - Current distribution within the P642

The bias current used by the relay for all the phases is the maximum bias current. In this case the relay will use Iabias.

From the above calculations it can be observed that all three phases are much greater than the high set one element (Is-HS1), which has been set to 4.9 pu. As mentioned in the operation chapter, for the relay to trip for Is-HS1, the differential current should be above the Is-HS1 setting and in the operating region of the bias characteristic. Therefore, due to the current distribution during the internal AN fault, the differential elements for phases B and C may trip even though these phases are not faulted.

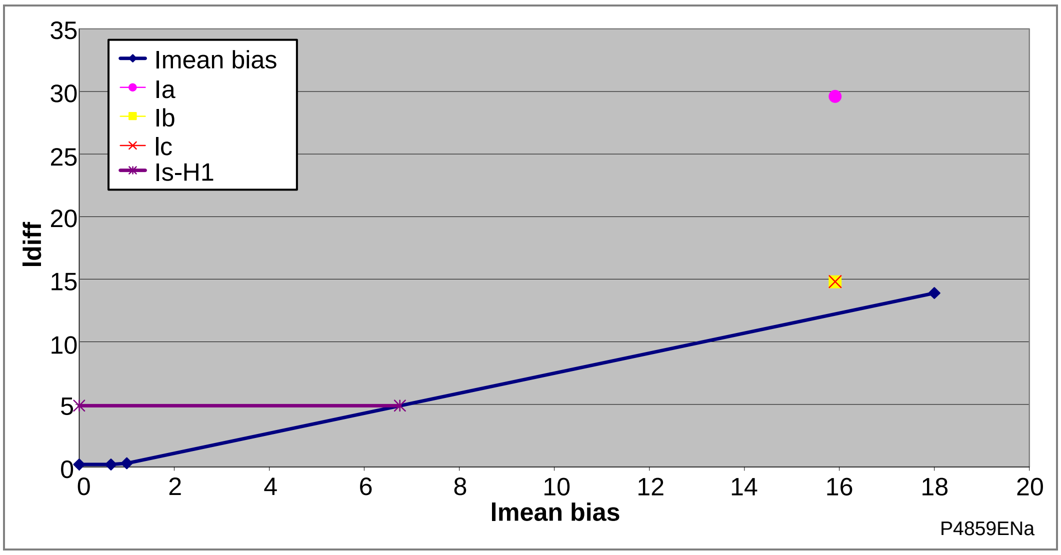


Figure 43 - Differential characteristic

It is important to note that all the calculations have only taken into consideration the mean bias and mean differential currents. The relay also adds an additional transient bias quantity to the operating current. It should be noted that due to the effect of transient bias

if the differential calculations of the non-faulted phases are close to the bias characteristic, then these un-faulted phases may not operate.
The current distribution in this system is shown in Figure 44. The positive, negative and zero sequence currents in the HV terminal were calculated already, and they are as follows:

- Positive sequence = $1.2\angle -88.5^\circ \text{pu}$
- Negative sequence = $1.2\angle -88.5^\circ \text{pu}$
- Zero sequence = $5.1\angle -88.8^\circ \text{pu}$

The phase currents in the autotransformer HV terminal are calculated as follows:

$$Ia = I_0 + I_1 + I_2 = 5.1\angle -88.8^\circ + 1.2\angle -88.5^\circ + 1.2\angle -88.5^\circ = 7.5\angle -88.7^\circ \text{pu}$$

$$Ib = I_0 + a^2 \times I_1 + a \times I_2$$

$$Ib = 5.1\angle -88.8^\circ + 1\angle 240^\circ \times 1.2\angle -88.5^\circ + 1\angle 120 \times 1.2\angle -88.5^\circ = 3.9\angle -88^\circ \text{pu}$$

$$Ic = I_0 + a \times I_1 + a^2 \times I_2$$

$$Ib = 5.1\angle -88.8^\circ + 1\angle 120 \times 1.2\angle -88.5^\circ + 1\angle 240^\circ \times 1.2\angle -88.5^\circ = 3.9\angle -88^\circ \text{pu}$$

To analyse the current distribution of the autotransformer, the current values need to be converted from pu to amperes. Then Kirchoff’s current law is then applied.

The base current in the 275kV side is $\dfrac{240 \times 10^6}{\sqrt{3} \times 275 \times 10^3} = 504\text{A}$.

The base current in the 132kV side is $\dfrac{240 \times 10^6}{\sqrt{3} \times 132 \times 10^3} = 1050\text{A}$.

The currents flowing from source 1 are:

$$IA = 41.8\angle -84\text{pu} = 41.8\angle -84^\circ \times 504 = 21067\angle -84^\circ \text{A}$$

$$IB = 3.82\angle 91.1\text{pu} = 3.82\angle 91.1^\circ \times 504 = 1925\angle 91.1^\circ \text{A}$$

$$IC = 3.82\angle 91.1\text{pu} = 3.82\angle 91.1^\circ \times 504 = 1925\angle 91.1^\circ \text{A}$$

$$3I0 = 3 \times 11.4\angle -82.9^\circ = 34.2\angle -82.9^\circ \text{pu} = 34.2\angle -82.9^\circ \times 504 = 17237\angle -82.9^\circ \text{A}$$

The currents flowing from source 2 to the autotransformer LV terminal are:

$$IA = 1.89\angle -89.7\text{pu} = 1.89\angle -89.7^\circ \times 1050 = 1985\angle -89.7^\circ \text{A}$$

$$IB = 1.71\angle 92.8\text{pu} = 1.71\angle 92.8^\circ \times 1050 = 1796\angle 92.8^\circ \text{A}$$

$$IC = 1.71\angle 92.8\text{pu} = 1.71\angle 92.8^\circ \times 1050 = 1796\angle 92.8^\circ \text{A}$$

$$3I0 = 3 \times 0.51\angle 95.9^\circ = 1.53\angle 95.9^\circ \text{pu} = 1.53\angle 95.9^\circ \times 1050 = 1607\angle 95.5^\circ \text{A}$$

The currents flowing from the autotransformer HV terminal are:

$$IA = 7.5\angle -88.7\text{pu} = 7.5\angle -88.7^\circ \times 504 = 3780\angle -88.7^\circ \text{A}$$

$$IB = 3.9\angle -88pu = 3.9\angle -88^{\circ} \times 504 = 1966\angle -88^{\circ}\,A \approx 1925\angle 91.1^{\circ}\,A$$

$$IC = 3.9\angle -88pu = 3.9\angle -88^{\circ} \times 504 = 1966\angle -88^{\circ} \approx A1925\angle 91.1^{\circ}\,A$$

$$3I0 = 3\times 5.1\angle -88.8^{\circ} = 15.3\angle -88.8^{\circ}pu = 15.3\angle -88.8^{\circ} \times 1504 = 7610\angle -88.8^{\circ}\,A$$

As expected, the currents in phases B and C in the autotransformer HV terminal are the same as the currents in phases B and C in source 1.

The current in the ground of the autotransformer is the subtraction of $3I_{0\text{-HV}}$ minus $3I_{0\text{-LV}}$:

$$3I_{0-HV} - 3I_{0-LV} = 7610\angle -88.8^{\circ} - 1607\angle 95.5^{\circ} = 9213\angle -88^{\circ}\,A$$

The zero sequence current trapped in the delta is calculated using current division as follows:

$$5.1\angle -88.8^{\circ} \times \frac{0.133\angle 85.7^{\circ}}{-j0.012 + 0.133\angle 85.7^{\circ}} = 5.6\angle -88.4^{\circ}pu$$

The base current in the 33kV side is $\frac{240\times 10^{6}}{\sqrt{3}\times 33\times 10^{3}} = 4199\,A$.

Therefore the current trapped in the delta is 5.6∠-88.4° × 4199 = 23514 ∠-88.4° A.

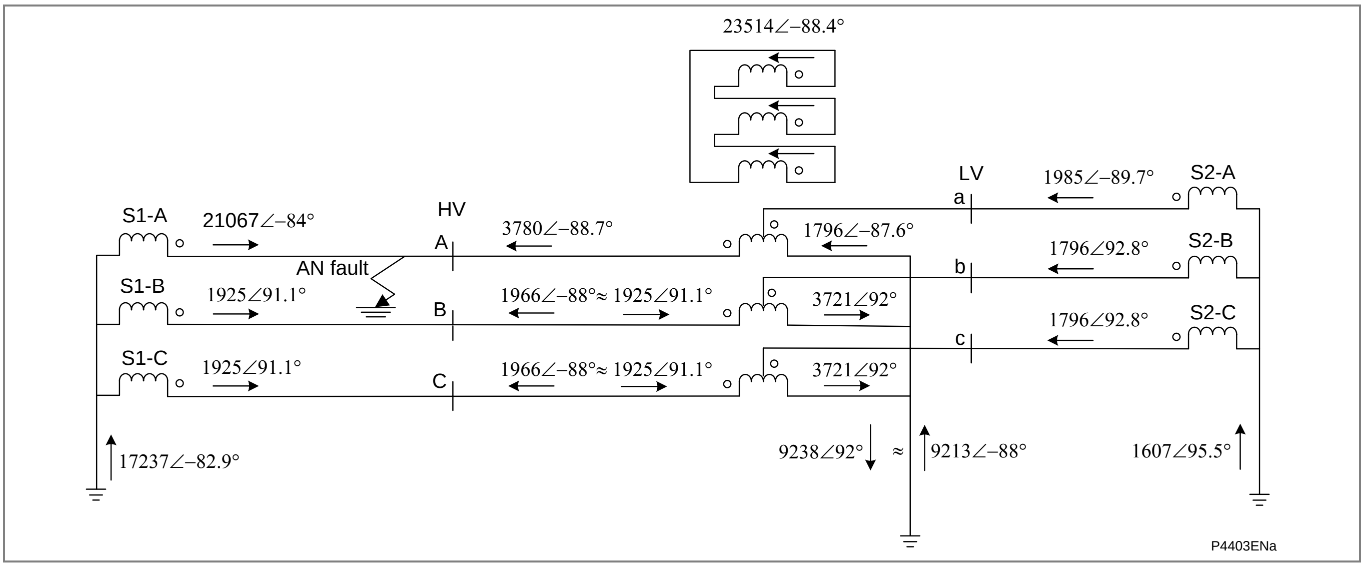

23514∠−88.4°
LV
a
b
c
1985∠−89.7°
S2-A
1796∠92.8°
S2-B
1796∠92.8°
S2-C
S1-A
21067∠−84°
HV
A
3780∠−88.7°
1796∠−87.6°
AN fault
S1-B
1925∠91.1°
B
1966∠−88°≈ 1925∠91.1°
3721∠92°
S1-C
1925∠91.1°
C
1966∠−88°≈ 1925∠91.1°
3721∠92°
17237∠−82.9°
9238∠92°
≈
9213∠−88°
1607∠95.5°
P4403ENa

Figure 44 - Current distribution

2.3 Restricted Earth Fault Protection

2.3.1 Basic Principles

An earth fault is the most common type of fault that occurs in a transformer. The following conditions must be satisfied for an earth fault current to flow:

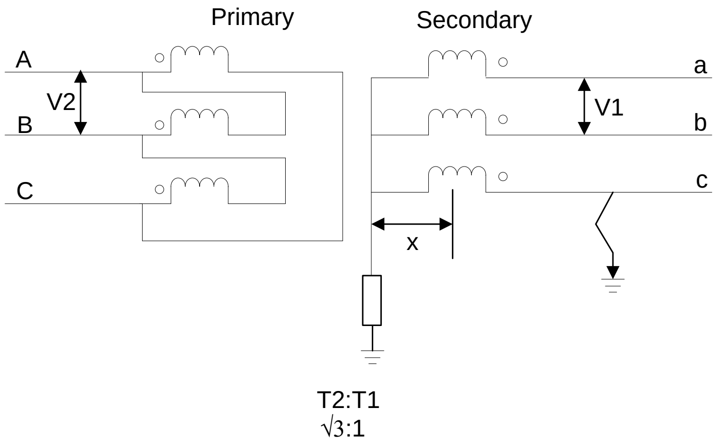
- A path exists for the current to flow into and out of the windings (a zero sequence path)

- The ampere turns balance is maintained between the windings

The magnitude of earth fault current is dependent on the method of earthing (solid or resistance) and the transformer connection.

Consider the resistance earthed star winding shown in Figure 45. An earth fault on such a winding causes a current which is dependent on the value of earthing impedance. This earth fault current is proportional to the distance of the fault from the neutral point since the fault voltage is directly proportional to this distance.

The ratio of transformation between the primary winding and the short circuited turns also varies with the position of the fault. Therefore the current that flows through the transformer terminals is proportional to the square of the fraction of the winding which is short circuited.



The earthing resistor is rated to pass full load current $\frac{V_1}{\sqrt{3}R} = I_{FLC}$

Assuming that V1 = V2 then:

$$V1\phi = T1$$

$$V2\phi = T2$$

$$\frac{V1}{V2} = \frac{\sqrt{3}\cdot V1\phi}{V2\phi} = \frac{\sqrt{3}\cdot T1}{T2}$$

$$1 = \frac{\sqrt{3}\cdot T1}{T2} \Rightarrow T2 = \sqrt{3}\cdot T1$$

For a fault at x pu distance from the neutral If is $I_f = \frac{x.V_1}{\sqrt{3}R}$

The secondary fault current referred to the primary is $I\,\text{primary} = \frac{x\cdot V_1}{\sqrt{3}R}\;\frac{x\cdot T_1}{T_2}$

$$= x^2\cdot I_{FLC}\,\frac{1}{\sqrt{3}}$$

P4307ENa

Figure 45 - Star winding resistance earthed

If the fault in Figure 45 is a single end fed fault, the primary current should be greater than 0.2 pu (Is1 default setting) for the differential protection to operate. Therefore,

$$\frac{x^2}{\sqrt{3}} > 20\%$$

Table 5 shows that 41% of the winding is protected by the differential element.

x	Idiff in %
10	0.58
20	2.31
30	5.20
40	9.24
50	14.43
59	20.00
70	28.29
80	36.95
90	46.77
100	57.74

59% of
unprotected winding

41% of
protected winding

Table 5 - % of winding protected by differential element

In a solidly earthed star winding, the fault current is limited only by the leakage reactance of the winding, which varies in a complex manner with the position of the fault. For the majority of the winding the fault current is approximately 3 x I_{FLC}, reaching a maximum of 5 x I_{FLC}.

Earth faults occurring in a transformer winding or terminal may be of limited magnitude, either due to the impedance present in the earth path or by the percentage of transformer winding that is involved in the fault. It is common to apply standby earth fault protection fed from a single CT in the transformer earth connection; this provides time-delayed protection for a transformer winding or terminal fault. In general, particularly as the size of the transformer increases, it becomes unacceptable to rely on time delayed protection to clear winding or terminal faults as this would lead to an increased amount of damage to the transformer. A common requirement is therefore to provide instantaneous phase and earth fault protection. Applying differential protection across the transformer may also fulfil these requirements. However, an earth fault occurring on the LV winding, particularly if it is of a limited level, may not be detected by the differential relay, as it is only measuring the corresponding HV current. Therefore instantaneous protection is applied that is restricted to operating for transformer earth faults only. This is referred to as restricted, or balanced, earth fault protection (REF or BEF). The BEF terminology is usually used when the protection is applied to a delta winding.

The P64x uses biased differential protection to provide fast clearance for faults within the protected zone. The value of earth fault current, however, may be limited by any impedance in the earth path or by the percentage of the winding involved in the fault. The P64x offers a restricted earth fault element for up to 3 windings of the protected transformer to provide greater sensitivity for earth faults which will not change with load current.

The levels of fault current available for relay measurement are shown below. If an earth fault is considered on an impedance earthed star winding of a Dyn transformer (Figure 46), the value of current flowing in the fault (If) depends on two factors. These are the value of earthing impedance and the fault point voltage, which is governed by the fault location. The value of fault current (If) is directly proportional to the location of the fault as shown in Figure 46. A restricted earth fault element (64) is connected to measure If directly, to provide more sensitive earth fault protection. The overall differential protection is less sensitive, since it only measures the HV current Is. The value of Is is limited by the number of faulty secondary turns in relation to the HV turns.

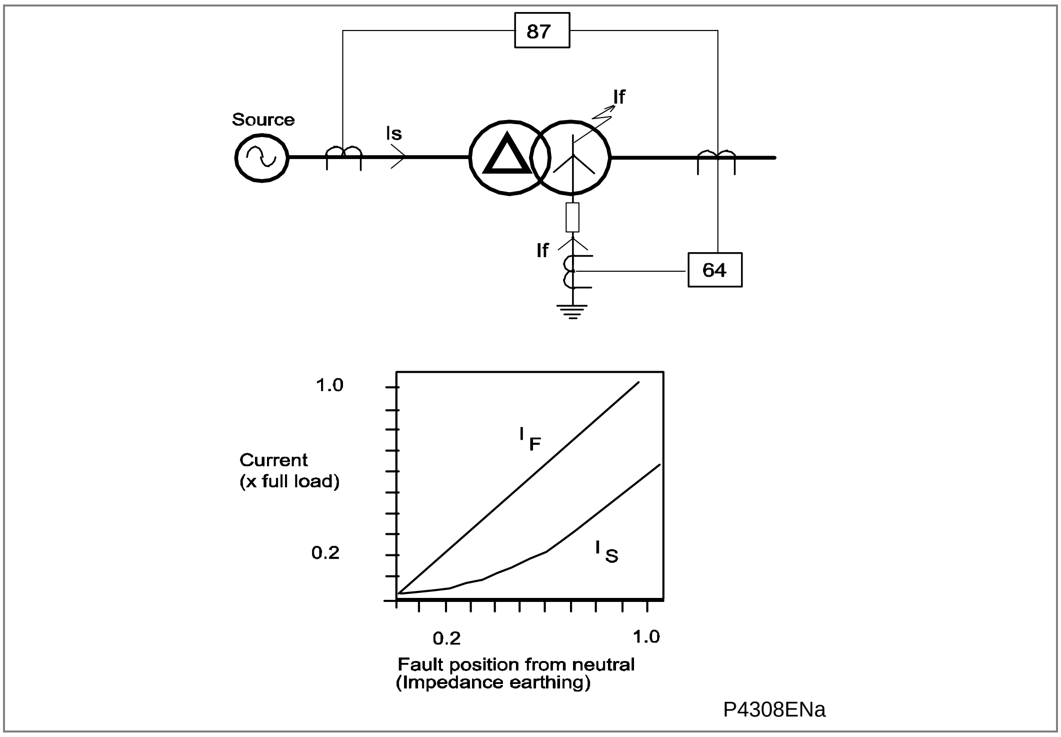

87
Source
Is
If
If
64
1.0
Current
(x full load)
0.2
I F
I S
0.2
1.0
Fault position from neutral
(Impedance earthing)
P4308ENa

Figure 46 - Fault limitation on an impedance earthed system

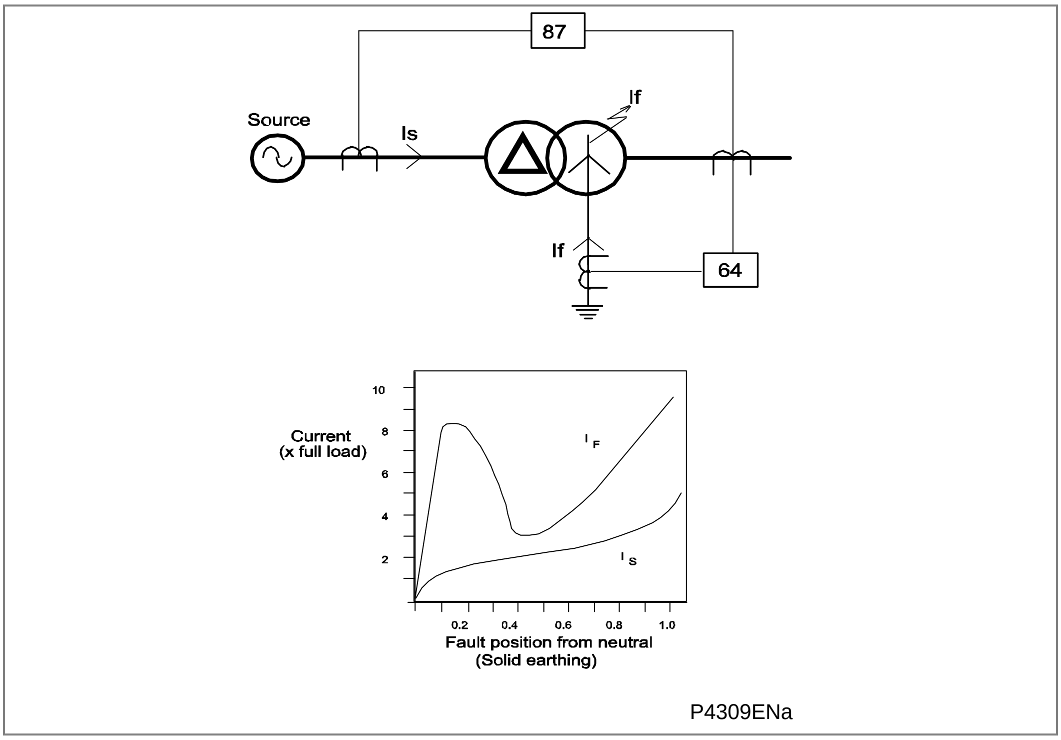

87
Source
Is
If
If
64
10
8
6
4
2
Current
(x full load)
I F
I S
0.2
0.4
0.6
0.8
1.0
Fault position from neutral
(Solid earthing)
P4309ENa

Figure 47 - Fault limitation on a solidly earthed system

If a fault on a solidly earthed star winding (Figure 47) is considered, the fault current is limited by the leakage reactance of the winding, any impedance in the fault path and by the fault point voltage. The value of fault current varies in a complex manner with fault location. As in the case of the impedance earthed transformer, the value of current available as an overall differential protection operating quantity is limited. More sensitive earth fault protection is provided by a restricted earth fault relay (64), which is arranged to measure If directly. Although more sensitive protection is provided by REF, the operating current for the overall differential protection is still significant for faults over most of the winding. For this reason, independent REF protection may not have previously been considered necessary for a solidly earthed winding, especially where an additional relay would have been required. With the P64x, the REF protection is available at no extra cost if a neutral CT is available.

Restricted earth fault protection is also commonly applied to Delta windings of large power transformers, to improve the operating speed and sensitivity of the protection package for winding earth faults. When applied to a Delta winding this protection is commonly referred to as “balanced earth fault protection”. It is inherently restricted in its zone of operation when it is stabilized for CT spill current during inrush or during phase faults. The value of the fault current flowing depends on system earthing arrangements and the fault point voltage.

2.3.2 Low Impedance REF Operating Mode

When applying differential protection such as REF, some suitable means must be used to give the protection stability under external fault conditions, ensuring that relay operation only occurs for faults on the transformer winding or connections. The P64x uses the bias technique which operates by measuring the level of through current flowing and altering the relay sensitivity accordingly. In addition, the P64x uses transient bias to improve the stability of REF during external faults.

Low impedance REF with a triple slope biased characteristic is provided in the P64x. One low impedance REF protection function is available for each transformer winding. It can also be used in 1.5 Bk and autotransformer applications. Low impedance REF is based on comparing the vector sum of phase currents of the transformer winding to the neutral point current measured directly.

The differential current and bias current are given by the following expression:

$$I_{REF,diff} = \left| \left(\overrightarrow{I_A} + \overrightarrow{I_B} + \overrightarrow{I_C} \right) \times \text{scalingfactor} + \overrightarrow{I_N} \right|$$

$$I_{REF,bias} = 0.5 \cdot \left[\left(\max \left[\left|\overrightarrow{I_A}\right|, \left|\overrightarrow{I_B}\right|, \left|\overrightarrow{I_C}\right| \right] \right) \times \text{scalingfactor} + \left|\overrightarrow{I_N}\right| \right]$$

The REF biased characteristic is as follows:

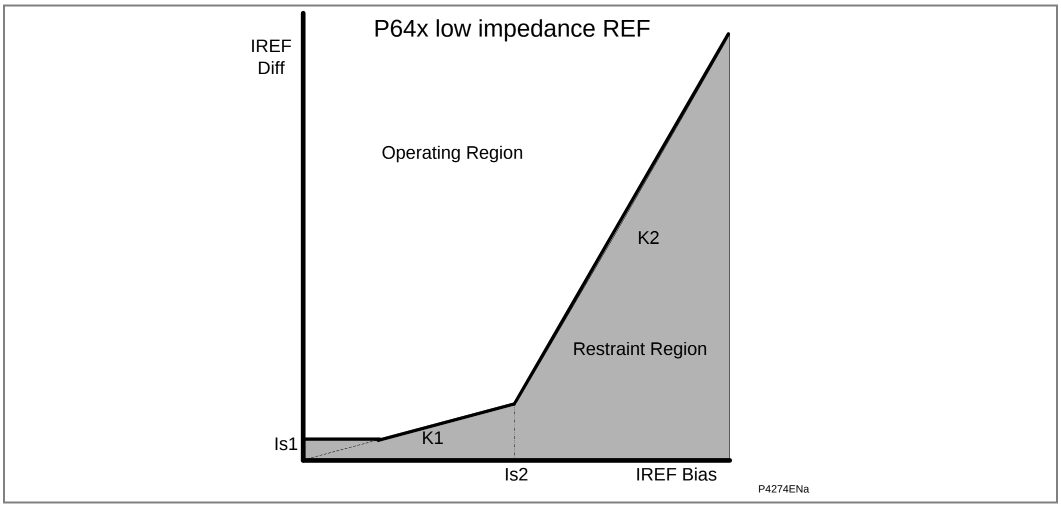


Figure 48 - P64x restricted earth fault biased characteristic

Low impedance biased REF settings are similar to those of the biased differential protection function. The low impedance REF is blocked by CTS.

2.3.3 Setting Guidelines for Low Impedance Biased REF Protection

Two bias settings are provided in the REF protection in the P64x. The IREF K1 level of bias is applied up to through currents of Is2 Set, which is normally set to the rated current of the transformer. IREF> K1 is normally set to 0% to give optimum sensitivity for internal faults. However, if any differential spill current is present under normal conditions due to CT mismatch, IREF K1 may be increased accordingly to compensate. Then a setting of 20% is recommended.

IREF> K2 bias is applied for through currents above Is2 Set and may typically be set to 150% to ensure adequate restraint for external faults.

The neutral current scaling factor which automatically compensates for differences between neutral and phase CT ratios relies on the relay having been programmed with the correct CT ratios. It must therefore be ensured that these CT ratios are entered into the relay, in the **CT RATIOS** menu, for the scheme to operate correctly.

Typical settings for Is1 Set according to ESI 48-3 1977 are 10-60% of the winding rated current when solidly earthed and 10-25% of the minimum earth fault current for a fault at the transformer terminals when resistance earthed.

Figure 49 shows the relay connections for the P64x relay applied for biased REF protection.

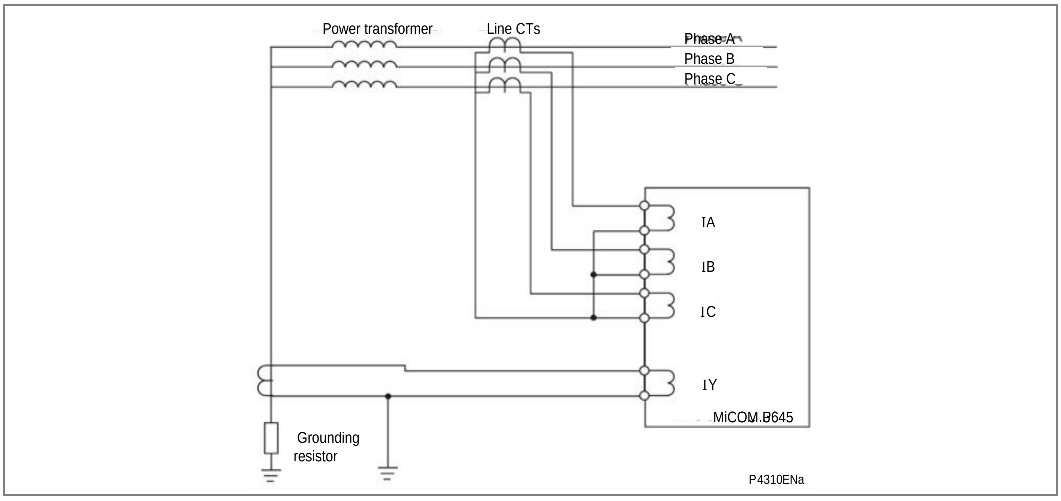
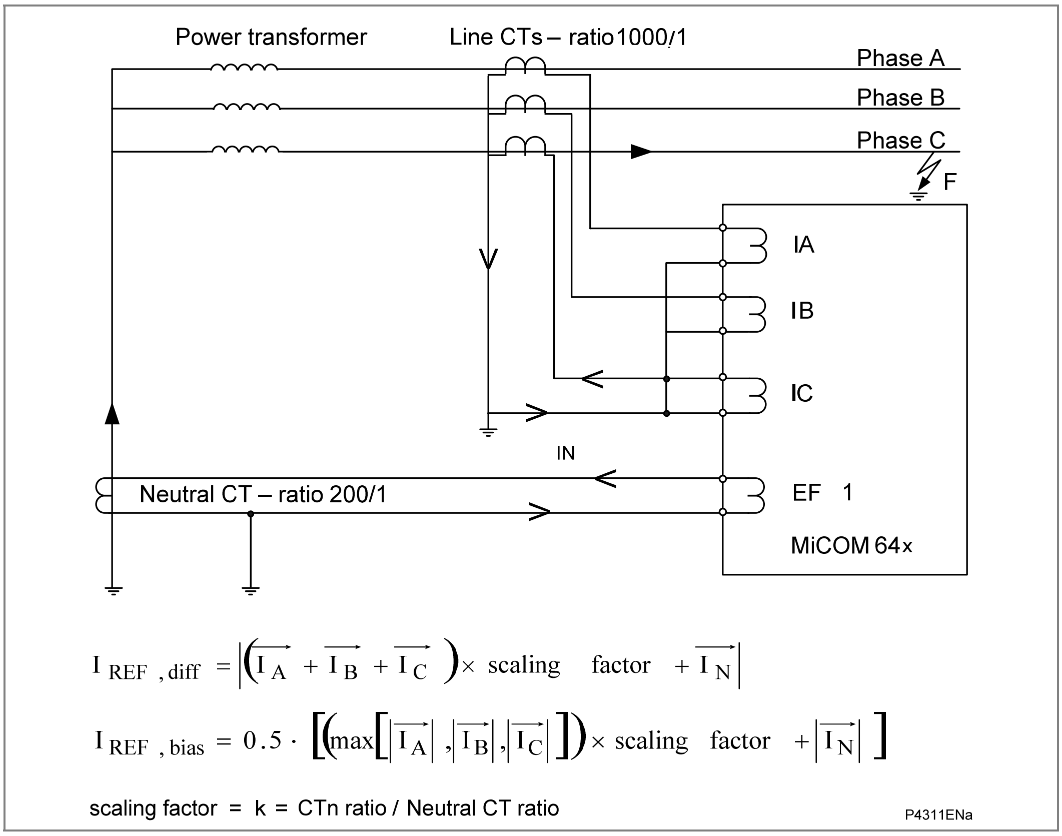


Figure 49 - P64x connections for biased REF protection

In Figure 49, the three line CTs are connected to the three phase CTs in the normal manner. The neutral CT is then connected to the Iy input. These currents are then used internally to derive both a bias and a differential current quantity for use by the low impedance REF protection. The actual operating characteristic of the element is shown in Figure 50. The advantage of this mode of connection is that the line and neutral CTs are not differentially connected so the neutral CT can also be used to drive the 51N protection to provide Standby Earth Fault Protection. Also, no external equipment such as stabilizing resistors or metrosils are required, as is the case with high impedance protection.

Where it is required that the neutral CT also drives the 51N protection element to provide standby earth fault protection, it may be a requirement that the neutral CT has a lower ratio than the line CTs to provide better earth fault sensitivity. If this was not accounted for in the REF protection, the neutral current value used would be incorrect. The relay automatically calculates the scaling factor that matches in amplitude the summation of line currents to the neutral current. This is shown in Figure 50.


Power transformer
Line CTs – ratio 1000/1
Phase A
Phase B
Phase C
F
IA
IB
IC
IN
Neutral CT – ratio 200/1
EF 1
MiCOM 64x
P4311ENa

$$I_{REF,diff} = \left| \left(\overrightarrow{I_A} + \overrightarrow{I_B} + \overrightarrow{I_C} \right) \times \text{scaling factor} + \overrightarrow{I_N} \right|$$

$$I_{REF,bias} = 0.5 \cdot \left[\left(\max\left[\left|\overrightarrow{I_A}\right|, \left|\overrightarrow{I_B}\right|, \left|\overrightarrow{I_C}\right| \right] \right) \times \text{scaling factor} + \left|\overrightarrow{I_N}\right| \right]$$

scaling factor = k = CTn ratio / Neutral CT ratio

Figure 50 - P64x REF scaling factor

Example 1: Consider a solidly earthed 90 MVA transformer which has a star winding protected by the REF function in the P64x. Consider 400:1 line CTs.

Is1 Set is set to 10% of the winding nominal current:

$$Is1\ \ Set = 0.1 \times \frac{90 \times 10^6}{\sqrt{3} \times 132 \times 10^3} = 39 A primary \ \frac{39}{400} = 0.98 A \sec ondary$$

Is2 is set to the rated current of the transformer:

$$Is2\ \ Set = \frac{90 \times 10^6}{\sqrt{3} \times 132 \times 10^3} = 390 A primary = \frac{390}{400} = 1 A \sec ondary$$

As recommended previously K1 may be set to 0% and K2 to 150%.

2.3.4 High Impedance REF Operating Mode

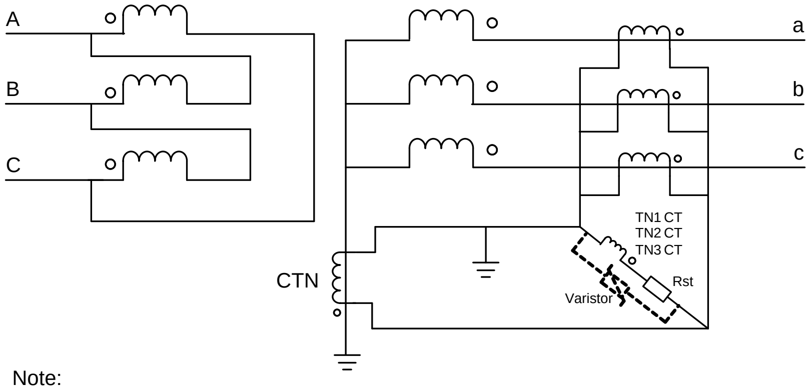
The restricted earth fault protection is a high impedance differential scheme which balances zero sequence current flowing in the transformer neutral against zero sequence current flowing in the transformer phase windings. Any unbalance for in-zone fault will result in an increasing voltage on the CT secondary and thus will activate the REF protection.

The high impedance differential technique ensures that the impedance of the circuit is sufficiently high such that the differential voltage that may occur under external fault conditions is lower than the voltage required to drive setting current through the relay. This ensures stability against external fault conditions and then the relay will operate only for faults occurring inside the protected zone.

This scheme is very sensitive and can then protect against low levels of fault current in resistance grounded systems where the earthing impedance and the fault voltage limit the fault current. In this application, the **HV/LV/TV/Auto Is1 Set** setting should be chosen to provide a primary operating current less than 10-25% of the minimum earth fault level.

This scheme can also be used in a solidly grounded system. It provides a more sensitive protection, even though the overall differential scheme provides a protection for faults over most of the windings. In this application, the **HV/LV/TV/Auto Is1 Set** setting should be chosen to provide a primary operating current between 10% and 60 % of the winding rated current.

Figure 51, Figure 52 and Figure 53 show how the P64x is used in REF, BEF and autotransformer REF applications.



Note:
CT1 and CTN must have the same CT ratio and similar magnetising characteristics

P4842ENa

Figure 51 - P64x high impedance REF of the grounded star winding of a power transformer

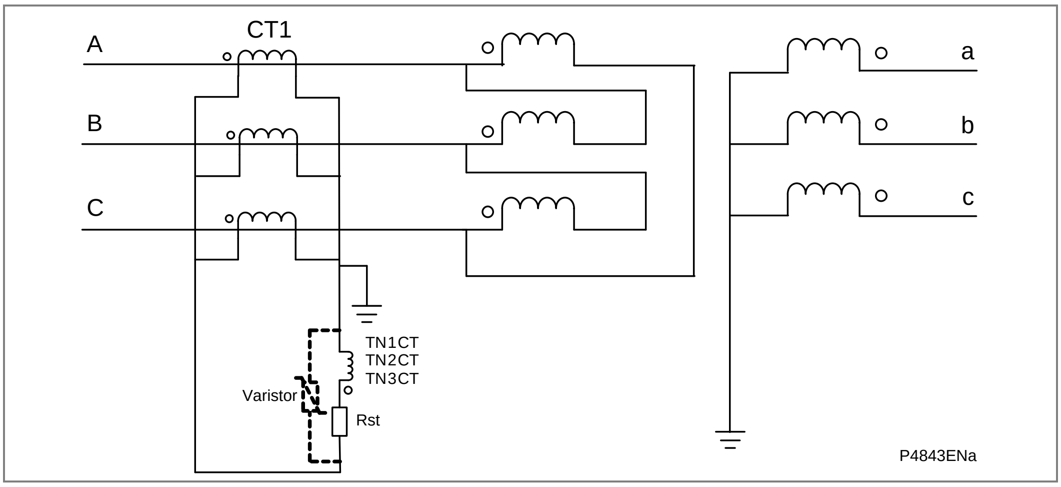
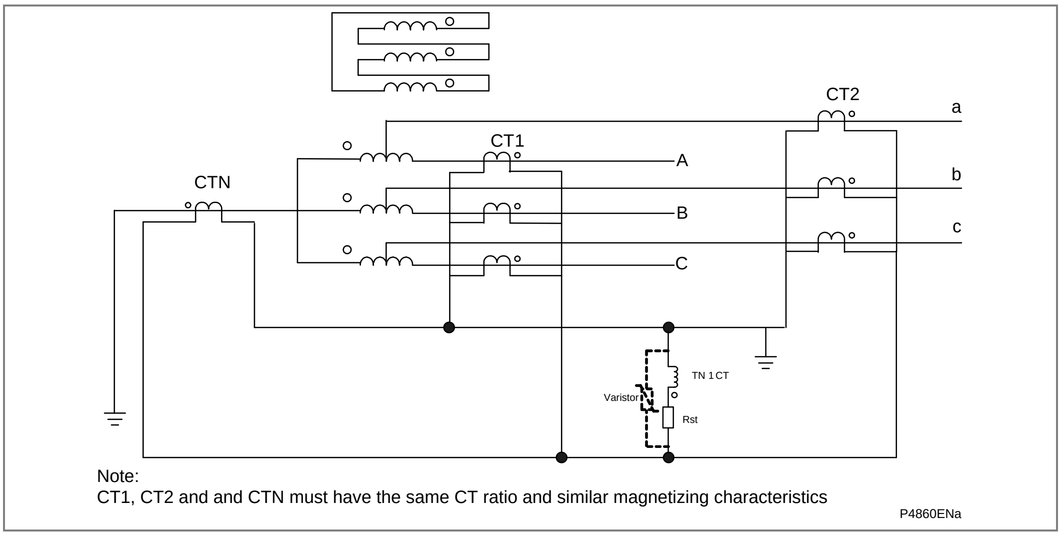

A
CT1
B
C
a
b
c
TN1CT
TN2CT
TN3CT
Varistor
Rst
P4843ENa

Figure 52 - P64x high impedance BEF of the delta winding of a power transformer with supply system earthed


CT2
a
CT1
A
CTN
b
B
c
C
TN 1CT
Varistor
Rst
P4860ENa

Note:
CT1, CT2 and and CTN must have the same CT ratio and similar magnetizing characteristics

Figure 53 - P64x Autotransformer high impedance REF

2.3.5 Setting Guidelines for High Impedance REF Protection

Figure 54 shows the application of a high impedance REF to protect the LV winding of a power transformer.

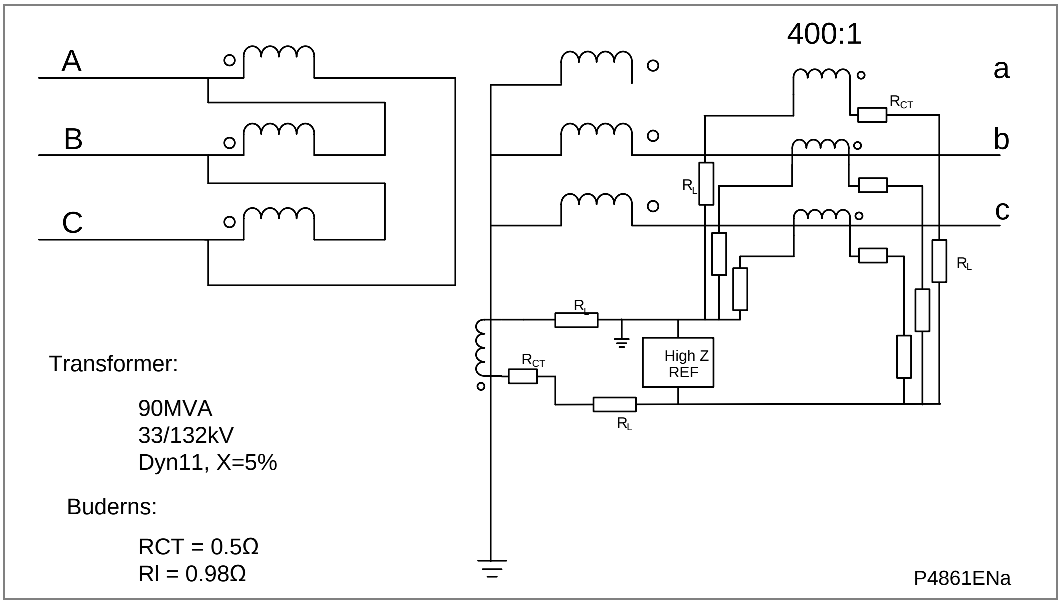

400:1
A
B
C
a
b
c
R_CT
R_L
R_L
R_CT
R_L
R_L
High Z REF
Transformer:
90MVA
33/132kV
Dyn11, X=5%
Buderns:
RCT = 0.5Ω
Rl = 0.98Ω
P4861ENa

Figure 54 - Restricted earth fault protection on a transformer

2.3.5.1 Stability Voltage Calculation

The transformer full load current, I_{FLC}, is:

$$I_{FLC} = \frac{90 \times 10^6}{132 \times 10^3 \times \sqrt{3}}$$
$$= 394A$$

To calculate the stability voltage the maximum through fault level should be considered. The maximum through fault level, ignoring the source impedance, I_F, is:

$$I_F = \frac{I_{FLC}}{X_{TX}}$$
$$= \frac{394A}{0.05} = 7873A$$

Required relay stability voltage, V_S, and assuming one CT saturated is:

$$V_S = KI_F\left(R_{CT} + 2R_L\right)$$

The graphic shown in Figure 55 should be used to determine the K factor and the operating time.

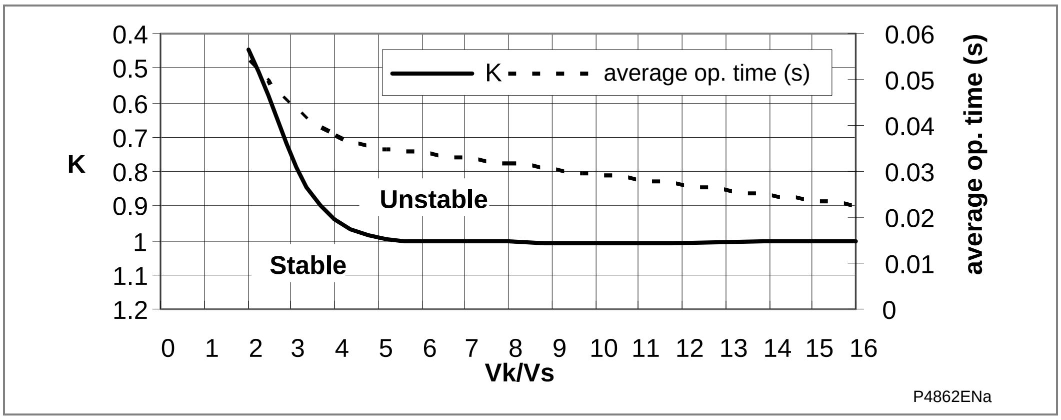


Figure 55 - Variation of K and the average operating time as a function of Vk/Vs – REF applications

Consider that an average operating time of 40 ms is appropriate. The corresponding Vk/Vs of approximately 4 can then be obtained from the graph of Figure 55 and subsequently an approximate K value of 0.94, for stable operation, can be obtained from the same graph.

$$
\begin{aligned}
V_S &= KI_F\left(R_{CT} + 2R_L\right) \\
&= 0.94 \times 7873x\frac{1}{400}\left(0.5 + 2 \times 0.98\right) \\
&= \mathbf{45.5V}
\end{aligned}
$$

The CTs knee point voltage should be at least 4 times Vs so that an average operating time of 40 ms is achieved.

2.3.5.2 Primary Operating Current Calculation

The primary operating current should be between 10 and 60 % of the winding rated current. Assuming that the relay effective setting or primary operating current is approximately 30% of the full load current, the calculation below shows that a setting of less than 0.3A is required on the relay.

$$
\begin{aligned}
\text{relay effective setting} &= 0.3 \times \frac{I_{FLC}}{\text{CT ratio}} \\
&= 0.3 \times \frac{394A}{400} = 0.3A
\end{aligned}
$$

2.3.5.3 Stabilising Resistor Calculation

Assuming that a setting of 0.1A is selected the value of the stabilizing resistor, R_{ST}, required is:

$$R_{ST} = \frac{V_S}{\text{HV Is1 Set}} = \frac{45.5}{0.1} = 455\Omega$$

To achieve an average operating time of 40 ms, Vk/Vs should be 4 as indicated in Figure 55.

$$
\begin{aligned}
\text{Kneepoint Voltage}, V_K &= 4V_S \\
&= 4 \times 45.5 \\
&= 182V
\end{aligned}
$$

If the actual Vk is greater than 4 times Vs, then the K factor increases. In this case, Vs should be recalculated considering the new K factor and using equation $V_S = KI_F\left(R_{CT} + 2R_L\right)$. Note that K can reach a maximum value of 1 approximately.

2.3.5.4 Current Transformers

The effective relay setting or primary operating current is $I_P = N \times \left(I_S + nI_e\right)$. By re-arranging this equation, the excitation current for each of the current transformers at the relay stability voltage can be calculated:

$$\text{CT Magnetising current at stability voltage, } I_e \le \frac{\frac{I_P}{N} - I_S}{n}$$

$$\le \frac{0.3 - 0.1}{4}$$

$$\le 0.05\text{A}$$

In summary, the current transformers used for this application must have a kneepoint voltage of 182 V or higher (note that maximum Vk/Vs that may be considered is 16 and the maximum K factor is 1), with a secondary winding resistance of 0.5 Ω or lower and a magnetizing current at 45.5 V of less than 0.05 A.

2.3.5.5 Non-Linear Resistors

If the peak voltage developed across the relay circuit under maximum internal fault conditions exceeds 3000 V peak then a suitable non-linear resistor should be connected across the relay and stabilizing resistor, in order to protect the insulation of the CTs, relay and interconnecting leads. To calculate the maximum fault voltage assuming no CT saturation, use the following equation:

$$V_F = I'_F\left(R_{CT} + 2R_L + R_{ST} + R_r\right)$$

$$= 7873\text{x}\frac{1}{400}\left(0.5 + 2 \times 0.98 + 455\right)$$

$$= 9004\text{V}$$

Assuming a CT kneepoint voltage of 200 V, the peak voltage can be estimated as:

$$V_P = 2\sqrt{2V_K\left(V_F - V_K\right)}$$

$$= 2\sqrt{2\text{x}200(9004 - 200)}$$

$$= 3753\text{V}$$

This value is above the peak voltage of 3000 V and therefore a non-linear resistor is required.

Note	*The kneepoint voltage value used in the above formula should be the actual voltage obtained from the CT magnetizing characteristic and not a calculated value.*

One stabilizing resistor, Schneider Electric part No. ZB9016 756, and one varistor, Schneider Electric part No. 600A/S1/S256 might be used.

2.4 Overfluxing Protection and Blocking

2.4.1 Basic Principles

Overfluxing or overexcitation of a transformer connected to the terminals of a generator, can occur if the ratio of voltage to frequency exceeds certain limits. High voltage or low frequency, causing a rise in the V/f ratio, will produce high flux densities in the magnetic core of the transformer. This could cause the core of the transformer to saturate and stray flux to be induced in unlaminated components that have not been designed to carry flux. The resulting eddy currents in solid components (core bolts and clamps) and end of core laminations can cause rapid overheating and damage.

The P64x relays provide a four stage overfluxing element. One stage can be set to operate with a definite time or inverse time delay (IDMT), this stage can be used to provide the protection trip output. There are also three other definite time stages which can be combined with the inverse time characteristic to create a combined multi-stage V/Hz trip operating characteristic using PSL. An inhibit signal is provided for the V/Hz>1 stage 1 only, which has the inverse time characteristic option. This allows a definite time stage to override a section of the inverse time characteristic if required. The inhibit has the effect of resetting the timer, the start signal and the trip signal. There is also one definite time alarm stage that can be used to indicate unhealthy conditions before damage has occurred to the machine.

The P64x relay offers an overfluxing protection element which can be used to raise an alarm or initiate tripping in the event of prolonged periods of transformer overfluxing. In addition, a differential current 5th harmonic blocking feature is also provided within the P64x, which can be used to prevent possible maloperation of the differential element under transient overfluxing conditions.

To make use of the time delayed overfluxing protection, the P64x relay must be supplied with a voltage signal which is representative of the primary system voltage on the source side of the transformer. The 5th harmonic blocking feature does not require a voltage signal. A 5th harmonic signal is derived from the differential current wave form on each phase and blocking of the low set biased characteristic is on a per phase basis.

2.4.2 Transformer Overfluxing

Transformer overfluxing might arise for the following reasons:

- High system voltage
- Generator full load rejection
- Ferranti effect with light loading transmission lines
- Low system frequency
- Generator excitation at low speed with AVR in service
- Geomagnetic disturbance
- Low frequency earth current circulation through a transmission system

The initial effects of overfluxing will be to increase the magnetizing current for a transformer. This current will be seen as a differential current. If it reaches a high level there would be a risk of differential protection tripping.

Persistent overfluxing may result in thermal damage or degradation of a transformer as a result of heating caused by eddy currents that may be induced in non-laminated metalwork of a transformer. The flux levels in such regions would normally be low, but excessive flux may be passed during overfluxed operation of a transformer.

The following protection strategy is proposed to address potential overfluxing conditions:

- Maintain protection stability during transient overfluxing
- Ensure tripping for persistent overfluxing

In most applications, the recommended minimum differential trip threshold for P64x, its filtering action and possible operation of the inrush detector will ensure stability of the differential element. If more difficult situations exist, the P64x relay is offered with a 5th harmonic differential current blocking facility. This facility could be applied with some study of the particular problem.

To ensure tripping for persistent overfluxing, due to high system voltage or low system frequency, the P64x is provided with time delayed Volts per Hertz protection. Where there is any risk of persistent geomagnetic overfluxing, with normal system voltage and frequency, the 5th harmonic differential current facility could be used to initiate tripping after a long time delay. This time delay would need to be programmed in the PSL as shown in Figure 56.

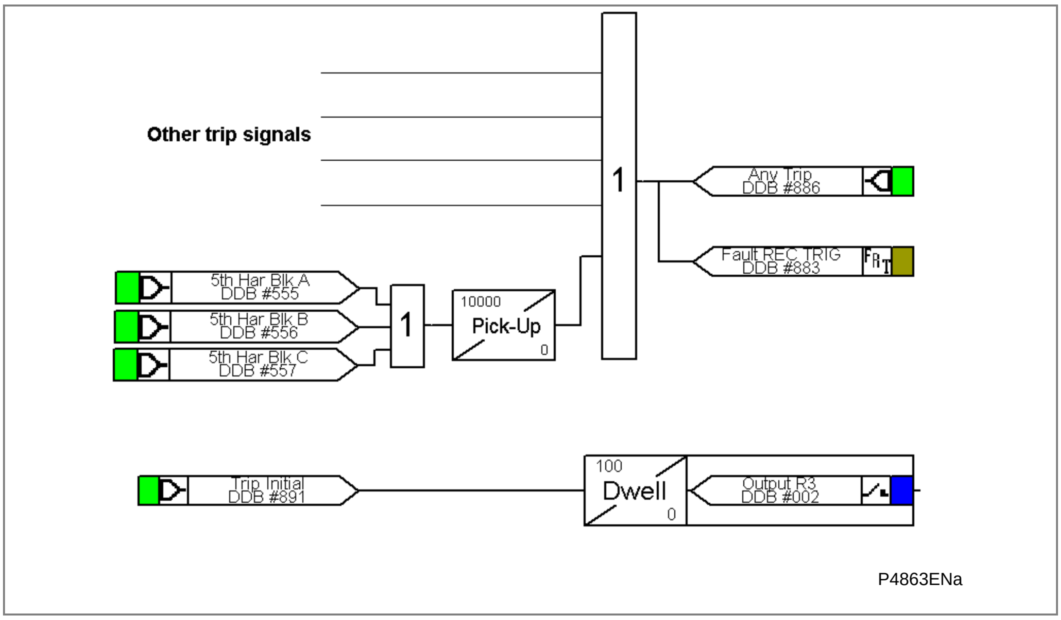


Figure 56 - Fifth harmonic tripping

2.4.3 Time Delayed Overfluxing Protection

Two overfluxing elements for HV and LV transformer sides are provided in the P643 and P645. One overfluxing element is available in the P642.

The following functions are provided:

- Alarm stage with definite time delay
- Trip stage V/Hz>1 with DT or IDMT time delay
- Trip stage V/Hz>2/3/4 with DT delay

The settings of the alarm stage should be such that the alarm signal can be used to prompt automatic or manual corrective action.

Protection against damage due to prolonged overfluxing is offered by a V/f protection element with a variable time tripping characteristic. The setting flexibility of this element, by adjustment of the time delay at various V/f values, makes it suitable for various applications. The manufacturer of the transformer or generator should be able to supply information about the short-time over-excitation capabilities, which can be used to determine appropriate settings for the V/f tripping element. The variable time overfluxing protection would be used to trip the transformer directly.

If preferred, the V/f tripping element can be set with a definite time characteristic.

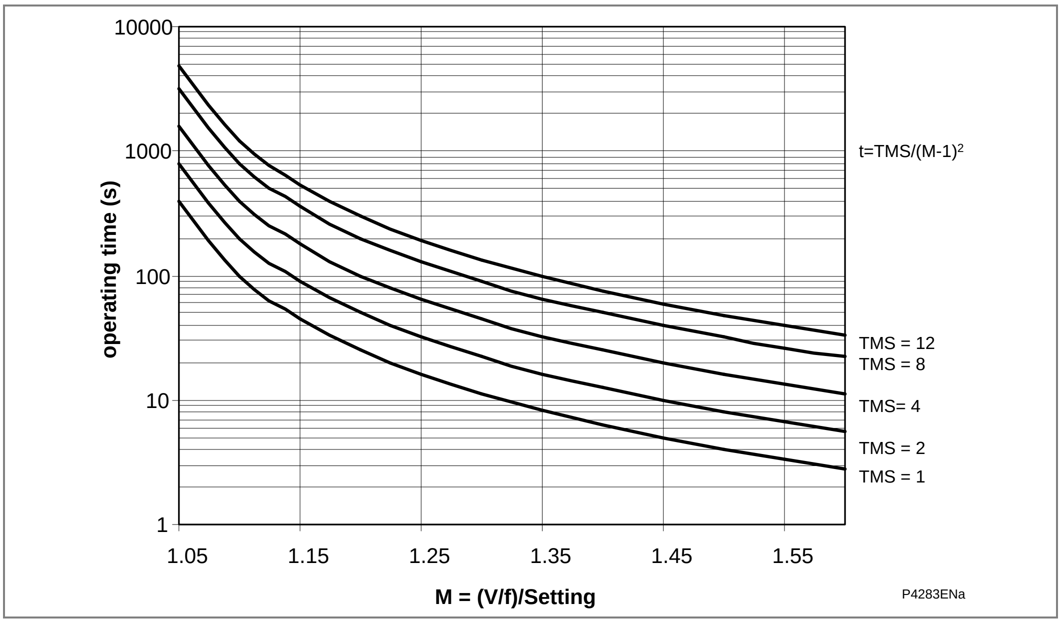


Figure 57 - Variable time overfluxing protection characteristic

2.4.4 Setting Guidelines for Overfluxing Protection

The V/Hz>1 overfluxing protection element trip stage can be selected by setting the V/Hz Trip Func cell to the required time delay characteristic: DT for definite time operation, IDMT, for inverse time operation. In the **V/Hz>x Status** cells, the four overfluxing protection trip stages can be set to **Enable** or **Disable**.

In the **V/Hz Alarm Status** cell, the overfluxing protection alarm stage can be set to **Enable** or **Disable**.

The pick up for the overfluxing elements depends on the nominal core flux density levels. Generator transformers are generally run at higher flux densities than transmission and distribution transformers, so they require a pick up setting and shorter tripping times which reflect this. Transmission transformers can also be at risk from overfluxing conditions and withstand levels should be consulted when deciding on the required settings.

IEEE Standard C37.91-2000 states that overexcitation of a transformer can occur whenever the ratio of the per unit voltage to per unit frequency (V/Hz) at the secondary terminals of a transformer exceeds its rating of 1.05 per unit (PU) on transformer base at full load, 0.8 power factor, or 1.1 PU at no load. Refer to subclause 4.1.6 in IEEE Std C57.12.00-2006 for further discussion on the capability of a transformer to operate above rated voltage and below rated frequency.

The element is set in terms of the actual ratio of voltage to frequency; the overfluxing threshold setting, **V/Hz>x Trip Set**, can therefore be calculated as shown below:

A 1.05 p.u. setting = 110/50 x 1.05 = 2.31

Where:

- The VT secondary voltage at rated primary volts is 110 V
- The rated frequency is 50 Hz

The overfluxing alarm stage threshold setting, **V/Hz Alarm Set**, shall be set lower than the trip stage setting to provide an indication that abnormal conditions are present and to alert an operator to adjust system parameters accordingly.

The time delay settings should be chosen to match the withstand characteristics of the protected transformer. If an inverse time characteristic is selected, select the time multiplier setting, **V/Hz>1 Trip TMS** so the operating characteristic closely matches the withstand characteristic of transformer. If a definite time setting is chosen for the trip stages the time delay is set in the **V/Hz>x Trip Delay** cells. The alarm stage time delay is set in the **V/Hz Alarm Delay** cell.

The three definite time stages and one DT/IDMT stage can be combined to create a combined multi-stage V/Hz trip operating characteristic using PSL, see Figure 58 and Figure 59.

Reference should be made to manufacturers' withstand characteristics before formulating these settings.

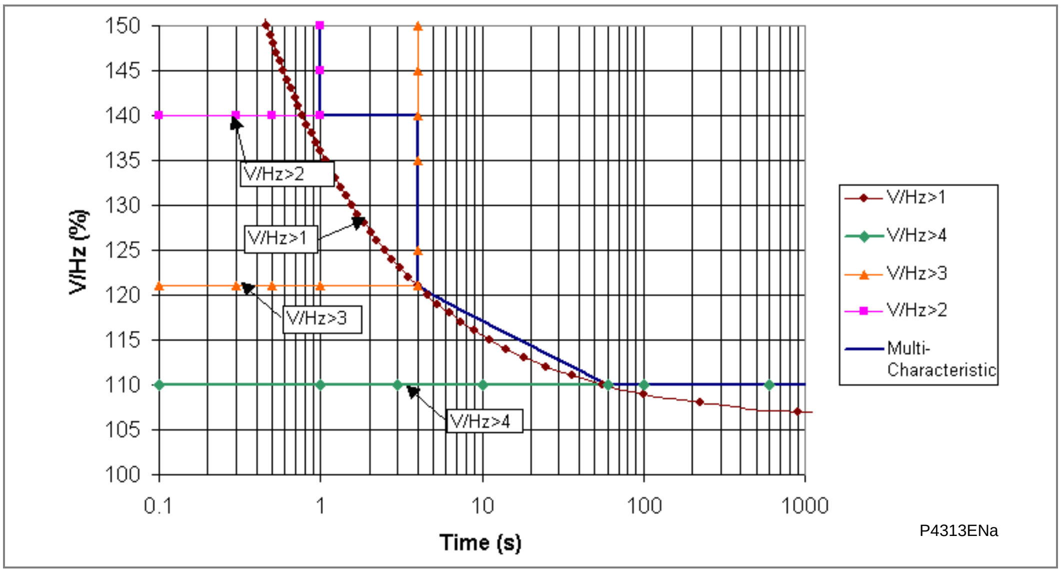


Figure 58 - Multi-stage overfluxing characteristic

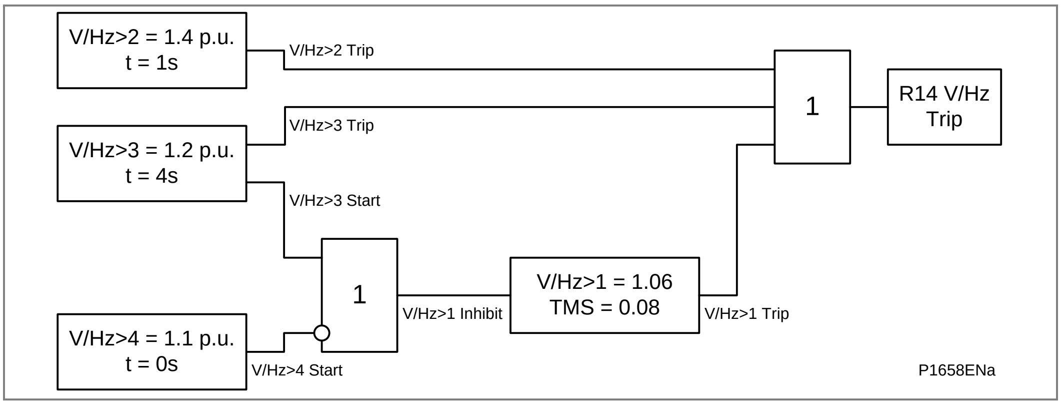


Figure 59 - Scheme logic for multi-stage overfluxing characteristic

2.4.5 5th Harmonic Blocking

The 5th Harmonic blocking feature is available for possible use to prevent unwanted operation of the low set differential element under transient overfluxing conditions.

When overfluxing occurs, the transformer core becomes partially saturated and the resultant magnetizing current waveforms increase in magnitude and become harmonically distorted. Such waveforms have a significant 5th harmonic content, which can be extracted and used as a means of identifying the abnormal operating condition.

The 5th harmonic blocking threshold is adjustable between 0 - 100% differential current. The threshold should be adjusted so that blocking will be effective when the magnetizing current rises above the chosen threshold setting of the low-set differential protection.

For example, when a load is suddenly disconnected from a power transformer the voltage at the input terminals of the transformer may rise by 10-20% of the rated value. Since the voltage increases, the flux, which is the integral of the excitation voltage, also increases. As a result, the transformer steady state excitation current becomes higher. The resulting excitation current flows in one winding only and therefore appears as differential current which may rise to a value high enough to operate the differential protection. A typical differential current waveform during such a condition is shown in Figure 60. A typical setting for **Ih(5)%>** is 35%

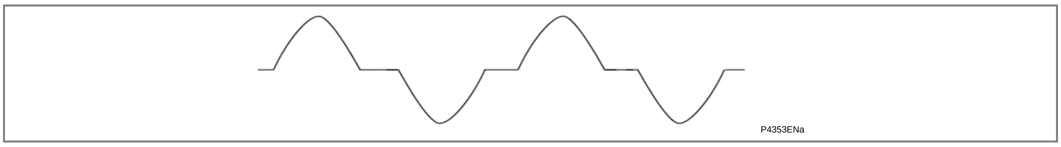


Figure 60 - Typical overflux current waveform

To offer some protection against damage due to persistent overfluxing that might be caused by a geomagnetic disturbance, the 5th harmonic blocking element can be routed to an output contact using an associated timer. Operation of this element could be used to give an alarm to the network control centre. If such alarms are received from a number of transformers, they could serve as a warning of geomagnetic disturbance so that operators could take some action to safeguard the power system. Alternatively this element can be used to initiate tripping in the event of prolonged pick up of a 5th harmonic measuring element. It is not expected that this type of overfluxing condition would be detected by the AC overfluxing protection. This form of time delayed tripping should only be applied in regions where geomagnetic disturbances are a known problem and only after proper evaluation through simulation testing.

2.5 Phase Fault Overcurrent Protection (50/51)

A fault external to a transformer can result in damage to the transformer. If the fault is not cleared promptly, the resulting overload on the transformer can cause severe overheating and failure. Overcurrent relays may be used to clear the transformer from the faulted bus or line before the transformer is damaged. Overcurrent relays are often the only form of protection applied to small transformers. They are used for backup protection for larger transformers and both instantaneous and time delayed overcurrent can be applied.

The overcurrent inverse time characteristic on the HV side of the transformer must grade with the overcurrent inverse time characteristic on the LV side which in turn must grade with the LV outgoing circuits. The overcurrent function provides limited protection for internal transformer faults because sensitive settings and fast operation times are usually not possible. Sensitive settings are not possible because the pickup should allow overloading of the transformer when required. Fast operating times are not possible because of the grading required with respect to downstream overcurrent relays. To allow fast operating times, phase instantaneous overcurrent functions with low transient overreach are required.

The pickup of the time delayed overcurrent element can be set to 125-150% of the maximum MVA rating to allow overloading of the transformer according to IEEE Std. C37.91-2000.

As recommended by IEEE Std. C37.91-2000, the instantaneous overcurrent element should be set to pick up at a value higher than the maximum asymmetrical through fault current. This is usually the fault current through the transformer for a low-side three-phase fault. For instantaneous elements subject to transient overreach, a pickup of 175% (variations in settings of 125–200% are common) of the calculated maximum low-side three-phase symmetrical fault current generally provides sufficient margin to avoid false tripping for a low-side bus fault, while still providing protection for severe internal faults. Due to low transient overreach of the third and fourth overcurrent stages in the P64x, the instantaneous overcurrent element may be set to 120-130% of the through fault level of the transformer ensuring that the relay is stable for through faults. The instantaneous pickup setting should also consider the effects of transformer magnetizing inrush current.

Under fault conditions, currents are distributed in different ways according to winding connections. It is important to understand the fault current distribution under faults to set the overcurrent element. The following diagrams show various current distributions.

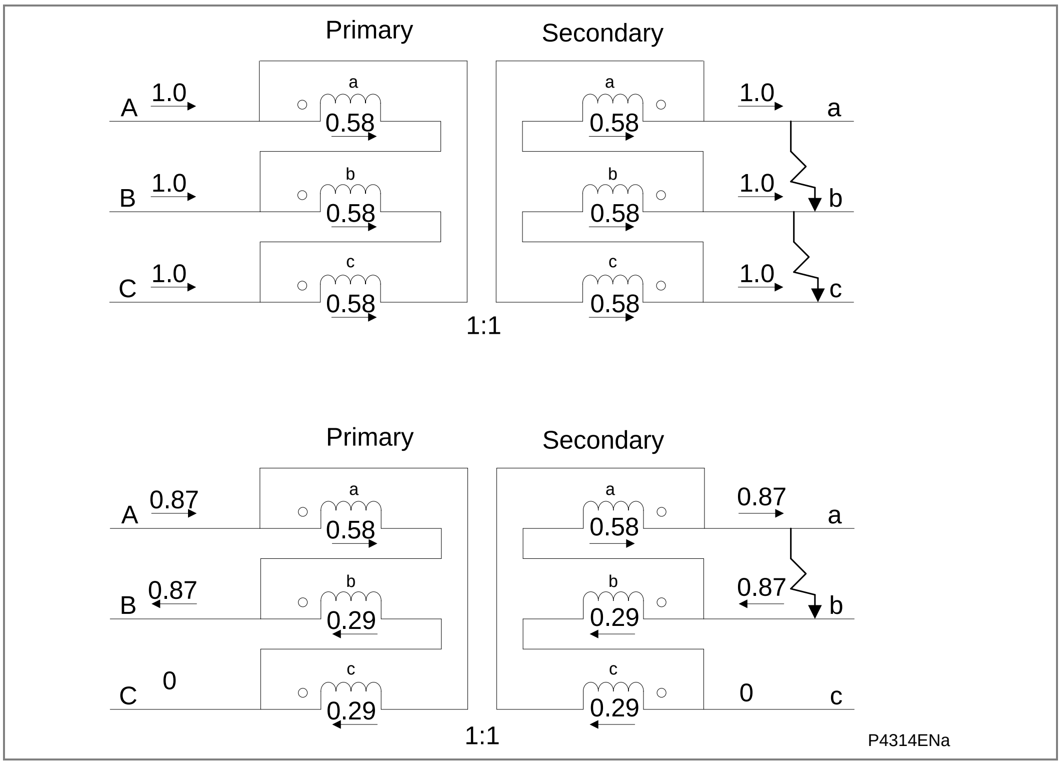


Figure 61 - Current distribution for Δ-Δ connected transformers

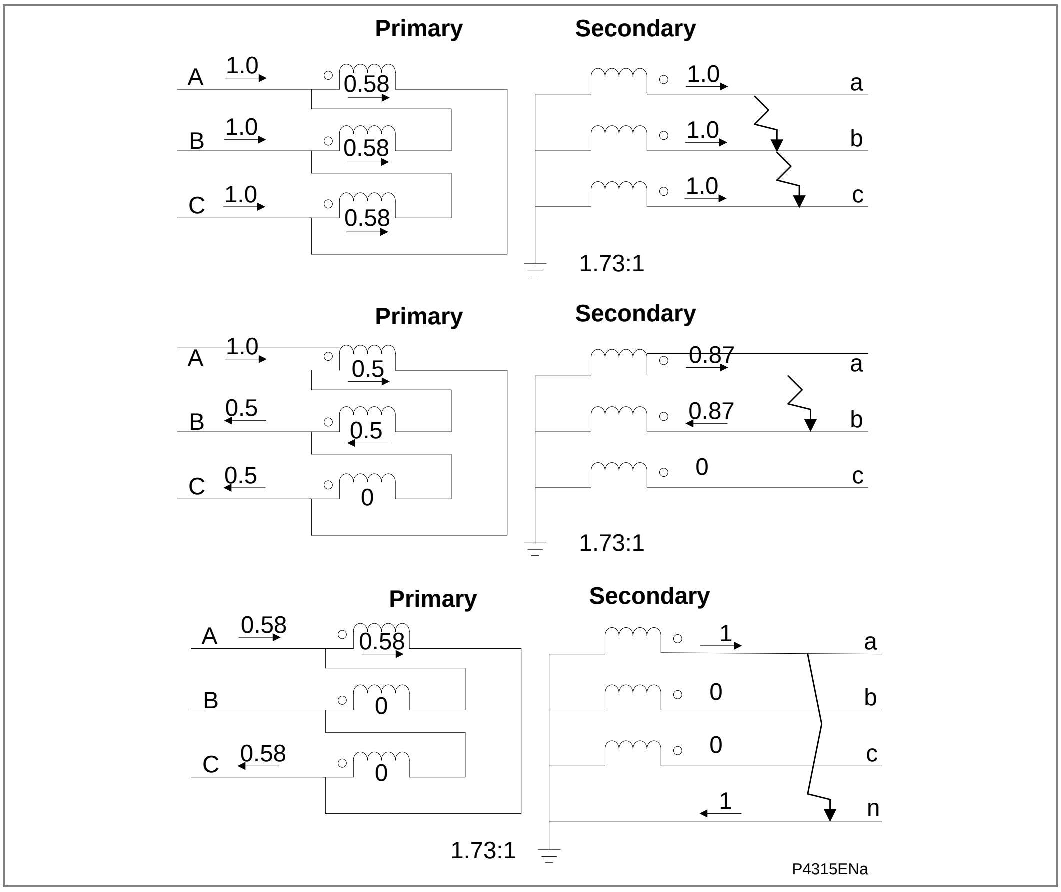

Primary
Secondary
A
B
C
1.0
0.58
a
b
c
1.73:1
0.5
0.87
0
0.58
1
n
P4315ENa

Figure 62 - Current distribution for Δ-Y connected transformers

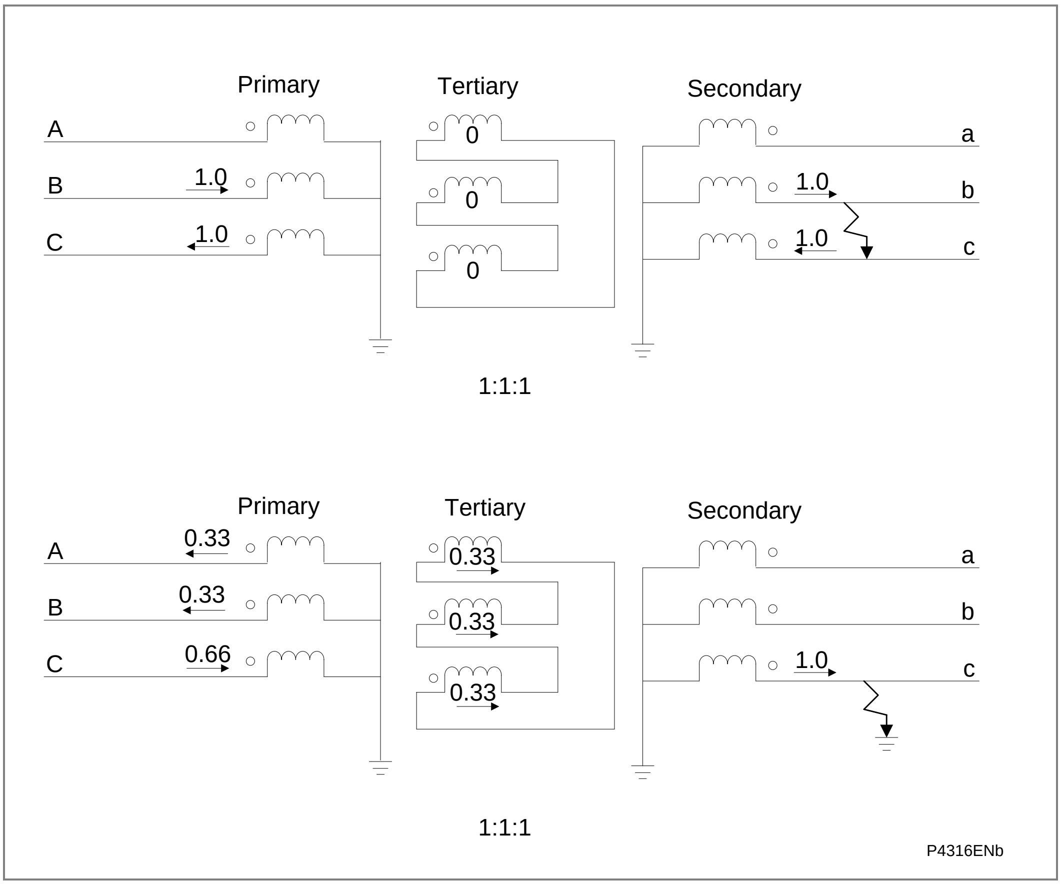


Figure 63 - Current distribution for Y-Δ-Y connected transformers

Transformers are mechanically and thermally limited in their ability to withstand short-circuit current for finite periods of time. For proper backup protection, the relays should operate before the transformer is damaged by an external fault. In setting transformer overcurrent relays, the short-time overload capability of the transformer in question should not be exceeded. Low values of 3.5 or less times normal base current may result from overloading rather than faults. Also the overcurrent characteristic should always be below the transformer damage curve.

A four-stage directional/non-directional overcurrent element is provided in the P643 and P645 relays, and a four-stage non-directional element is provided in the P642. This element can be used to provide time-delayed backup protection for the system and instantaneous protection providing fast operation for transformer faults.

The first two stages have a time delayed characteristic that can be set as either Inverse Definite Minimum Time (IDMT) or Definite Time (DT). The third and fourth stages have a definite time delay, which can be set to zero to produce instantaneous operation. Each stage can be selectively enabled or disabled.

In summary, there are a few application considerations to make when applying overcurrent relays to protect a transformer:

- When applying overcurrent protection to the HV side of a power transformer it is usual to apply a high set instantaneous overcurrent element in addition to the time delayed low-set, to reduce fault clearance times for HV fault conditions. Typically, this will be set to approximately 1.3 times the LV fault level, so that it will only operate for HV faults. A 30% safety margin is sufficient due to the low transient overreach of the third and fourth overcurrent stages. Transient overreach defines the response of a relay to DC components of fault current and is quoted as a percentage. A relay with a low transient overreach will be largely insensitive to a DC offset and may therefore be set more closely to the steady state AC waveform.

- The second requirement for this element is that it should remain inoperative during transformer energization, when a large primary current flows for a transient period. In most applications, the requirement to set the relay above the LV fault level will automatically result in settings that will be above the level of magnetizing inrush current.

All four overcurrent stages operate on the Fourier fundamental component. Therefore, for the third and fourth overcurrent stages in P64x relays, it is possible to apply settings corresponding to 40% of the peak inrush current while maintaining stability for the condition.

Where an instantaneous element is required to accompany the time delayed protection, as described above, the third or fourth overcurrent stage of the P64x relay should be used, as they have wider setting ranges.

2.5.1 Application of Timer Hold Facility

This feature may be useful in certain applications, for example when grading with electromechanical overcurrent relays which have inherent reset time delays. Setting of the hold timer to a value other than zero, delays the resetting of the protection element timers for this period therefore allowing the element to behave similarly to an electromechanical relay.

Another situation where the timer hold facility may be used to reduce fault clearance times is where intermittent faults may be experienced. An example of this may occur in a PVC insulated cable. In this application the fault energy can melt and reseal the cable insulation, extinguishing the fault.

When the reset time of the overcurrent relay is instantaneous, the relay will be repeatedly reset and not be able to trip until the fault becomes permanent. By using the timer hold facility the relay will integrate the fault current pulses, reducing fault clearance time.

The timer hold facility for the first and second overcurrent stages is settings **I>1 tReset** and I**>2 tReset**, respectively. This cell is not visible for the IEEE/US curves if an inverse time reset characteristic has been selected, as the reset time is then determined by the programmed time dial setting.

2.5.2 Setting Guidelines for Overcurrent Protection

The first or second stage of overcurrent protection can be selected by setting **I>1 Status** or **I>2 Status** to any of the inverse or DT settings. The first or second stage are disabled if **I>1 Status** or **I>2 Status** are set to **Disabled**.

The first or second stage can provide backup protection for faults on the transformer and the system. It should be coordinated with downstream protection to provide discrimination for system faults, setting the current threshold **I>1/2 Current Set** and the time delay.

I>1 TMS	For IEC curves;
I>1 Time Dial	For US/IEEE curves;
I>1 Time Delay	For definite time accordingly.

The third and fourth stages of overcurrent protection can be enabled by setting **I>3 Status** or **I>4 Status** to **DT**, providing a definite time operating characteristic. The third and fourth stages are disabled if **I>3 Status** or **I>4 Status** are set to **Disabled**. The third or fourth stage can be set as an instantaneous overcurrent protection, providing protection against internal faults on the transformer. The overcurrent function has low transient overreach. It should be set to 120-130% of the through fault level of the transformer to ensure stability for through faults. Care must also be taken to ensure that it does not operate under magnetizing inrush conditions.

The directionality of the overcurrent element can be chosen by setting **I>1/2/3/4 Direction**.

2.5.3 Setting Guidelines for Voltage Controlled Overcurrent Protection

Two voltage controlled overcurrent elements are available. They can be set as directional or non directional and definite time or inverse time. The voltage controlled overcurrent element threshold is reduced when the voltage is below a settable undervoltage threshold. **VCO>1 Curr' Set** and **VCO>1 K Setting** are set on the basis of the minimum fault-current condition independent of any load current requirements. This element is controlled by an undervoltage threshold, **VCO>1 V<Setting**. The undervoltage threshold is set below the normal minimum system load voltage, but above the maximum expected fault voltage. As a result, sensitive phase fault protection is provided with no risk of tripping due to load current.

2.6 Directional Phase Fault Overcurrent Protection (67)

If fault current can flow in both directions through a relay location, it is necessary to add directionality to the overcurrent relays to obtain correct co-ordination. Typical systems which require such protection are parallel feeders (both plain and transformer) and ring main systems, each of which are relatively common in distribution networks.

To give directionality to an overcurrent relay, it is necessary to provide it with a suitable reference, or polarizing, signal. The reference generally used is the system voltage, as its angle remains relatively constant under fault conditions. The phase fault elements of the P64x relays are internally polarized by the quadrature phase-phase voltages, as shown in the following table.

Phase of protection	Operating current	Polarizing voltage
A Phase	IA	VBC
B Phase	IB	VCA
C Phase	IC	VAB

Table 6 - Phase of protection, operating currents and polarizing voltages

It is therefore important to ensure the correct phasing of all current and voltage inputs to the relay, in line with the supplied application diagram.

Under system fault conditions, the fault current vector will lag its nominal phase voltage by an angle dependent on the system X/R ratio. It is therefore a requirement that the relay operates with maximum sensitivity for currents lying in this region. This is achieved using the relay characteristic angle (RCA) setting; this defines the angle by which the current applied to the relay must be displaced from the voltage applied to the relay to obtain maximum relay sensitivity. This is set in cell **I>Char Angle** in the **OVERCURRENT 1** menu.

A common application which requires the use of directional relays is considered below.

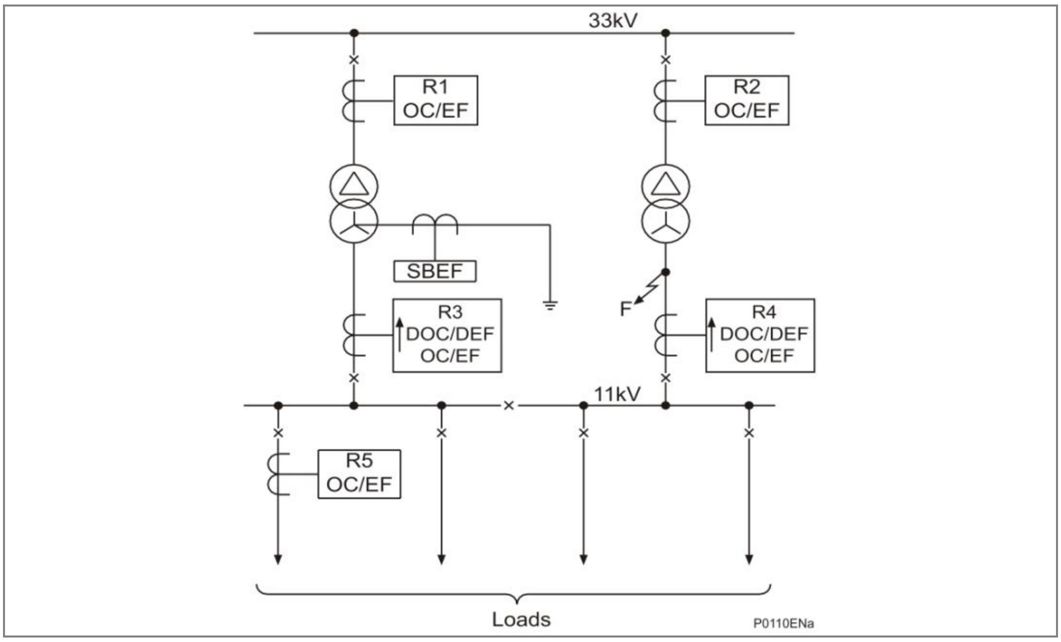


Figure 64 - Typical distribution system using parallel transformers

Figure 64 shows a typical distribution system using parallel power transformers. In such an application, a fault at 'F' could result in the operation of both R3 and R4 relays and the subsequent loss of supply to the 11 kV busbar. Therefore with this system configuration it is necessary to apply directional relays at these locations set to look into their respective transformers. These relays should co-ordinate with the non-directional relays, R1 and R2; ensuring discriminative relay operation during such fault conditions.

In such an application, relays R3 and R4 may commonly require non-directional overcurrent protection elements to provide protection to the 11 kV busbar, in addition to providing a back-up function to the overcurrent relays on the outgoing feeders (R5).

When applying the P64x relays in the above application, stage 1 of the overcurrent protection of relays R3 and R4 would be set non-directional and time graded with R5, using an appropriate time delay characteristic. Stage 2 could then be set directional, looking back into the transformer, also having a characteristic which provides correct coordination with R1 and R2. IDMT or DT characteristics are selectable for both stages 1 and 2 and directionality of each of the overcurrent stages is set in cell **I>x Direction**.

Note	*The principles previously outlined for the parallel transformer application are equally applicable for plain feeders which are operating in parallel.*

2.7 Standby Earth Fault Protection (SBEF)

The parallel transformer application previously shown in Figure 64 requires directional earth fault protection at locations R3 and R4, to provide discriminative protection. However, to provide back-up protection for the transformer, busbar and other downstream earth fault devices, StandBy Earth Fault (SBEF) protection is also commonly applied. This function is fulfilled by a separate earth fault current input, fed from a single CT in the transformer earth connection. The HV, LV and TV earth fault elements of the P64x relay may be used to provide both the directional earth fault (DEF) and SBEF functions, respectively.

Where a Neutral Earthing Resistor (NER) is used to limit the earth fault level to a particular value, it is possible that an earth fault condition could cause a flashover of the NER and hence a dramatic increase in the earth fault current. For this reason, it may be appropriate to apply two stage SBEF protection. The first stage should have suitable current and time characteristics which coordinate with downstream earth fault protection. The second stage may then be set with a higher current setting but with zero time delay, providing fast clearance of an earth fault which gives rise to an NER flashover.

The remaining two stages are available for customer-specific applications.

2.8 Directional Earth Fault Protection (DEF)

2.8.1 Residual Voltage Polarization

With earth fault protection, the polarizing signal needs to be representative of the earth fault condition. As residual voltage is generated during earth fault conditions, this quantity is commonly used to polarize DEF elements. The P64x relay internally derives this voltage from the 3-phase voltage input which must be supplied from either a five-limb or three single phase VTs. These types of VT design allow the passage of residual flux and consequently permit the relay to derive the required residual voltage. In addition, the primary star point of the VT must be earthed. A three-limb VT has no path for residual flux and is therefore unsuitable to supply the relay.

It is possible that small levels of residual voltage will be present under normal system conditions due to system imbalances, VT inaccuracies and relay tolerances. Therefore the P64x relay includes a user-settable threshold **IN>VNPol set** which must be exceeded for the DEF function to be operational. The residual voltage measurement provided in the MEASUREMENTS 1 column of the menu may assist in determining the required threshold setting during the commissioning stage, as this will indicate the level of standing residual voltage present.

Note *Residual voltage is nominally 180° out of phase with residual current. Consequently, the DEF elements are polarised from the -Vres quantity. This 180° phase shift is automatically introduced in the P64x relay.*

2.8.2 Negative Sequence Polarization

In certain applications, the use of residual voltage polarization of DEF may either be not possible to achieve, or problematic. An example of the former case would be where a suitable type of VT was unavailable, for example if only a three limb VT was fitted. An example of the latter case would be an HV/EHV parallel line application where problems with zero sequence mutual coupling may exist.

In either of these situations, the problem may be solved by the use of negative phase sequence (nps) quantities for polarization. This method determines the fault direction by comparison of nps voltage with nps current. The operating quantity, however, is still residual current.

This is available for selection on both the derived and measured standard earth fault elements. It requires a suitable voltage and current threshold to be set in cells **IN>V2pol set** and **IN>I2pol set**, respectively.

Negative sequence polarizing is not recommended for impedance earthed systems regardless of the type of VT feeding the relay. This is due to the reduced earth fault current limiting the voltage drop across the negative sequence source impedance (V2pol) to negligible levels. If this voltage is less than 0.5 volts the relay will cease to provide DEF protection.

2.8.3 General Setting Guidelines for DEF

When setting the Relay Characteristic Angle (RCA) for the directional overcurrent element, a positive angle setting was specified. This was due to the fact that the quadrature polarizing voltage lagged the nominal phase current by 90°. The position of the current under fault conditions was leading the polarizing voltage so a positive RCA was required. With DEF, the residual current under fault conditions lies at an angle lagging the polarizing voltage. Therefore negative RCA settings are required for DEF applications. This is set in the cell **I>Char Angle** in the relevant earth fault menu.

The following angle settings are recommended for a residual voltage polarized relay:

- Resistance earthed systems = 0°
- Distribution systems (solidly earthed) = –45°
- Transmission systems (solidly earthed) = –60°
- For negative sequence polarization, the RCA settings must be based on the angle of the NPS source impedance, much the same as for residual polarizing. Typical settings would be:
- Distribution systems –45°
- Transmission systems –60°

2.9 Negative Phase Sequence (NPS) Overcurrent Protection (46OC)

When applying traditional phase overcurrent protection, the overcurrent elements must be set higher than maximum load current, thereby limiting the element’s sensitivity. Most protection schemes also use an earth fault element, which improves sensitivity for earth faults. However, certain faults may arise which can remain undetected by such schemes.

Any unbalanced fault condition will produce negative sequence current of some magnitude. Therefore a negative phase sequence overcurrent element can operate for both phase to phase and phase to earth faults.

- Negative phase sequence overcurrent elements give greater sensitivity to resistive phase to phase faults, where phase overcurrent elements may not operate.

Note	*NPS overcurrent protection will not provide any system backup protection for three phase faults since there is no negative sequence current component for a three phase fault.*

- In certain applications, residual current may not be detected by an earth fault relay due to the system configuration. For example, an earth fault relay applied on the delta side of a delta-star transformer is unable to detect earth faults on the star side. However, negative sequence current will be present on both sides of the transformer for any fault condition, irrespective of the transformer configuration. Therefore, a negative phase sequence overcurrent element may be used to provide time-delayed backup protection for any uncleared asymmetrical faults downstream.
- For rotating machines a large amount of negative phase sequence current can be a dangerous condition for the machine due to its heating effect on the rotor. Therefore, a negative phase sequence overcurrent element may be applied to provide backup protection to the negative phase sequence thermal protection that is normally applied to a rotating machine.
- It may be required to simply alarm for the presence of negative phase sequence currents on the system. Operators may then investigate the cause of the unbalance.

2.9.1 Setting Guidelines for NPS Overcurrent Protection

- Since the negative phase sequence overcurrent protection does not respond to balanced-load or three-phase faults, negative sequence overcurrent relays may provide the desired overcurrent protection. This is particularly applicable to Δ−Y grounded transformers where only 58% of the secondary per unit phase-to-ground fault current appears in any one primary phase conductor. Backup protection can be particularly difficult when the Y is impedance-grounded.

2.9.1.1 Negative Phase Sequence (NPS) Current Threshold

A negative sequence relay can be connected in the primary supply to the transformer and set as sensitively as required to protect for secondary phase-to-ground or phase-to-phase faults. This function will also provide better protection than the phase overcurrent function for internal transformer faults. The NPS overcurrent protection should be set to coordinate with the low-side phase and ground relays for phase-to-ground and phase-to-phase faults. The current pickup threshold must also be set higher than the negative sequence current because of unbalanced loads. This can be set practically at the commissioning stage, making use of the relay measurement function to display the standing negative phase sequence current, and setting at least 20% above this figure.

Where the negative phase sequence element is required to operate for specific uncleared asymmetric faults, a precise threshold setting would have to be based on an individual fault analysis for that particular system due to the complexities involved. However, to ensure operation of the protection, the current pick-up setting must be set approximately 20% below the lowest calculated negative phase sequence fault current contribution to a specific remote fault condition.

Note	*In practice, if the required fault study information is unavailable, the setting must adhere to the minimum threshold previously outlined, employing a suitable time delay for co-ordination with downstream devices, this is vital to prevent unnecessary interruption of the supply resulting from inadvertent operation of this element.*

2.9.1.2 Time Delay for the Negative Phase Sequence Overcurrent Element

As stated above, correct setting of the time delay for this function is vital. It should also be noted that this element is applied primarily to provide backup protection to other protective devices, or to provide an alarm or used in conjunction with neutral voltage displacement protection for interturn protection. Therefore in practice it would be associated with a long time delay if used to provide backup protection or an alarm.

Where the protection is used for backup protection or as an alarm it must be ensured that the time delay is set greater than the operating time of any other protective device (at minimum fault level) on the system which may respond to unbalanced faults, such as:

- Phase overcurrent elements
- Earth fault elements

2.9.1.3 Directionalizing the Negative Phase Sequence (NPS) Overcurrent Element

Where negative phase sequence current may flow in either direction through a relay location, such ring main systems, directional control of the element should be used.

Directionality is achieved by comparison of the angle between the negative phase sequence voltage and the negative phase sequence current and the element may be selected to operate in either the forward or reverse direction. A suitable relay characteristic angle setting (**2> Char Angle**) is chosen to provide optimum performance. This setting should be set equal to the phase angle of the negative sequence current with respect to the inverted negative sequence voltage (–V2), to be at the center of the directional characteristic.

The angle that occurs between V2 and I2 under fault conditions is directly dependent on the negative sequence source impedance of the system. However, typical settings for the element are as follows:

- For a transmission system the RCA should be set equal to –60°
- For a distribution system the RCA should be set equal to –45°

For the negative phase sequence directional elements to operate, the relay must detect a polarizing voltage above a minimum threshold, **I2> V2pol Set**. This must be set in excess of any steady state negative phase sequence voltage. This may be determined during the commissioning stage by viewing the negative phase sequence measurements in the relay.

2.10 Undervoltage Protection Function (27)

Undervoltage conditions may occur on a power system for a variety of reasons, some of which are outlined below:

- Increased system loading. Generally, some corrective action would be taken by voltage regulating equipment such as AVRs or On Load Tap Changers, to bring the system voltage back to its nominal value. If the regulating equipment is unsuccessful in restoring healthy system voltage, tripping with an undervoltage relay will be required following a suitable time delay.
- Faults occurring on the power system result in a reduction in voltage of the phases involved in the fault. The proportion by which the voltage decreases is directly dependent on the type of fault, method of system earthing and it’s location with respect to the relaying point. Consequently, co-ordination with other voltage and current-based protection devices is essential to achieve correct discrimination.
- Complete loss of busbar voltage. This may occur due to fault conditions present on the incomer or busbar itself, resulting in total isolation of the incoming power supply. For this condition, it may be a requirement for each of the outgoing circuits to be isolated, so that when supply voltage is restored, the load is not connected. Therefore the automatic tripping of a feeder on detection of complete loss of voltage may be required. This may be achieved by a three-phase undervoltage element.
- Where outgoing feeders from a busbar are supplying induction motor loads, excessive dips in the supply may cause the connected motors to stall, and should be tripped for voltage reductions which last longer than a pre-determined time. Both the under and overvoltage protection functions can be found in the relay menu Volt Protection.

2.10.1 Setting Guidelines for Undervoltage Protection

The undervoltage protection is an optional feature within the P64x. It is available on request of the three-phase VT input.

In the majority of applications, undervoltage protection is not required to operate during system earth fault conditions. If this is the case, the element should be selected in the menu to operate from a phase to phase voltage measurement, as this quantity is less affected by single-phase voltage depressions due to earth faults.

The undervoltage protection can be set to operate from phase-phase or phase-neutral voltage as selected by **V< Measur't Mode**. Single or three-phase operation can be selected in **V< Operate Mode**. When Any Phase is selected, the element will operate if any phase voltage falls below setting, when Three-phase is selected the element will operate when all three-phase voltages are below the setting.

The voltage threshold setting for the undervoltage protection should be set at some value below the voltage excursions that may be expected under normal system operating conditions. This threshold is dependent on the system in question but typical healthy system voltage excursions may be in the order of -10% of the nominal value.

Similar comments apply with regard to a time setting for this element, so the required time delay is dependent on the time for which the system is able to withstand a depressed voltage. If motor loads are connected, a typical time setting may be in the order of 0.5 seconds.

Stage 1 may be selected as either IDMT (for inverse time delayed operation), DT (for definite time delayed operation) or Disabled, in the **V<1 Function** cell. Stage 2 is definite time only and is **Enabled** or **Disabled** in the **V<2 Status** cell. The time delay (**V<1 TMS** for IDMT curve; **V<1 Time Delay**, **V<2 Time Delay** for definite time) should be adjusted accordingly.

Stage 2 can be set as an alarm stage to warn the user of unusual voltage conditions so that corrections can be made.

If only a single phase VT signal is available and the user requires an undervoltage alarm, then the P643/P645 (three-phase VT input required) may provide this alarm as long as the VTS status is set to disable. Setting the VTS status to disable will prevent the Fast VTS Block signal from blocking the undervoltage element. Relays with software version 02B and further have the option of disabling the VTS status. Relays with software versions 01B and 01D do not have this option. The V< Measur't Mode is set Phase-Neutral and the V< Operate Mode is set Three Phase.

2.11 Overvoltage Protection (59)

As previously discussed, undervoltage conditions are relatively common, as they are related to fault conditions. However, overvoltage conditions are also a possibility and are generally related to loss of load conditions. Under conditions of load rejection, the supply voltage will increase in magnitude. This situation would normally be rectified by voltage regulating equipment such as AVRs or on-load tap changers. However, failure of this equipment to bring the system voltage back within prescribed limits leaves the system with an overvoltage condition which must be cleared to preserve the life of the system insulation. Therefore overvoltage protection that is suitably time-delayed to allow for normal regulator action may be applied. Also, during earth fault conditions on a power system, there may be an increase in the healthy phase voltages. Ideally the system should be designed to withstand such overvoltages for a defined period.

Overvoltage protection prevents insulation damage due to excessive voltages. Some of the causes of overvoltage at system frequency are listed below:

- Sudden loss of load caused by the disconnection of a heavily loaded power line
- Lightly loaded long transmission lines with high capacitance
- Phase to earth faults in unearthed or high impedance earthed systems
- Incorrect operation of a voltage regulator or wrong settings under manual voltage
- Overspeed of generator when disconnected from the network and incorrect operation of the machine AVR control

Transformers must not be subject to prolonged overvoltage because the insulation would be damaged. For maximum efficiency they are operated near the knee of their saturation curve, so at voltages above about 110% of rated, the exciting current becomes very high. A few percent increase in voltage results in a very large increase in exciting current. These large currents can destroy the unit if not reduced promptly. Protection against overvoltage is seldom applied directly, but it is included in regulating and control devices for the power system. On the other hand, overvoltage for generator-transformer units is more likely to occur, therefore an overvoltage protection may be considered.

2.11.1 Setting Guidelines for Overvoltage Protection

The overvoltage protection is an optional feature in the P64x. It is available on request of the three-phase VT input.

The inclusion of the two stages and their respective operating characteristics allows a number of possible applications:

- Use of the IDMT characteristic gives the option of a longer time delay if the overvoltage condition is only slight but results in a fast trip for a severe overvoltage. As the voltage settings for both of the stages are independent, the second stage could then be set lower than the first to provide a time delayed alarm stage if required.
- Alternatively, if preferred, both stages could be set to definite time and configured to provide the required alarm and trip stages.
- If only one stage of overvoltage protection is required, or if the element is required to provide an alarm only, the remaining stage may be disabled within the relay menu.

Stage 1 may be selected as either IDMT (for inverse time delayed operation), DT (for definite time delayed operation) or Disabled, in the **V>1 Function** cell. Stage 2 has a definite time delayed characteristic and is Enabled or Disabled in the **V>2 Status** cell. The time delay (**V>1 TMS** for IDMT curve; **V>1 Time Delay**, **V>2 Time Delay** - for definite time) should be selected accordingly.

The overvoltage protection can be set to operate from Phase-Phase or Phase-Neutral voltage as selected by the **V> Measur't Mode** cell. Single or three-phase operation can be selected in the **V> Operate Mode** cell. When **Any Phase** is selected the element will operate if any phase voltage is above setting; when **Three-phase** is selected the element will operate when all three-phase voltages are above the setting.

Transformers can typically withstand a 110% overvoltage condition continuously. The withstand times for higher overvoltages should be declared by the transformer manufacturer.

To prevent operation during earth faults, the element should operate from the phase-phase voltages. To achieve this **V>1 Measur't Mode** can be set to **Phase-Phase** with **V>1 Operating Mode** set to **Three-phase**. The overvoltage threshold **V>1 Voltage Set** should typically be set to 100% - 120% of the nominal phase-phase voltage seen by the relay. The time delay **V>1 Time Delay** should be set to prevent unwanted tripping of the delayed overvoltage protection function due to transient over voltages that do not pose a risk to the transformer. The typical delay to be applied would be 1s - 3s, with a longer delay being applied for lower voltage threshold settings.

The second stage can be used to provide instantaneous high-set over voltage protection. The typical threshold setting to be applied, **V>2 Voltage Set**, would be 130 - 150% of the nominal phase-phase voltage seen by the relay, depending on transformer manufacturers' advice and the utilities practice. For instantaneous operation, the time delay, **V>2 Time Delay**, should be set to 0 s.

If phase to neutral operation is selected, care must be taken to ensure that the element will grade with other protections during earth faults, where the phase-neutral voltage can rise significantly.

This type of protection must be coordinated with any other overvoltage relays at other locations on the system. This should be carried out in a similar manner to that used for grading current operated devices.

2.12 Residual Overvoltage/Neutral Voltage Displacement Protection Function (59N)

On a healthy three-phase power system, the addition of each of the three-phase to earth voltages is nominally zero, as it is the vector addition of three balanced vectors at 120° to one another. However, when an earth fault occurs on the primary system this balance is upset and a ‘residual’ voltage is produced.

In the P64x, the residual overvoltage is an optional feature. It is calculated by adding up the three-phase voltage vectors corresponding to the optional three-phase voltage input. Hence, a residual voltage element can be used to offer earth fault protection on such a system. This condition causes a rise in the neutral voltage with respect to earth that is commonly referred to as neutral voltage displacement or NVD.

2.12.1 Setting Guidelines for Residual Overvoltage/Neutral Voltage Displacement Protection

Stage 1 may be selected as either **IDMT** (inverse time operating characteristic), **DT** (definite time operating characteristic) or **Disabled**, in the **VN>1 Function** cell. Stage 2 operates with a definite time characteristic and is **Enabled** or **Disabled** in the **VN>2 Status** cell. The time delay. (**VN>1 TMS** for IDMT curve; **V>1 Time Delay**, **V>2 Time Delay** for definite time) should be selected in accordance with normal relay coordination procedures to ensure correct discrimination for system faults.

It must be ensured that the voltage setting of the element is set above any standing level of residual voltage that is present on the system. A typical setting for residual overvoltage protection is 5 V.

The second stage of protection can be used as an alarm stage on unearthed or very high impedance earthed systems where the system can be operated for an appreciable time under an earth fault condition.

2.13 Negative Phase Sequence Overvoltage Protection (47)

Where an incoming feeder is supplying a switchboard that is feeding rotating plant (e.g. a motor), correct phasing and balance of the ac supply is essential. Incorrect phase rotation could result in any connected machines rotating in the wrong direction. For some hydro machines two-phases can be swapped to allow the machine to rotate in a different direction to act as a generator or a motor pumping water.

Any unbalanced condition occurring on the incoming supply will result in the presence of negative phase sequence (NPS) components of voltage. In the event of incorrect phase rotation, the supply voltage would effectively consist of 100% negative phase sequence voltage only.

The P64x relay includes a NPS overvoltage element that responds to negative phase sequence voltage that may result from a fault or misconnection in a balanced three phase system. This element monitors the input voltage rotation and magnitude (normally from a bus connected voltage transformer).

The NPS overvoltage element can also be used to provide an additional check to indicate a phase-earth or phase-phase fault is present for the voltage controlled overcurrent protection in the PSL as shown in Figure 66. In this application the NPS overvoltage protection can be accelerated when the CB operating time is <60 ms) to prevent incorrect operation when closing the CB due to pole scattering. However, when the CB is closed there is no need to inherently slow the protection start (typical accelerated operating time is <40 ms). The V2>1 Accelerate signal (DDB 663) connected to CB Closed signal (DDB 719, 721, 723, 725, 727) can be used to accelerate the protection start as shown in Figure 65.

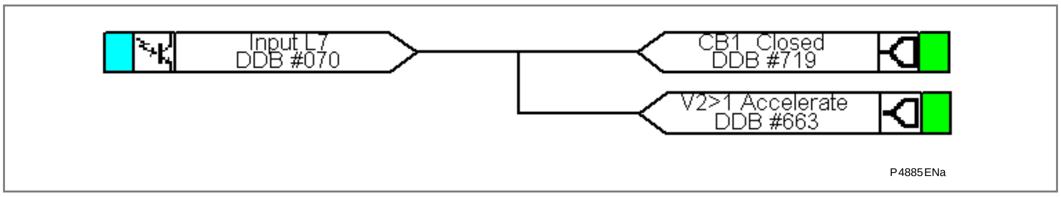


Figure 65 - V2>1 Accelerate – PSL configuration

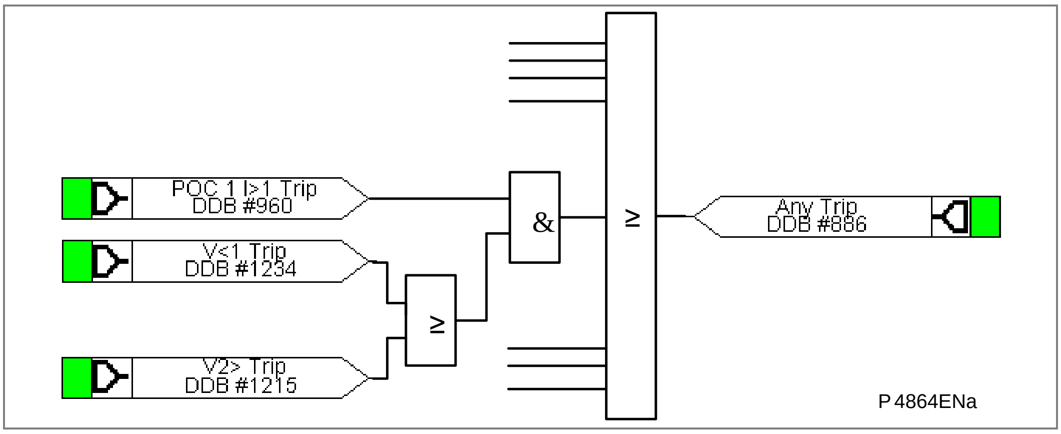


Figure 66 - NPS overvoltage control – PSL configuration

2.13.1 Setting Guidelines

If the primary concern is the detection of incorrect phase rotation (rather than small unbalances), a sensitive setting is not required. It must be ensured that the setting is above any standing NPS voltage that may be present due to imbalances in the measuring VT, relay tolerances etc. A setting of approximately 15% of rated voltage may be typical.

Note that standing levels of NPS voltage (V2) are displayed in "Measurements 1" column of the relay menu, labeled "V2 Magnitude". Hence, if more sensitive settings are required, they may be determined during the commissioning stage by viewing the actual level that is present.

The operation time of the element is highly dependent on the application. A typical setting would be in the region of 5 s. If the NPS overvoltage element is used to provide an additional check for the voltage controlled overcurrent element, set the time delay to 0 s.

2.14 Underfrequency Protection (81U)

Generation and utilization need to be well balanced in any industrial, distribution or transmission network. As load increases, the generation needs to be stepped up to maintain frequency of the supply because there are many frequency-sensitive electrical apparatus that can be damaged when network frequency departs from the allowed band for safe operation. At times, when sudden overloads occur, the frequency drops at a rate decided by the system inertia constant, magnitude of overload, system damping constant and various other parameters. Unless corrective measures are taken at the appropriate time, frequency decay can go beyond the point of no return and cause widespread network collapse. In a wider scenario, this can result in “Blackouts”. To put the network back in healthy condition, a considerable amount of time and effort is required to resynchronize and re-energize.

Protective relays that can detect a low frequency condition are generally used in such cases to disconnect unimportant loads to save the network, by re-establishing the “generation-load equation”. However, with such devices, the action is initiated only after the event and while some salvaging of the situation can be achieved, this form of corrective action may not be effective enough and cannot cope with sudden load increases, causing large frequency decays in very short times. In such cases a device that can anticipate the severity of frequency decay and act to disconnect loads before the frequency actually reaches dangerously low levels, can become very effective in containing damage.

During severe disturbances, the frequency of the system oscillates as various generators try to synchronize on to a common frequency. The measurement of instantaneous rate of change of frequency can be misleading during such a disturbance. The frequency decay needs to be monitored over a longer period of time to make the correct decision for load shedding.

Normally, generators are rated for a lifetime operation in a particular band of frequency and operation outside this band can cause mechanical damage to the turbine blades. Protection against such contingencies is required when frequency does not improve even after load shedding steps have been taken and can be used for operator alarms or turbine trips in case of severe frequency decay.

While load shedding leads to an improvement in the system frequency, the disconnected loads need to be reconnected after the system is stable again. Loads should only be restored if the frequency remains stable for some period of time, but minor frequency excursions can be ignored during this time period. The number of load restoration steps are normally less than the load shedding steps to reduce repeated disturbances while restoring load.

Four independent definite time-delayed stages of underfrequency protection are offered.

2.14.1 Setting Guidelines for Underfrequency Protection

To minimize the effects of underfrequency on a system, a multi stage load shedding scheme may be used with the plant loads prioritized and grouped. During an underfrequency condition, the load groups are disconnected sequentially depending on the level of underfrequency, with the highest priority group being the last one to be disconnected.

The effectiveness of each stage of load shedding depends on what proportion of the power deficiency it represents. If the load shedding stage is too small compared to the prevailing generation deficiency, the improvement in frequency may be non-existent. This aspect should be taken into account when forming the load groups.

Time delays should be sufficient to override any transient dips in frequency, as well as to provide time for the frequency controls in the system to respond. This should be balanced against the system survival requirement since excessive time delays may cause the system stability to be in jeopardy. Time delay settings of 5 to 20 s are typical.

Each stage of under frequency protection may be selected as **Enabled** or **Disabled** in the **F<x Status** cells. The frequency pickup setting, **F<x Setting**, and time delays, **F<x Time Delay**, for each stage should be selected accordingly.

The protection function should be set so that declared frequency-time limits for the generating set are not infringed. Typically, a 10% under frequency condition should be continuously sustainable.

The P64x under frequency protection function could be used to initiate local system load shedding when required. Four stages under frequency/load shedding can be provided.

2.15 Overfrequency Protection Function (81O)

Overfrequency running of a generator arises when the mechanical power input to the machine exceeds the electrical output. This could happen, for instance, when there is a sudden loss of load due to tripping of an outgoing feeder from the plant to a load centre.

Under such over speed conditions, the governor should respond quickly to obtain a balance between the mechanical input and electrical output, thereby restoring normal frequency. Over frequency protection is required as a backup to cater for slow response of frequency control equipment.

Two independent time-delayed stages of overfrequency protection are provided in the P64x.

2.15.1 Setting Guidelines for Overfrequency Protection

Following faults on the network, or other operational requirements, it is possible that various subsystems will be formed within the power network and it is likely that each of these subsystems will suffer from a generation to load imbalance. The “islands” where generation exceeds the existing load will be subject to over frequency conditions, the level of frequency being a function of the percentage of excess generation. Severe over frequency conditions may be unacceptable to many industrial loads, since running speeds of motors will be affected. The overfrequency element of the P64x can be suitably set to sense this contingency.

The settings for the overfrequency element depend on the maximum frequency that the equipment can tolerate for a given period of time.

Each stage of overfrequency protection may be selected as **Enabled** or **Disabled** in the **F>x Status** cells. The frequency pickup setting **F>x Setting** and time delays **F>x Time Delay** for each stage should be selected accordingly.

2.16 Circuit Breaker Fail (CBF) Protection

Following inception of a fault one or more main protection devices will operate and issue a trip output to the circuit breaker(s) associated with the faulted circuit. Operation of the circuit breaker is essential to isolate the fault, and prevent damage / further damage to the power system. For transmission/sub-transmission systems, slow fault clearance can also threaten system stability. It is therefore common practice to install circuit breaker failure protection, which monitors that the circuit breaker has opened within a reasonable time. If the fault current has not been interrupted following a set time delay from circuit breaker trip initiation, Circuit Breaker Failure (CBF) protection will operate.

CBF operation can be used to backtrip upstream circuit breakers to ensure that the fault is isolated correctly. CBF operation can also reset all start output contacts, ensuring that any blocks asserted on upstream protection are removed.

2.16.1 Reset Mechanisms for Breaker Fail Timers

It is common practice to use low set undercurrent elements in protection relays to indicate that circuit breaker poles have interrupted the fault or load current, as required. This covers the following situations:

- Where circuit breaker auxiliary contacts are defective, or cannot be relied on to definitely indicate that the breaker has tripped.
- Where a circuit breaker has started to open but has become jammed. This may result in continued arcing at the primary contacts, with an additional arcing resistance in the fault current path. Should this resistance severely limit fault current, the initiating protection element may reset. Therefore reset of the element may not give a reliable indication that the circuit breaker has opened fully.

For any protection function requiring current to operate, the relay uses operation of undercurrent elements (I<) to detect that the necessary circuit breaker poles have tripped and reset the CB fail timers. However, the undercurrent elements may not be reliable methods of resetting circuit breaker fail in all applications. For example:

- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a line connected voltage transformer. Here, I< only gives a reliable reset method if the protected circuit would always have load current flowing. Detecting drop-off of the initiating protection element might be a more reliable method.
- Where non-current operated protection, such as under/overvoltage or under/overfrequency, derives measurements from a busbar connected voltage transformer. Again using I< would rely on the feeder normally being loaded. Also, tripping the circuit breaker may not remove the initiating condition from the busbar, so drop-off of the protection element may not occur. In such cases, the position of the circuit breaker auxiliary contacts may give the best reset method.

2.16.2 Setting Guidelines for CBF Protection

2.16.2.1 Breaker Fail Timer Settings

Figure 67 shows the time chart during normal and breaker failure operation. The maximum clearing time should be less than the critical clearing time which is determined by a stability study. The CBF back-up trip time delay considers the maximum breaker clearing time, the CBF reset time and a safety margin. Typical circuit breakers clearing times are 1.5 or 3 cycles. The CBF reset time should be short enough to avoid CBF back-trip during normal operation. Phase and ground undercurrent elements must be asserted for the CBF to reset. The assertion of the undercurrent elements might be delayed due to the subsidence current that might be flowing through the secondary AC circuit. The subsidence current is the result of the decaying flux in the CT core once the primary current has been interrupted. The delay in asserting the undercurrent elements will cause an unwanted breaker failure operation. In the P64x, a zero crossing detection technique has been implemented to avoid this unwanted operation.

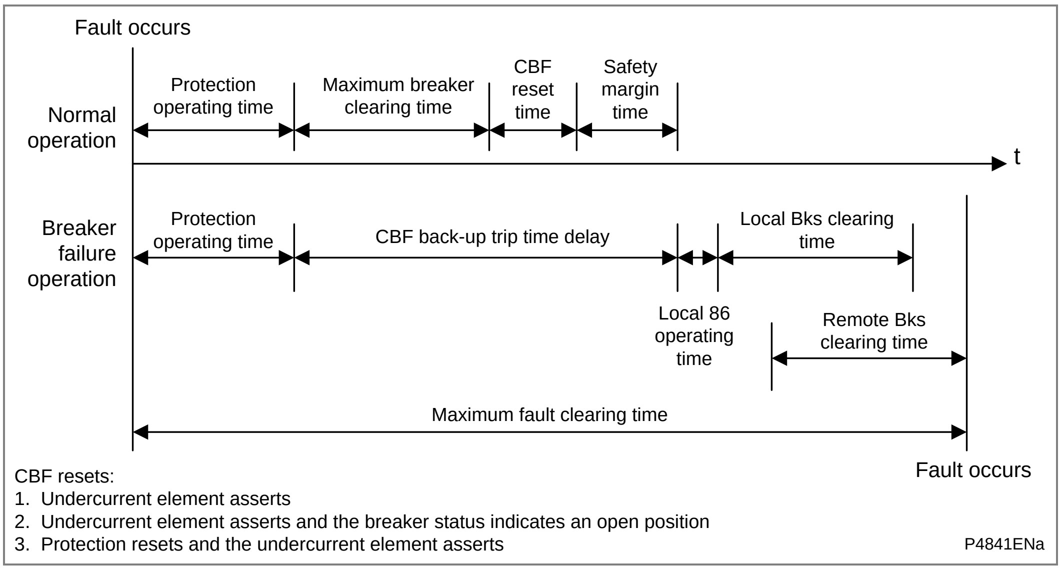

Fault occurs
Normal operation
Protection operating time
Maximum breaker clearing time
CBF reset time
Safety margin time
t
Breaker failure operation
Protection operating time
CBF back-up trip time delay
Local Bks clearing time
Local 86 operating time
Remote Bks clearing time
Maximum fault clearing time
Fault occurs
CBF resets:
1. Undercurrent element asserts
2. Undercurrent element asserts and the breaker status indicates an open position
3. Protection resets and the undercurrent element asserts
P4841ENa

Figure 67 - Breaker failure time chart

Typical timer settings to use are as follows:

CB fail reset mechanism	tBF time delay	Typical delay for 2 cycle circuit breaker
Initiating element reset	CB interrupting time + element reset time (max.) + error in tBF timer + safety margin	50 + 50 + 10 + 50 = 160 ms

CB fail reset mechanism	tBF time delay	Typical delay for 2 cycle circuit breaker
CB open	CB auxiliary contacts opening/ closing time (max.) + error in tBF timer + safety margin	50 + 10 + 50 = 110 ms
Undercurrent elements	CB interrupting time + undercurrent element (max.) + safety margin operating time	50 + 25 + 50 = 125 ms

Table 7 - Typical timer settings

> *Note* *All CB Fail resetting involves the operation of the undercurrent elements. Where element reset or CB open resetting is used the undercurrent time setting should still be used if this proves to be the worst case.*

The examples above consider direct tripping of a 2-cycle circuit breaker.

> *Note* *Where auxiliary tripping relays are used, an additional 10 to 15 ms must be added to allow for trip relay operation.*

2.16.2.2 Breaker Fail Undercurrent Settings

The phase undercurrent settings (I<) must be set less than load current, to ensure that I< operation indicates that the circuit breaker pole is open. A typical setting for overhead line or cable circuits is 20% In, with 5% In common for generator circuit breaker CBF.

2.16.3 Example 1

Consider an application having two breakers on the HV side and two breakers on the LV side. Overcurrent1 has been set to HV winding and Overcurrent2 to LV winding. Stages 1 of Overcurrent1 and 2 are used as back-up protection. The HV breakers must open when Overcurent1 is asserted but not Overcurrent2. The LV breakers must open when Overcurent2 is asserted but not Overcurrent1. The circuit breaker failure timers of breakers 1 and 2 should not be initiated when Overcurrent2/Stage 1 is asserted, and the circuit breaker failure timers of breakers 4 and 5 should not be initiated when Overcurrent1/Stage 1 is asserted. As indicated in the CB fail logic given in the Operation Chapter, the Any Trip signal starts all the breaker failure timers. POC 1 I>1 Trip and POC 2 I>1 Trip signals should be removed from the any trip mapping in psl. This is to avoid starting the HV circuit breaker failure timers due to POC 2 I>1 Trip and starting the LV circuit breaker failure timers due to POC 1 I>1 Trip. From the circuit breaker Our scheme requires the HV breakers to trip on Idiff, HV I>1, and HV IN>1. The LV breakers trip on Idiff, LV I>1 and LV IN>1.

Removing POC 1 I>1 Trip and POC 2 I>1 Trip from the any trip mapping prevents lighting the any trip led when POC 1 I>1 Trip or POC 2 I>1 Trip is asserted.

To generate fault records due to POC 1 I>1 Trip and POC 2 I>1 Trip, this signals should be configured in the fault record trigger in psl.

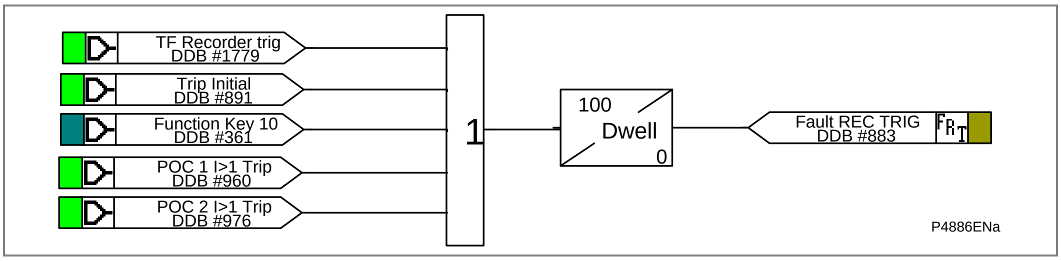


Figure 68 - Fault record trigger configuration

Configure POC 1 I>1 Trip to Extern CB1 trip and Extern CB2 trip in psl to initiate HV circuit breaker failure timers. Configure POC 2 I>1 Trip to Extern CB4 trip and Extern CB5 trip in psl to initiate LV circuit breaker failure timers.

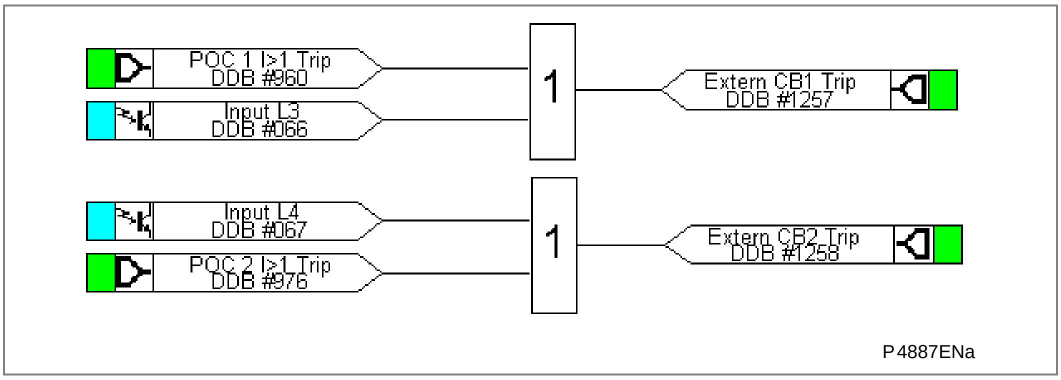


Figure 69 - External CB Trip

2.17 Resistive Temperature Device (RTD) Thermal Protection

Prolonged overloading of transformers may cause their windings to overheat, resulting in premature ageing of the insulation, or in extreme cases, insulation failure. To protect against any general or localized overheating, the P642/P643/P645 relay has the ability to accept inputs from up to 10 - 3-wire Type A PT100 Resistive Temperature Device (RTD) sensors.

Such probes can be strategically placed in areas of the equipment that are susceptible to overheating or heat damage. This could protect against winding hot spot overheating or overtemperature in the bulk of the insulating oil.

Typically a PT100 RTD probe can measure temperature within the range –40° to +300°C. The resistance of these devices changes with temperature, at 0°C they have a resistance of 100 Ω. The temperature at each probe location can be determined by the relay, and is available for:

- Temperature monitoring, displayed locally, or remotely using the relay communications
- Alarming, should a temperature threshold be exceeded for longer than a set time delay
- Tripping, should a temperature threshold be exceeded for longer than a set time delay

Should the measured resistance be outside of the permitted range, an RTD failure alarm will be raised, indicating an open or short circuit RTD input.

Note	*Direct temperature measurement can provide more reliable thermal protection than devices that use a thermal replica energized from phase current. The latter is susceptible to inaccuracies in time constants used by the replica model, and also inaccuracies due to the variation in ambient temperature.*

See the *Installation* chapter *P64x/EN IN*, for recommendations on RTD connections and cables.

2.17.1 Setting Guidelines for RTD Thermal Protection

Each RTD can be enabled by setting the relevant bit in **Select RTD**. For example if Select RTD is set to 0000000111, then RTD1, RTD2 and RTD3 would be enabled and the associated settings would be visible in the menu.

The temperature setting for the alarm stage for each RTD can be set in the **RTD x Alarm Set** cells and the alarm time delay in the **RTD x Alarm Dly** cell.

The temperature setting for the trip stage for each RTD can be set in the **RTD x Trip Set** cells and the trip stage time delay in the **RTD x Trip Dly** cell.

Typical operating temperatures for protected plant are given in the table below. These are provided as a guide, actual figures MUST be obtained from the equipment manufacturers:

Parameter	Typical service temperature	Short term overloading at full load
Bearing temperature generators	60 - 80°C, depending on the type of bearing.	60 - 80°C+
Top oil temperature of transformers	80°C (50 - 60°C above ambient).	A temperature gradient from winding temperature is usually assumed, so that top oil RTDs can provide winding protection
Winding hot spot temperature	98°C for normal ageing of insulation.	140°C+ during emergencies

Table 8 - Typical operating temperatures of plant

2.18 Thermal Overload Protection (49)

Transformer overheating can be caused due to failures of the cooling system, external faults that are not clear promptly, overload and abnormal system conditions. These abnormal conditions include low frequency, high voltage, non-sinusoidal load current, or phase-voltage unbalance.

Overheating shortens the life of the transformer insulation in proportion to the duration and magnitude of the high temperature. Overheating can generate gases that could result in electrical failure. Furthermore, excessive temperature may result in an immediate insulation failure. Also, the transformer coolant may be heated above its flash temperature, therefore a fire can be caused.

Results suggest that the life of insulation is approximately halved for each 10°C rise in temperature above the rated value. However, the life of insulation is not wholly dependent on the rise in temperature but on the time the insulation is maintained at this elevated temperature. Due to the relatively large heat storage capacity of a transformer, infrequent overloads of short duration may not damage it. However, sustained overloads of a few percent may result in premature ageing and failure of insulation.

The thermal overload protection in the P64x is based on IEEE Standard C57.91-1995. Thermal overload trip can be based on hot spot temperature, Θ_H, or top oil temperature, Θ_{TO}. Top oil temperature can be calculated or can be measured directly when either CLIO or RTD are available. Hot spot temperature is only calculated.

It is important to consider ambient temperature to determine the load capability of a transformer. The ambient temperature is the temperature of the air in contact with the transformer’s radiators. To determine the operating temperature, the temperature rise due to load is added to the ambient temperature. IEEE Standard C57.91-1995 states that transformer ratings are based on 24 hour average ambient temperature of 30°C. If the ambient temperature can be measured, then it should be averaged over a 24 hour period. In the P64x relays, the ambient temperature, Θ_A, can be measured directly or an average value can be set by the user.

The simplest application of overload protection employs I^2t characteristic. Time constants such as the winding time constant at hot spot location, τ_W, and top oil rise time constant, τ_{TO}, are set, so that the thermal model can follow the correct exponential heating and cooling profile, replicating the winding hotspot temperature. Transformer loads are becoming increasingly non-linear; hence, the P64x uses rms current values to replicate the winding hotspot temperature.

2.18.1 Setting Guidelines

The following tables are examples of the thermal data given by the transformer manufacturer. This data is required to set the thermal overload function.

Thermal characteristic 735 MVA 300 kV +7% to -18% / 23kV ODWF cooled generator transformer	
No load losses (core losses)	340 kW
Load losses at nominal tap	1580 kW
Load losses at maximum current tap	1963 kW
Oil time constant	2.15 hr
Oil exponent	1.0
Top oil rise over ambient temperature at rated load	33.4 K
Winding time constant at hot spot location	14 mins
Winding hottest spot rise over top oil temperature at rated load	30.2 K
Winding exponent	2.0

Table 9 - Example of thermal data given by transformer manufacturer

Note	*OD (oil directed) indicates that oil from heat exchangers (radiators) is forced to flow through the windings. WF states that the oil is externally cooled by pumped water.*

Thermal characteristic 600 MVA 432/23.5 kV ODWF cooled generator transformer	
No load losses (core losses)	237 kW
Load losses at nominal tap	1423 kW
Load losses at maximum current tap	1676 kW
Oil time constant	2.2 hr
Oil exponent	1.0
Top oil rise over ambient temperature at rated load	46.6 K
Winding time constant at hot spot location	9 mins
Winding hottest spot rise over top oil temperature at rated load	33.1K
Winding exponent	2.0

Table 10 - Example of thermal data given by transformer manufacturer

Thermal characteristic IEC60354 figures based on medium-large power transformers OD cooled	
Oil time constant	1.5 hr
Oil exponent	1.0
Top oil rise over ambient temperature at rated load	49 K
Winding time constant at hot spot location	5-10 mins
Winding hottest spot rise over top oil temperature at rated load	29 K
Winding exponent	2.0

Table 11 - Example of thermal data given by transformer manufacturer

The monitor winding can be set either to HV, LV, TV or biased current. It is recommended to set it to biased current so an overall thermal condition of the transformer is provided. The ambient temperature can be set to average (average ambient temperatures covers 24 hour time periods), or it can be measured directly using a CLI or RTD input. Top oil temperature may be set as calculated or measured. IB is the load in pu, and it is recommended to set it at rated load, of 1.0 pu. The following parameters should be provided by the transformer manufacturer:

- The ratio of load loss at rated load to no load loss (Rated NoLoadLoss). For example, if the no load losses are 340 kW and load losses at rated are 1580 kW, the rated NoLoadLoss is 1580/340 = 4.6.

The losses in a transformer are shown in Figure 70:

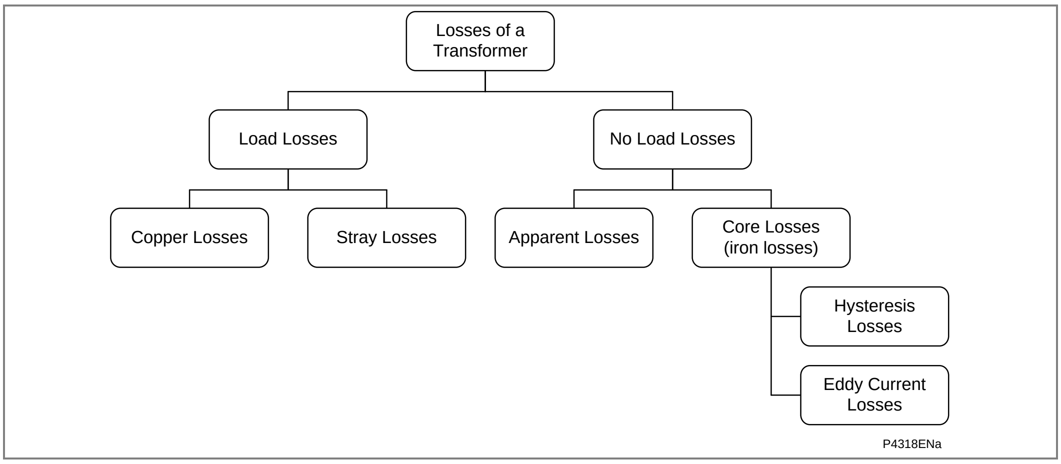


Figure 70 - Transformer losses

No-load losses are mainly iron losses. The loss that is due to the magnetizing current in the primary winding is called the apparent loss. The flow of the magnetizing current through the resistance of the winding does create a real I^2R loss and voltage drop, although both are generally quite small. Time-varying fluxes produce losses in ferromagnetic materials, known as core losses. These iron losses are divided into hysteresis losses and eddy-current losses.

The sum of copper losses and the stray losses is called the load losses. Cooper losses are due to the flow of load currents through the primary and secondary windings. They are equal to I^2R, and they heat up the wires and cause voltage drops. Stray losses are due to the stray capacitance and leakage inductance. Stray capacitance exists between turns, between one winding and another, and between windings and the core.

- Winding hottest-spot rise over top oil at rated load (Hot Spot overtop)
- Top oil rise over ambient temperature at rated load (Top Oil overamb). It can also be determined by actual test as per IEEE Std. C57.12.90-1993.
- Winding exponent (Winding exp m) and oil exponent (Oil exp n)

As indicated in the IEEE Std. C57.91-1995, Table 12 suggests winding and oil exponents.

Type of cooling	m (winding exponent)	n (oil exponent)
OA	0.8	0.8
FA	0.8	0.9
Non-directed FOA or FOW	0.8	0.9
Directed FOA or FOW	1.0	1.0

Type of cooling	m (winding exponent)	n (oil exponent)
Note OA=Oil/Air, FA=Forced Air, FOA=Forced Oil and Air FOW=Forced Oil and Water		

Table 12 - Suggested winding and oil exponents

ONAN or OA stands for Oil/Air: the cooling system transfers heat using oil to air without using pumps or fans. ONAF or FA stands for Forced Air: the cooling is aided by fans, but without any pumps to circulate the oil. With both of these systems the oil circulates through the radiators or heat exchangers by normal convection only. OFAF or FOA stands for Forced Oil and Air: the cooling system uses both pumps and fans to cool the oil. OFWF or FOW stands for Forced Oil and Water: the heat exchanger is water-cooled and does not have the typical radiator configuration. The cooler is normally a chamber with many tubes inside where the oil and water exchange heat energy. In non-directed flow transformers, the pumped oil flows freely through the tank. In directed flow transformers, the pumped oil is forced to flow through the windings.

These exponents are empirically derived and are required to calculate the variation of $\Delta\Theta H$ and $\Delta\Theta_{TO}$ with load changes. The value of m has been selected for each mode of cooling to approximately account for effects of changes in resistance and off viscosity with changes in load. The value of n has been selected for each mode of cooling to approximately account for effects of change in resistance with change in load.

- Winding time constant at hot spot location (Hot spot rise co). It may also be estimated from the resistance cooling curve during thermal tests.
- Oil time constant (Top oil rise co)

The P64x has up to three hot spot stages and up to three top oil stages. The tripping signal, Top Oil T>x Trip, is asserted when the top oil (measured or calculated) temperature is above the setting, **Top Oil>x Set**, and the time delay, **tTop Oil>x Set** has elapsed. Also, the tripping signal, Hot Spot>x Trip, is asserted when the hottest-spot (calculated only) temperature is above the setting, **Hot Spot>x Set**, and the time delay, **tHot Spot>x Set** has elapsed.

When setting the hot spot and top oil stages take into consideration the suggested temperature limits (IEEE Std. C57.91-1995):

Suggested limits of temperature for loading above nameplate distribution transformers with 65°C rise	
Top oil temperature	120°C
Hot spot conductor temperature	200°C

Suggested limits of temperature for loading above nameplate power transformers with 65°C rise (refer to IEEE Std. C57.91-1995 to consider the four types of loading)	
Top oil temperature	110°C
Hot spot conductor temperature	180°C

Table 13 - Suggested temperature limits (IEEE Std. C57.91-1995):

2.19 Loss of Life

As stated in IEEE Std. C57.91-1995, aging of insulation is a time function of temperature, moisture and oxygen content. The moisture and oxygen contributions to insulation deterioration are minimized due to modern oil preservation systems. Therefore, temperature is the key parameter in insulation ageing. Temperature distribution is not uniform; the part with the highest temperature undergoes the greatest deterioration. Therefore the hottest spot temperature is considered in loss of life calculations.

2.19.1 Setting Guidelines

Set the life hours at reference hottest spot temperature. According to IEEE Std. C57.91-1995, the normal insulation life at the reference temperature in hours or years must be arbitrarily defined. The following table extracted from IEEE Std. C57.91-1995 gives values of normal insulation life for a well-dried, oxygen-free 65°C average winding temperature rise insulation system at the reference temperature of 110°C.

Basis	Normal insulation life	
	Hours	Years
50% retained tensile strength of insulation (former IEEE Std C57.92-1981 criterion)	65000	7.42
25% retained tensile strength of insulation	135000	15.41
200 retained degree of polymerization in insulation	150000	17.12
Interpretation of distribution transformer functional life test data (former IEEE Std. C57.91-1981)	180000	20.55

Notes: *Tensile strength or degree of polymerization (D.P.) retention values were determined by sealed tube aging on well-dried insulation samples in oxygen-free oil.*
Refer to I.2 in annex I of the IEEE Std. C57.91-1995 for discussion of the effect of higher values of water and oxygen and also for the discussion on the basis given above.

Table 14 - Normal insulation life based on different factors

The Designed HS temp should be set to 110°C if the transformer is rated 65°C average winding rise. If the transformer is rated 55°C average winding rise, set the Designed HS temp to 95°C.

As recommended by IEEE Std. C57.91-1995, the Constant B Set should be set to 15000 based on modern experimental data.

If the ageing acceleration factor calculated by the relay is greater than the setting **FAA> Set** and the time delay **tFAA> Set** has elapsed, the FAA alarm (DDB 479) would be activated.

If the loss of life calculated by the relay is greater than the setting **LOL>1 Set** and the time delay **tLOL> Set** has elapsed, the LOL alarm (DDB 480) would be activated.

The following is an example on how to set the loss of life function. Consider a new 65°C average winding rise rated transformer whose life hours at designed hottest spot temperature is 180,000 hrs. As a result, Life Hours at HS is set to 180,000, and the Designed HS temp is set to 110.0°C. The Constant B Set is 15,000 as recommended by IEEE from experimental data. The aging acceleration factor takes into consideration the constant B and the hottest spot temperature calculated by the thermal function. For a distribution transformer, IEEE suggests 200°C as the limit for the hottest spot temperature (refer to the thermal overload function to determine the hottest spot temperature for a power transformer). The aging acceleration factor alarm may be asserted when 70% of the 200°C is reached. The aging acceleration factor is calculated as follows:

$$FAA = e^{\left[\frac{B}{383} - \frac{B}{hottest-spot-tempt+273}\right]} = e^{\left[\frac{B}{383} - \frac{B}{0.7 \times 200+273}\right]} = 17.2$$

Therefore FAA>set is 17.2. The tFAA> Set may be set to 10.00 min. The LOL>1 Set may be set to 115,000 hrs, if it is considered that the transformer has 65,000 hrs left (Life Hours at HS – hours left = 180,000 – 65,000 = 115,000 hrs). The tLOL> Set may be set to 10.00 min. Finally the Reset Life Hours setting determines the value of the LOL measurement once the Reset LOL command is executed. The default value is zero because considering a new transformer, after testing the thermal function in the P64x, the LOL measurement should be reset to zero.

Certain tests should be performed to determine the age of an old transformer. Advice from the transformer manufacturer should be requested.

2.20 Through Fault Monitoring

According to IEEE Std C57.109-1993(R2008), mechanical effects are more significant than thermal effects for fault-current magnitudes near the design capability of the transformer. However, at fault-current magnitudes close to the overload range, mechanical effects are less important unless the frequency of fault occurrence is high. Note that mechanical effects are more important in large kVA transformers. The maximum duration limit for the worst case of mechanical duty is 2 s.

The IEEE Std C57.109-1993(R2008) indicates that the transformer categories are as follows:

Transformer Categories		
Category	**Single phase (kVA)**	**Three-phase (kVA)**
I	5 to 500	15 to 500
II	501 to 1667	501 to 5000
III	1668 to 10000	5001 to 30000
IV	Above 10000	Above 30000

Table 15 - Transformer Categories

Category I and II transformer maximum through fault current only considers the transformer short-circuit impedance. Category III and IV transformer maximum through fault current considers the transformer short-circuit impedance and the system short-circuit impedance at the transformer location. The short-circuit impedances are expressed in percent on the transformer rated voltage and rated base kVA.

The P64x through fault monitoring element can monitor the HV, the LV or the TV winding. In three winding applications, monitor the winding through which the highest current would flow during an external fault. Fault studies are required to determine the maximum through fault current and which winding carries the most current. For example, consider the autotransformer shown in Figure 24. Consider that an equivalent source and load are connected to the 230 kV terminal. Also an equivalent source and load are connected to the 115 kV terminal and only the load is connected to the 13.8 kV terminal. An external fault on the 230 kV side would be fed by the source on the 115 kV side. Therefore, the current would mainly flow from the 115 kV side to the 230 kV side. If the external fault occurs on the 115kV side, the through fault current would flow from the 230 kV side to the 115 kV side. If an external fault occurs on the 13.8 kV side, the through fault current would flow from the 230 kV and 115 kV sides to the 13.8 kV side. The source and transformer impedances determine the fault current level. Monitor the winding through which the maximum through fault current flows.

Set the **TF I> Trigger** above the maximum overload. According to IEEE Std. C57.109-1993, values of 3.5 or less times normal base current may result from overloads instead of faults. TF I> may be set to 3.85 pu. If the monitored current is above this level and no differential element has started, then the I^2t is calculated.

To set the **TF I^2t> Trigger**, consider the maximum through fault current and the maximum time duration. The maximum through fault current may be determined as 1/X, where X is the transformer impedance. This approximation is valid when the source is strong, so that its impedance is small compared to the transformer impedance. If the transformer has an impedance of 10%, the maximum through fault current may be calculated as $1/X = 1/0.1 = 10$ pu. Set **TF I^2t> Trigger** to $(10)^2 = 100$ pu. Therefore, if 10 pu flow through the transformer for 1 s, a through fault alarm is issued.

2.21 Current Loop Inputs and Outputs

2.21.1 Current Loop Inputs

Four analog (or current loop) inputs are provided for transducers with ranges of 0 to 1 mA, 0 to 10 mA, 0 to 20 mA or 4 to 20 mA. The analog inputs can be used for various transducers such as vibration monitors, tachometers and pressure transducers. Associated with each input there are two protection stages, one for alarm and one for trip. Each stage can be individually enabled or disabled and each stage has a definite time delay setting. The Alarm and Trip stages can be set for operation when the input value falls below the Alarm/Trip threshold ‘Under’ or when the input current is above the input value ‘Over’.

Power-on diagnostics and continuous self-checking are provided for the hardware associated with the current loop inputs.

For the 4 to 20 mA input range, a current level below 4 mA indicates that there is a fault with the transducer or the wiring. An instantaneous under current alarm element is available, with a setting range from 0 to 4 mA. This element controls an output signal (CLI1/2/3/4 I< Fail Alm, DDB 461-464) which can be mapped to a user defined alarm if required.

2.21.2 Setting Guidelines for Current Loop Inputs

For each analog input, the user can define the following:

- The current input range: 0 – 1 mA, 0 – 10 mA, 0 – 20 mA, 4 – 20 mA
- The analog input function and unit, this is in the form of a 16-character input label
- Analog input Minimum value (setting range from –9999 to 9999)
- Analog input Maximum value (setting range from –9999 to 9999)
- Alarm threshold, range within the maximum and minimum set values
- Alarm function - over or under
- Alarm delay
- Trip threshold, range within maximum and minimum set values
- Trip function - over or under
- Trip delay

Each current loop input can be selected as Enabled or Disabled as can the Alarm and Trip stage of each of the current loop input. The Alarm and Trip stages can be set for operation when the input value falls below the Alarm/Trip threshold ‘Under’ or when the input current is above the input value ‘Over’ depending on the application. One of four types of analog inputs can be selected for transducers with ranges of 0 to 1 mA, 0 to 10 mA, 0 to 20 mA or 4 to 20 mA.

The Maximum and Minimum settings allow the user to enter the range of physical or electrical quantities measured by the transducer. The settings are unit-less; however, the user can enter the transducer function and the unit of the measurement using the 16-character user defined CLI Input Label. For example, if the analog input is used to monitor a power measuring transducer, the appropriate text could be “Active Power (MW)”.

The alarm and trip threshold settings should be set within the range of physical or electrical quantities defined by the user. The relay will convert the current input value into its corresponding transducer measuring value for the protection calculation.

For example if the CLI Minimum is –1000 and the CLI Maximum is 1000 for a 0 to 10 mA input, an input current of 10 mA is equivalent to a measurement value of 1000, 5 mA is 0 and 1 mA is –800. If the CLI Minimum is 1000 and the CLI Maximum is -1000 for a 0 to 10 mA input, an input current of 10 mA is equivalent to a measurement value of –1000, 5 mA is 0 and 1 mA is 800. These values are available for display in the **CLIO Input 1/2/3/4** cells in the **MEASUREMENTS 3** menu. The top line shows the CLI Input Label and the bottom line shows the measurement value.

2.21.3 Current Loop Outputs

Four analog current outputs are provided with ranges of 0 to 1 mA, 0 to 10 mA, 0 to 20 mA or 4 to 20 mA, which can alleviate the need for separate transducers. These may be used to feed standard moving coil ammeters for analog indication of certain measured quantities or into a SCADA using an existing analog RTU.

The outputs can be assigned to any of the following relay measurements:

- Magnitudes of IA, IB, IC of every CT input
- Magnitudes of IA, IB, IC at HV, LV and TV sides of the transformer
- Magnitudes of IN Measured and IN Derived of every winding
- Magnitudes of I1, I2, I0 at HV, LV and TV sides of the transformer
- Magnitudes of VAB, VBC, VCA, VAN, VBN, VCN, VN Measured, VN Derived
- Magnitude of Vx
- VAN RMS, VBN RMS, VCN RMS
- Frequency
- CL Inputs 1-4
- RTD 1-10

The user can set the measuring range for each analog output. The range limits are defined by the Maximum and Minimum settings. This allows the user to “zoom in” and monitor a restricted range of the measurements with the desired resolution. For voltage, current quantities, these settings can be set in either primary or secondary quantities, depending on the **CLO1/2/3/4 Set Values** then **Primary** or **Secondary** setting associated with each current loop output.

Power-on diagnostics and continuous self-checking are provided for the hardware associated with the current loop outputs.

2.21.4 Setting Guidelines for Current Loop Outputs

Each current loop output can be selected as Enabled or Disabled. One of four types of analog output can be selected for transducers with ranges of 0 to 1 mA, 0 to 10 mA, 0 to 20 mA or 4 to 20 mA. The 4 to 20 mA range is often used so that an output current is still present when the measured value falls to zero. This is to give a fail safe indication and may be used to distinguish between the analog transducer output becoming faulty and the measurement falling to zero.

The Maximum and Minimum settings allow the user to enter the measuring range for each analog output. The range, step size and unit corresponding to the selected parameter is shown in the table in the Operations chapter, *P64x/EN OP*. This allows the user to “zoom in” and monitor a restricted range of the measurements with the desired resolution.

For voltage, current and power quantities, these settings can be set in either primary or secondary quantities, depending on the **CLO1/2/3/4 Set Values** then **Primary** or **Secondary** setting associated with each current loop output.

The relationship of the output current to the value of the measurand is of vital importance and needs careful consideration. Any receiving equipment must, of course, be used within its rating but, if possible, some kind of standard should be established.

One of the objectives must be to have the capability to monitor the voltage over a range of values, so an upper limit must be selected, typically 120%. However, this may lead to difficulties in scaling an instrument.

The same considerations apply to current transducers outputs and with added complexity to watt transducers outputs, where both the voltage and current transformer ratios must be taken into account.

Some of these difficulties do not need to be considered if the transducer is only feeding, for example, a SCADA outstation. Any equipment which can be programmed to apply a scaling factor to each input individually can accommodate most signals. The main consideration will be to ensure that the transducer is capable of providing a signal right up to the full-scale value of the input, that is, it does not saturate at the highest expected value of the measurand.

3 APPLICATION OF NON-PROTECTION FUNCTIONS

3.1 VT Supervision

The Voltage Transformer Supervision (VTS) feature is used to detect failure of the ac voltage inputs to the relay. This may be caused by internal voltage transformer faults, overloading, or faults on the interconnecting wiring to relays. This usually results in one or more VT fuses blowing. Following a failure of the ac voltage input there would be a misrepresentation of the phase voltages on the power system, as measured by the relay, which may result in
mal-operation.

The VTS logic in the relay is designed to detect the voltage failure, and automatically adjust the configuration of protection elements whose stability would otherwise be compromised. A time-delayed alarm output is also available.

There are three main aspects to consider regarding the failure of the VT supply:

- Loss of one or two phase voltages
- Loss of all three phase voltages under load conditions
- Absence of three phase voltages on line energization

3.1.1 Loss of One or Two Phase Voltages

The VTS feature within the relay operates on detection of negative phase sequence (nps) voltage without the presence of negative phase sequence current. This gives operation for the loss of one or two phase voltages. Stability of the VTS function is assured during system fault conditions, by the presence of nps current. The use of negative sequence quantities ensures correct operation even where three-limb or ‘V’ connected (open delta) VTs are used.

Negative Sequence VTS Element:

> The negative sequence thresholds used by the element are V2 = 10 V and I2 = 0.05 to 0.5 In settable (defaulted to 0.05 In).

3.1.2 Loss of all Three Phase Voltages Under Load Conditions

Under the loss of all three phase voltages to the relay, there will be no negative phase sequence quantities present to operate the VTS function. However, under such circumstances, a collapse of the three phase voltages will occur. If this is detected without a corresponding change in any of the phase current signals (which would be indicative of a fault), a VTS condition will be raised. In practice, the relay detects the presence of superimposed current signals, which are changes in the current applied to the relay. These signals are generated by comparison of the present value of the current with that exactly one cycle previously. Under normal load conditions, the value of superimposed current should therefore be zero. Under a fault condition a superimposed current signal will be generated which will prevent operation of the VTS.

The phase voltage level detectors are fixed and will drop off at 10 V and pickup at 30 V.

The sensitivity of the superimposed current elements is fixed at 0.1 In.

3.1.3 Absence of Three Phase Voltages On Line Energization

If a VT were inadvertently left isolated prior to line energization, incorrect operation of voltage dependent elements could result. The previous VTS element detected three phase VT failure by absence of all three phase voltages with no corresponding change in current. On line energization there will, however, be a change in current (as a result of load or line charging current for example). An alternative method of detecting 3-phase VT failure is therefore required on line energization.

The absence of measured voltage on all three phases on line energization can be as a result of two conditions. The first is a 3-phase VT failure and the second is a close up three phase fault. The first condition would require blocking of the voltage dependent function and the second would require tripping. To differentiate between these two conditions an overcurrent level detector **VTS I> Inhibit** is used which will prevent a VTS block from being issued if it operates. This element should be set in excess of any non-fault based currents on line energization (load, line charging current, transformer inrush current if applicable) but below the level of current produced by a close up 3-phase fault. If the line is now closed where a 3-phase VT failure is present the overcurrent detector will not operate and a VTS block will be applied. Closing onto a three phase fault will result in operation of the overcurrent detector and prevent a VTS block being applied.

This logic will only be enabled during a live line condition (as indicated by the relay’s pole dead logic) to prevent operation under dead system conditions, where no voltage will be present and the **VTS I> Inhibit** overcurrent element will not be picked up.

3.1.4 Setting the VT Supervision Element

The relay may respond as follows, on operation of any VTS element:

- VTS set to provide alarm indication only;
- Optional blocking of voltage dependent protection elements;
- Optional conversion of directional overcurrent elements to non-directional protection (available when set to Blocking mode only). These settings are found in the Function Links cell of the overcurrent protection.

A VTS indication will be given after the VTS Time Delay has expired. In the case where the VTS is set to indicate only the relay may potentially maloperate, depending on which protection elements are enabled. In this case the VTS indication will be given prior to the VTS time delay expiring if a trip signal is given.

Where a miniature circuit breaker (MCB) is used to protect the voltage transformer ac output circuits, it is common to use MCB auxiliary contacts to indicate a three phase output disconnection. It is possible for the VTS logic to operate correctly without this input. However, this facility has been provided for compatibility with various utilities current practices. Energizing an opto-isolated input assigned to MCB/VTS (DDB 874) on the relay will therefore provide the necessary block.

Where directional overcurrent elements are converted to non-directional protection on VTS operation, it must be ensured that the current pick-up setting of these elements is higher than full load current.

The **VTS I> Inhibit** or **VTS I2> Inhibit** elements are used to override a VTS block in event of a fault occurring on the system which could trigger the VTS logic. Once the VTS block has been established, however, then it would be undesirable for subsequent system faults to override the block. Therefore the VTS block will be latched after a user settable time delay VTS Time Delay. Once the signal has latched the resetting method is determined by a menu setting Manual or Auto. The first is manually using the front panel interface (or remote communications) provided the VTS condition has been removed. The second method is automatically when VTS Reset Mode is set to Auto mode, provided the VTS condition has been removed and the three phase voltages have been restored above the phase level detector settings for more than 240 ms.

The VTS I> Inhibit overcurrent setting is used to inhibit the voltage transformer supervision in the event of a loss of all three phase voltages caused by a close up 3-phase fault occurring on the system following closure of the CB to energize the line. This element should be set in excess of any non-fault based currents on line energization (load, line charging current, transformer inrush current if applicable) but below the level of current produced by a close up 3-phase fault.

This **VTS I2> Inhibit** NPS overcurrent setting is used to inhibit the voltage transformer supervision in the event of a fault occurring on the system with negative sequence current above this setting. The NPS current pick-up threshold must be set higher than the negative phase sequence current due to the maximum normal load unbalance on the system. This can be set practically at the commissioning stage, making use of the relay measurement function to display the standing negative phase sequence current, and setting at least 20% above this figure.

3.2 CT Supervision

The current transformer supervision feature is used to detect failure of one or more of the ac phase current inputs to the relay. Failure of a phase CT or an open circuit of the interconnecting wiring can result in incorrect operation of any current operated element. Additionally, interruption in the ac current circuits risks dangerous CT secondary voltages being generated.

3.2.1 Setting the CT Supervision Element

The positive sequence current in at least two current inputs exceeds the **CTS I1** setting. The **CTS I1** setting should be below the minimum load current of the protected object. Therefore, 10% of the rated current might be used.

The high set ratio of negative to positive sequence current, **CTS I2/I1>2**, should be set below the ratio of negative sequence to positive sequence current when the secondary circuit of any phase of any of the CT inputs is disconnected. For example, consider that balanced full load current is flowing and that the secondary of phase A CT1 is disconnected. The currents measured by the relay are:

$$I_A = 0$$

$$I_B = 1\angle -120^\circ \text{pu}$$

$$I_C = 1\angle -240^\circ \text{pu}$$

The positive and negative sequence currents are calculated as:

$$I_1 = \left|\frac{1}{3}\times\left(I_A + aI_B + a^2 I_C\right)\right| = \left|\frac{1}{3}\times\left(a\times 1\angle -120^\circ + a^2\times 1\angle -240^\circ\right)\right| = \frac{2}{3}$$

$$I_2 = \left|\frac{1}{3}\times\left(I_A + a^2 I_B + aI_C\right)\right| = \left|\frac{1}{3}\times\left(a^2\times 1\angle -120^\circ + a\times 1\angle -240^\circ\right)\right| = \frac{1}{3}$$

The ratio of negative to positive sequence current is 50%. A typical setting of 40% might be used.

The low set ratio of negative to positive sequence current, **CTS I2/I1> 1**, should be set above the maximum load unbalance. In practice, the levels of standing negative phase sequence current present on the system govern this minimum setting. This can be determined from a system study, or by making use of the relay measurement facilities at the commissioning stage. If the latter method is adopted, it is important to take the measurements during maximum system load conditions, to ensure that all single-phase loads are accounted for. A 20% setting might be used.

If the following information is recorded by the relay during commissioning:

Ifull load = 500 A

I2 = 50 A

Therefore I2/I1 ratio is given by I2/I1 = 50/500 = 0.1

To allow for tolerances and load variations a setting of 20% of this value may be typical. Therefore set CTS I2/I1>1 = 20%.

After the **CTS Time Delay** expires the CT Fail Alarm is asserted. The default setting of 2 sec is appropriate.

3.3 CT Input Exclusion

When a current input is excluded, the current associated to the input is set to zero. As a result, all the protection functions considering the current from the excluded input are not affected. The CT input exclusion might be useful during maintenance. In Figure 71, the adjacent isolators to CB1 are open and locked because of maintenance work on CB1.

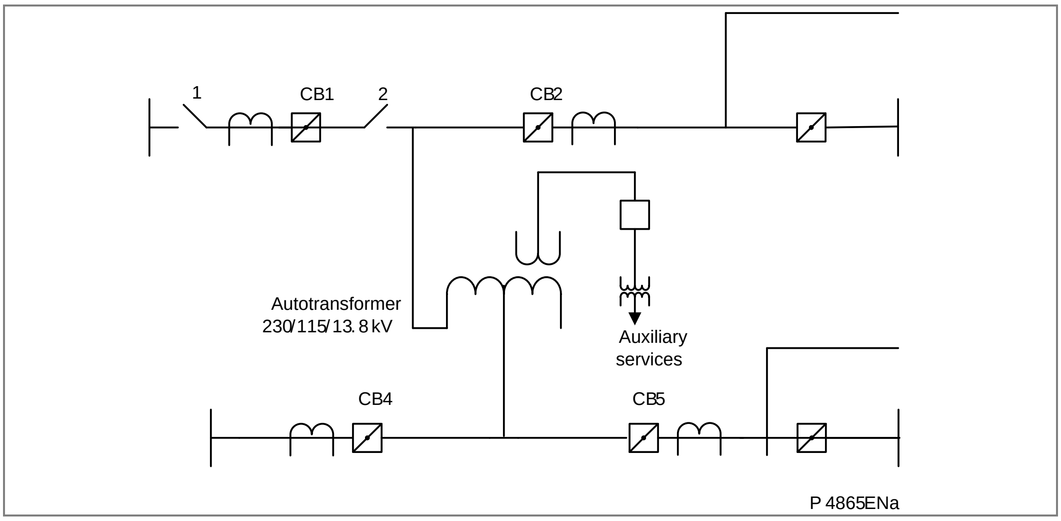

1
CB1
2
CB2
Autotransformer
230/115/13.8 kV
Auxiliary
services
CB4
CB5
P 4865ENa

Figure 71 - CT input exclusion – 1.5 Bk application

The current transformer associated to CB1 has been connected to T1 CT input in P645. As shown in Figure 72, auxiliary contacts from CB1 isolators 1 and 2 must be connected to an opto-input in P645 configured as CT1 Exclu Ena (DDB 704) in psl.

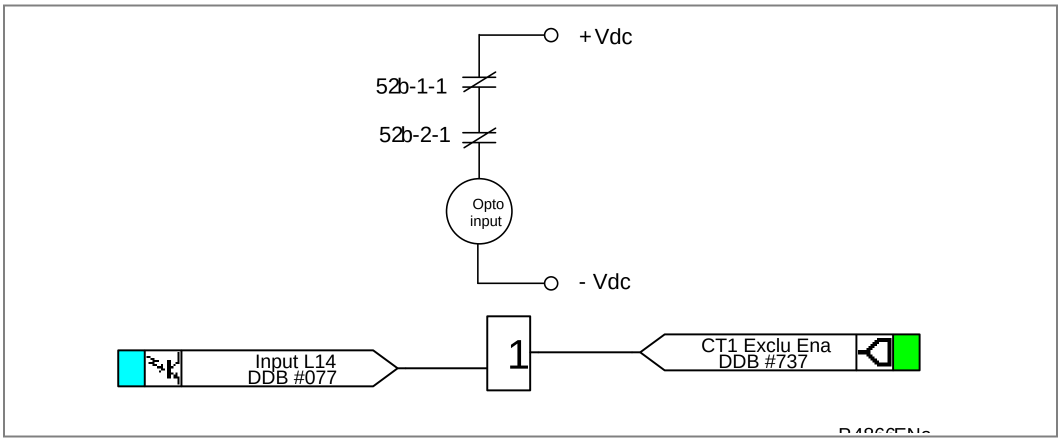
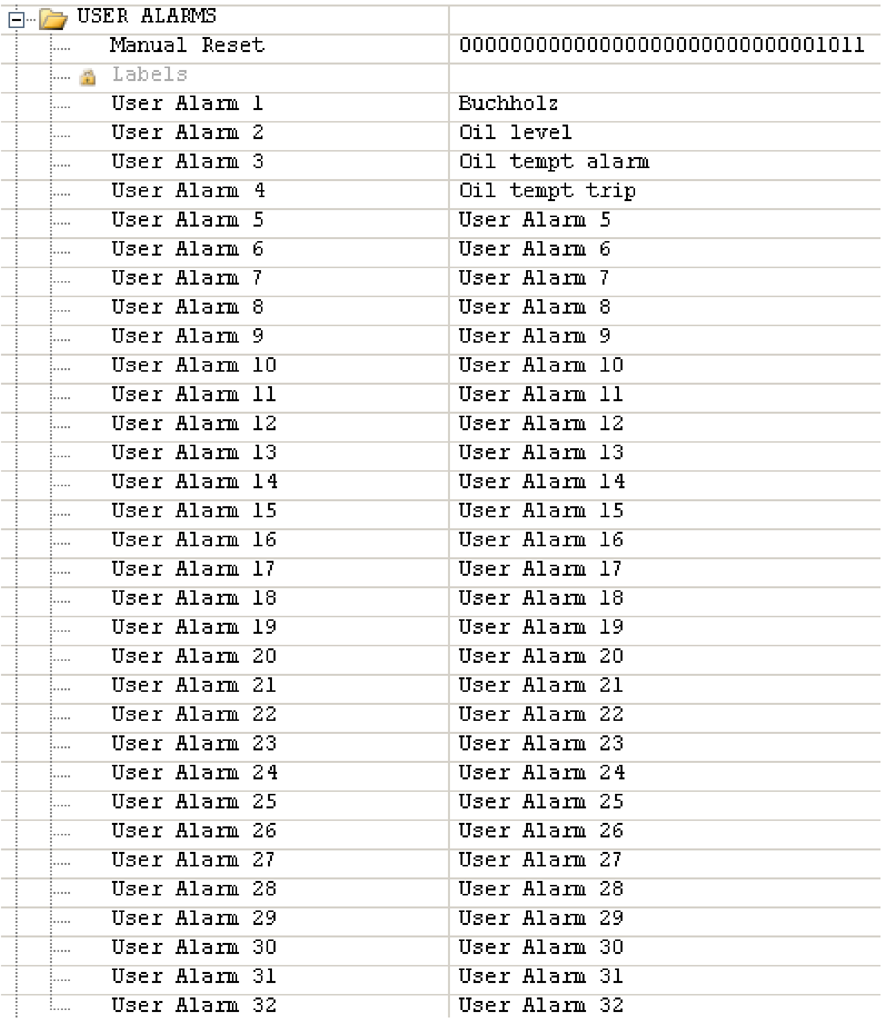

+Vdc
52b-1-1
52b-2-1
Opto
input
- Vdc
Input L14
DDB #077
1
CT1 Exclu Ena
DDB #737

Figure 72 - CT input exclusion

When isolators 1 and 2 are open the opto-input L14 is energized and CT1 Exclu Ena is asserted. To set T1 CT excluded (DDB 704), T1 CT Phase A, B and C undercurrent elements must also be asserted.

3.4 User Alarms

Thirty-two configurable self-reset or manual reset user alarms are available in the P64x. Transformer protection such as Buchholz, temperature, oil level can be configured to a user alarm as follows:



USER ALARMS	
Manual Reset	00000000000000000000000000001011
Labels	
User Alarm 1	Buchholz
User Alarm 2	Oil level
User Alarm 3	Oil tempt alarm
User Alarm 4	Oil tempt trip
User Alarm 5	User Alarm 5
User Alarm 6	User Alarm 6
User Alarm 7	User Alarm 7
User Alarm 8	User Alarm 8
User Alarm 9	User Alarm 9
User Alarm 10	User Alarm 10
User Alarm 11	User Alarm 11
User Alarm 12	User Alarm 12
User Alarm 13	User Alarm 13
User Alarm 14	User Alarm 14
User Alarm 15	User Alarm 15
User Alarm 16	User Alarm 16
User Alarm 17	User Alarm 17
User Alarm 18	User Alarm 18
User Alarm 19	User Alarm 19
User Alarm 20	User Alarm 20
User Alarm 21	User Alarm 21
User Alarm 22	User Alarm 22
User Alarm 23	User Alarm 23
User Alarm 24	User Alarm 24
User Alarm 25	User Alarm 25
User Alarm 26	User Alarm 26
User Alarm 27	User Alarm 27
User Alarm 28	User Alarm 28
User Alarm 29	User Alarm 29
User Alarm 30	User Alarm 30
User Alarm 31	User Alarm 31
User Alarm 32	User Alarm 32

P2681ENa

Figure 73 - User alarm settings

Buchholz, temperature and oil level trips can be executed by the P64x if the user alarm is configured to the any trip signal (DDB 886) as follows:

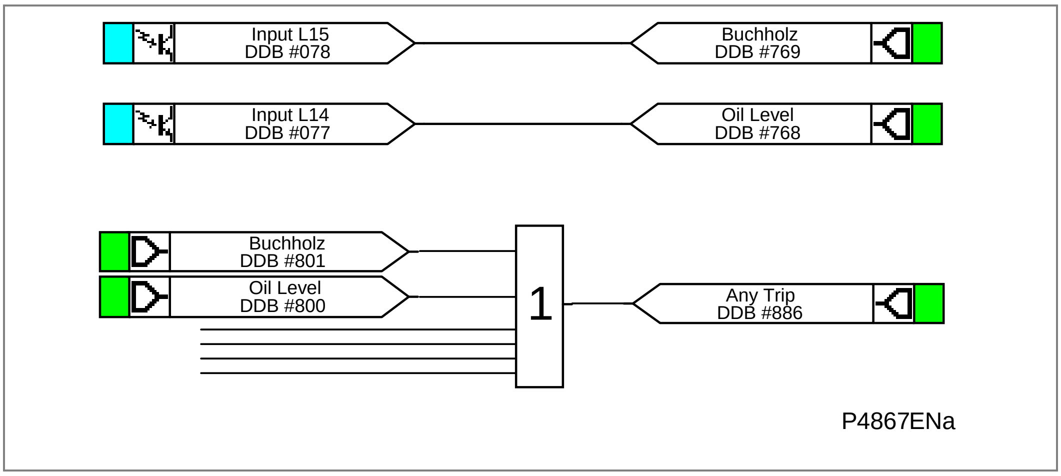

Input L15
DDB #078
Buchholz
DDB #769
Input L14
DDB #077
Oil Level
DDB #768
Buchholz
DDB #801
Oil Level
DDB #800
1
Any Trip
DDB #886
P4867ENa

Figure 74 - User alarm configuration

DDBs 768 and 800 are user alarm 1 output and input signal respectively. Both signals have been labeled as Oil Level in the setting file. Whenever opto-input 14 is energized DDB 768 is asserted. The user alarm output always follows the status of the signal configured to it in psl. In this example, DDB 768 follows the status of opto-input 14 and DDB 769 follows the status of opto-input 15. If user alarm 1 is set as manual reset, then DDB 800 is latched but DDB 768 is not. Similarly if user alarm 2 is set as manual reset, DDB 801 is latched but DDB 769 is not.

3.5 Trip Circuit Supervision (TCS)

The trip circuit, in most protective schemes, extends beyond the relay enclosure and passes through components such as fuses, links, relay contacts, auxiliary switches and other terminal boards. This complex arrangement, coupled with the importance of the trip circuit, has led to dedicated schemes for its supervision.

Several TCS schemes with various features can be produced with the P64x range. Although there are no dedicated settings for TCS, in the P64x, the following schemes can be produced using the Programmable Scheme Logic (PSL). A user alarm is used in the PSL to issue an alarm message on the relay front display. If necessary, the user alarm can be renamed using the menu text editor to indicate that there is a fault with the trip circuit.

3.5.1 TCS Scheme 1

3.5.1.1 Scheme Description

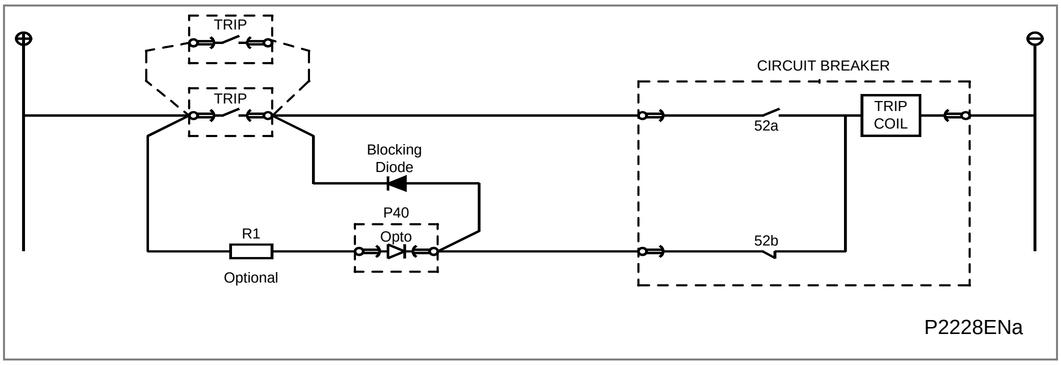

TRIP
TRIP
CIRCUIT BREAKER
52a
TRIP
COIL
Blocking
Diode
P40
Opto
R1
Optional
52b
P2228ENa

Figure 75 - TCS scheme 1

This scheme provides supervision of the trip coil with the breaker open and the trip path with the breaker closed, or closed, however, pre-closing supervision is not provided. This scheme is also incompatible with latched trip contacts, as a latched contact will short out the opto for greater than the recommended DDO timer setting of 400 ms. If breaker status monitoring is required, a further 1 or 2 opto inputs must be used.

Note	*A 52a CB auxiliary contact follows the CB position and a 52b contact is the opposite.*

When the breaker is closed, supervision current passes through the opto input, blocking diode and trip coil. When the breaker is open current still flows through the opto input and into the trip coil through the 52b auxiliary contact.

No supervision of the trip path is provided while the breaker is open, but the trip coil is supervised. Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

Resistor R1 is an optional resistor that can be fitted to prevent mal-operation of the circuit breaker if the opto input is inadvertently shorted, by limiting the current to <60 mA. The resistor should not be fitted for auxiliary voltage ranges of 30/34 volts or less, as satisfactory operation can no longer be guaranteed. The table below shows the appropriate resistor value and voltage setting (from the **OPTO CONFIG** menu) for this scheme.

This TCS scheme will function correctly even without resistor R1, since the opto input automatically limits the supervision current to less that 10 mA. However, if the opto is accidentally shorted the circuit breaker may trip.

Auxiliary voltage (Vx)	Resistor R1 (ohms)	Opto voltage setting with R1 fitted
24/27	-	-
30/34	-	-
48/54	1.2k	24/27
110/250	2.5k	48/54
220/250	5.0k	110/125

Table 16 - Auxiliary voltage, Resistor R1 and Opto voltage setting

Note	*When R1 is not fitted, the opto voltage setting must be set equal to the supply voltage of the supervision circuit.*

3.5.2 Scheme 1 PSL

Figure 76 shows the scheme logic diagram for the TCS scheme 1. Any of the available opto inputs can be used to indicate whether or not the trip circuit path or trip coil is healthy. The delay on drop off timer operates as soon as the opto is energized, but will take 400 ms to drop off/reset in the event of a trip circuit failure. The 400 ms delay prevents a false alarm due to voltage dips caused by faults in other circuits or during normal tripping operation when the opto input is shorted by a self-reset trip contact. When the timer is operated the NC (normally closed) output relay opens and the LED and user alarms are reset.

The 50 ms delay on pick-up timer prevents false LED and user alarm indications during the relay power up time, following an auxiliary supply interruption.

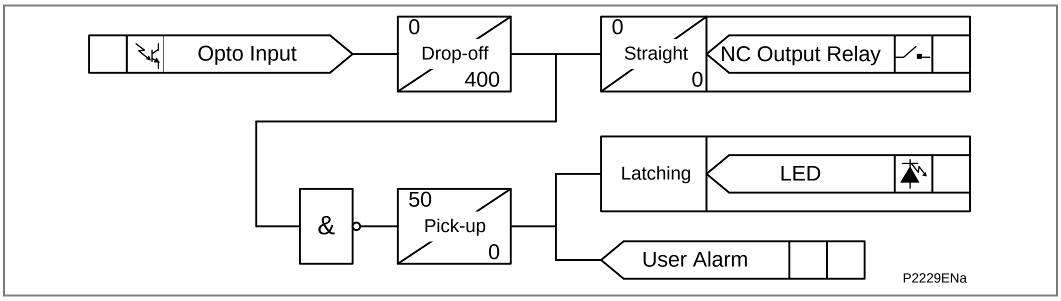

Opto Input
0
Drop-off
400
0
Straight
0
NC Output Relay
Latching
LED
&
50
Pick-up
0
User Alarm
P2229ENa

Figure 76 - PSL for TCS schemes 1 and 3

3.5.3 TCS Scheme 2

3.5.3.1 Scheme Description

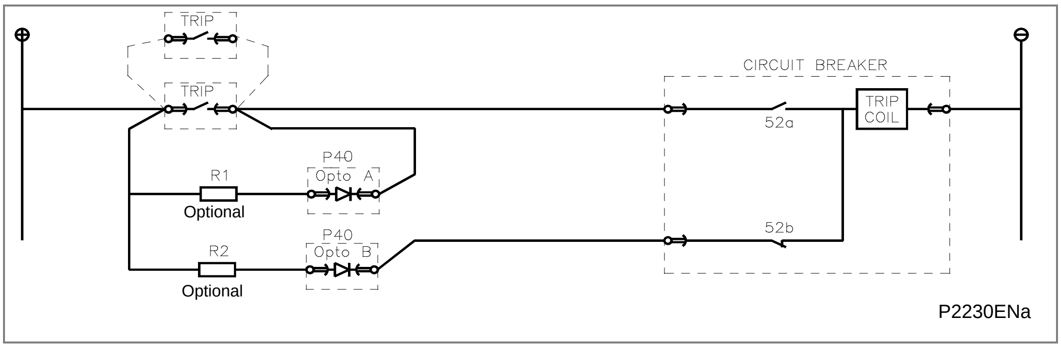

TRIP
TRIP
CIRCUIT BREAKER
TRIP COIL
52a
R1
Optional
P40
Opto A
R2
Optional
P40
Opto B
52b
P2230ENa

Figure 77 - TCS scheme 2

Much like scheme 1, this scheme provides supervision of the trip coil with the breaker open and of the trip path with the breaker closed. It also does not provide pre-closing supervision. However, using two opto inputs allows the relay to correctly monitor the circuit breaker status since they are connected in series with the CB auxiliary contacts. This scheme is also fully compatible with latched contacts as the supervision current will be maintained through the 52b contact when the trip contact is closed.

When the breaker is closed, supervision current passes through opto input A and the trip coil. When the breaker is open current flows through opto input B and the trip coil. As with scheme 1, no supervision of the trip path is provided whilst the breaker is open but the trip coil is supervised. Any fault in the trip path will only be detected on CB closing, after a 400 ms delay.

As with scheme 1, optional resistors R1 and R2 can be added to prevent tripping of the CB if either opto is shorted. The resistor values of R1 and R2 are equal and can be set the same as R1 in scheme 1.

3.5.4 Scheme 2 PSL

The PSL for this scheme (Figure 78) is practically the same as that of scheme 1. The main difference being that both opto inputs must be off before a trip circuit fail alarm is given.

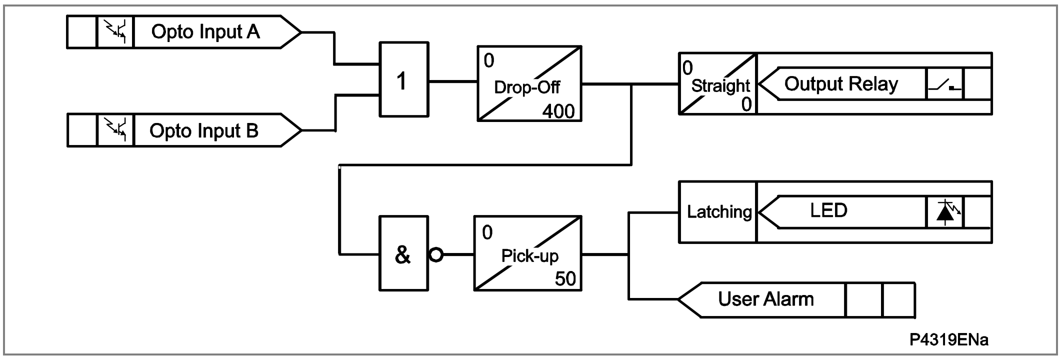

Opto Input A
Opto Input B
1
0
Drop-Off
400
0
Straight
0
Output Relay
&
0
Pick-up
50
Latching
LED
User Alarm
P4319ENa

Figure 78 - PSL for TCS scheme 2

3.5.5 TCS Scheme 3

3.5.5.1 Scheme Description

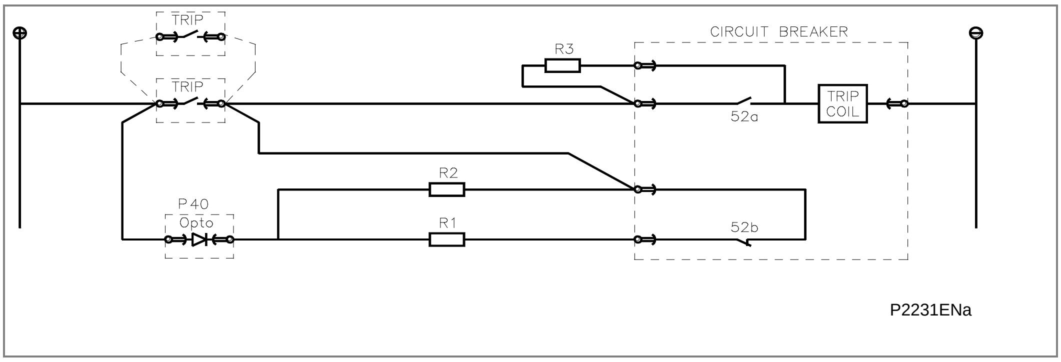

TRIP
TRIP
R3
CIRCUIT BREAKER
52a
TRIP COIL
R2
P40
Opto
R1
52b
P2231ENa

Figure 79 - TCS scheme 3

Scheme 3 is designed to provide supervision of the trip coil with the breaker open or closed, but unlike schemes 1 and 2, it also provides pre-closing supervision. Since only one opto input is used, this scheme is not compatible with latched trip contacts.

When the breaker is closed, supervision current passes through the opto input, resistor R2 and the trip coil. When the breaker is open current flows through the opto input, resistors R1 and R2 (in parallel), resistor R3 and the trip coil. Unlike schemes 1 and 2, supervision current is maintained through the trip path with the breaker in either state, therefore giving pre-closing supervision.

As with schemes 1 and 2, resistors R1 and R2 are used to prevent false tripping, if the opto-input is accidentally shorted. However, unlike the other two schemes, this scheme is dependent on the position and value of these resistors. Removing them would result in incomplete trip circuit monitoring. The table below shows the resistor values and voltage settings required for satisfactory operation.

Auxiliary voltage (Vx)	Resistor R1 & R2 (ohms)	Resistor R3 (ohms)	Opto voltage setting
24/27	-	-	-
30/34	-	-	-
48/54	1.2k	0.6k	24/27
110/250	2.5k	1.2k	48/54
220/250	5.0k	2.5k	110/125

Table 17 - Resistor values and voltage settings required

Note	*Scheme 3 is not compatible with auxiliary supply voltages of 30/34 volts and below.*

3.5.6 Scheme 3 PSL

The PSL for scheme 3 is identical to that of scheme 1 (see Figure 76).

3.6 VT Connections

3.6.1 Open Delta (V-Connected) VTs

The P642/P643/P645 relay can be used with V-connected VTs by connecting the VT secondaries to C2, C4 and E2 input terminals, Vn is left open (see the wiring diagrams in the *Installation* chapter *P64x/EN IN*).

This type of VT arrangement cannot pass zero-sequence (residual) voltage to the relay, or provide any phase to neutral voltage quantities. Therefore any protection that is dependent on zero sequence voltage measurements should be disabled. Therefore, residual voltage displacement protection and directional earth fault protection should be disabled.

The accuracy of single-phase voltage measurements can be impaired when using V-connected VTs. The relay attempts to derive the phase to neutral voltages from the phase to phase voltage vectors. If the impedance of the voltage inputs were perfectly matched the phase to neutral voltage measurements would be correct, provided the phase to phase voltage vectors were balanced. However, in practice there are small differences in the impedance of the voltage inputs, which can cause small errors in the phase to neutral voltage measurements.

The phase to neutral voltage measurement accuracy can be improved by connecting three well-matched load resistors between the phase voltage inputs (C2, C4, E2) and neutral (C4,C3,E1), creating a ‘virtual’ neutral point. The load resistor values must be chosen so their power consumption is within the limits of the VT. It is recommended that 10kΩ ±1% (6 W) resistors are used for the 110 V (Vn) rated relay, assuming the VT can supply this burden.

3.6.2 VT Single Point Earthing

The P64x range will function correctly with conventional three-phase VTs earthed at any one point on the VT secondary circuit. Typical earthing examples are neutral earthing and yellow phase earthing.

4 CURRENT TRANSFORMER REQUIREMENTS

4.1 Current Transformer Theory

The flow current in the primary winding produces an alternating flux in the core and this flux induces an e.m.f. in the secondary winding which results in the flow of secondary current when this winding is connected to an external closed circuit. The magnetic effect of the secondary current is in opposition to that of the primary and the value of the secondary current automatically adjusts itself to such a value, that the resultant magnetic effect of the primary and secondary currents, produces a flux required to induce the e.m.f. necessary to drive the secondary current through the impedance of the secondary. In an ideal transformer, the primary ampere-turns are always exactly equal to the secondary ampere-turns and the secondary current is, therefore, always proportional to the primary current. In an actual current transformer, however, this is never the case. All core materials require a certain number of ampere-turns to induce the magnetic flux required to induce the necessary voltage. The most accurate current transformer is one in which the exciting ampere-turns are least in proportion to the secondary ampere-turns.

In many applications, core saturation will almost inevitably occur during the transient phase of a heavy short circuit. The performance of the current transformers during faults is, therefore, an important consideration in providing an effective relaying scheme. In any current transformer the first consideration is the highest secondary winding voltage possible prior to core saturation.

This may be calculated from:

$Ek = 4.44 \times B\ A\ f\ N$ volts

Where:
Ek = secondary induced volts (rms value, known as the knee-point voltage)
B = flux density in tesla
N = number of secondary turns
f = system frequency in hertz
A = net core cross-sectional area in square meters

This induced voltage causes the maximum current to flow through the external burden while still maintaining a virtually sinusoidal secondary current. Any higher value of primary current demanding further increase in secondary current would, due to core saturation, tend to produce a distorted secondary current.

The circuit voltage required is typically:

$Es = Is\ (Z_B + Z_S + Z_L)$

Where:
Is = secondary current of ct in amps (assume nominal value, usually 1 A or 5 A)
Z_B = the connected external burden in ohms
Z_S = the ct secondary winding impedance in ohms
Z_L = the resistance of any associated connecting leads

In any given case, several of these quantities are known or can usually be estimated to predict the performance of the transformers. From the ac magnetization characteristic, commonly plotted in secondary volts versus exciting current, Es can be determined for a minimum exciting current. The equation for Es given above then indicates whether the voltage required is adequate. It may be seen that the secondary burden and the maximum available fault current are two important criteria in determining the performance of a given current transformer.

The primary current contains two components. These are respectively the secondary current which is transformed in the inverse ratio of the turns ratio and an exciting current, which supplies the eddy and hysteresis losses and magnetizes the core. This latter current flows in the primary winding only and therefore, is the cause of the transformer errors. It is, therefore, not sufficient to assume a value of secondary current and to work backwards to determine the value of primary current by invoking the constant ampere-turns rule, since this approach does not take into account the exciting current. From this observation it may be concluded that certain values of secondary current could never be produced whatever the value of primary current and this is of course, the case when the core saturates and a disproportionate amount of primary current is required to magnetize the core.

The amount of exciting current drawn by a current transformer depends on the core material and the amount of flux which must be developed in the core to satisfy the burden requirements of the current transformer. The appropriate current may be obtained directly from the exciting characteristic of the transformer since the secondary e.m.f. and therefore the flux developed is proportional to the product of secondary current and burden impedance.

The general shape of the exciting characteristic for a typical grade of CROSS core (cold rolled grain orientated silicon steel) is shown in Figure 80. The characteristic is divided into three regions, defined by ankle-point and the knee-point. The working range of a protective current transformer extends over the full range between the ankle-point and the knee-point and beyond. Protection current transformers are required to operate correctly at many times the rated current.

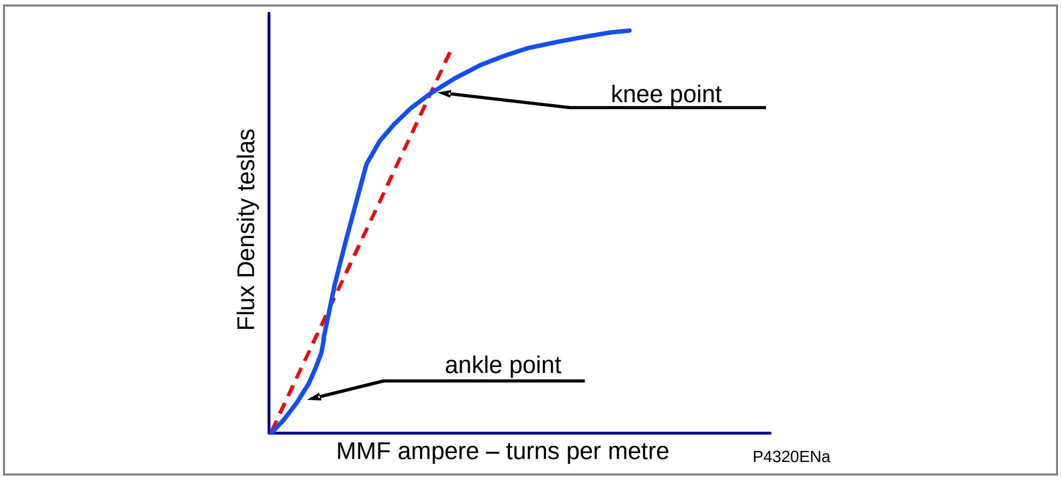


Figure 80 - Exciting characteristic for a CROSS core CT

The current transformer requirements for each current input will depend on the protection function with which they are related and whether the line current transformers are being shared with other current inputs. Where current transformers are being shared by multiple current inputs, the knee-point voltage requirements should be calculated for each input and the highest calculated value used.

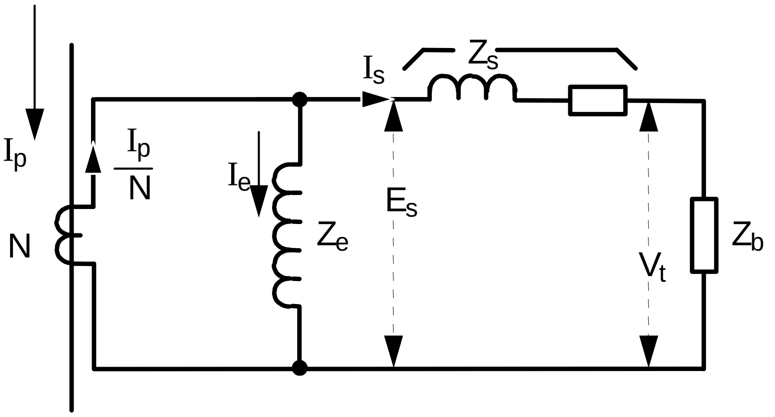
IEC defines the knee-point of the excitation characteristic as the point at which a 10% increase in secondary voltage produces a 50% increase in exciting current. It may, therefore, be regarded as practical limit beyond which a specified current ratio may be maintained.

The current transformer magnetization curve, is usually expressed in terms of Kv, (Kv = Es/B), and Ki, (Ki = L/N, where L is the mean magnetic path) which when multiplied by the flux density in teslas and ampere-turns per m respectively gives corresponding volts and amperes.

⚠ **Caution** **The secondary circuit of a current transformer should never be left open-circuited while primary continues to flow. In these circumstances only the primary winding is effective so the current**

transformer behaves as a highly saturated choke (induction) to the flow of primary winding current. Therefore a peaky and relatively high value of voltage appears at the secondary output of terminals, endangering life, not to mention the possible resulting breakdown of secondary circuit insulation.

The errors of a current transformer may be considered as due to the whole of the primary current not being transformed, a component of which being required to excite the core. Alternatively, as shown in Figure 81, we may consider that the whole of the primary current is transformed without loss but that the secondary current is shunted by a parallel circuit. The impedance of this parallel circuit is such that the equivalent of the exciting current flows through it. The circuit shown is the equivalent circuit of the current transformer. The primary current is assumed to be transformed perfectly, with no ratio or phase single error, to a current IP/N which is often called 'the primary current referred to the secondary'. A part of the current may be considered consumed in exciting the core and this current Ie is called the secondary excitation current. The remainder Is is a true secondary current. It will be evident that the excitation current is a function of the secondary excitation voltage Es and the secondary excitation impedance Ze. It will also be evident that the secondary current is a function of Es and the total impedance in the secondary circuit. This total impedance consists of the effective resistance (and any leakage reactance) of the secondary winding and the impedance of the burden.



I_p = primary current in amperes
N = current transformer ratio (primary to secondary amperes)
Z_b = burden impedance of relays in ohms (r + jx)
Z_s = current transformer secondary winding impedance in ohms (r + jx)
Z_e = secondary excitation impedance in ohms (jx)
I_e = secondary excitation current in amperes
I_s = secondary current in amperes
E_s = secondary excitation voltage in volts
V_t = secondary terminal voltage in volts across the current transformer terminals (input to the relay or burden)

P4321ENa

Figure 81 - CT equivalent circuit

4.1.1 Steady CT Saturation

Consider the simplified CT equivalent circuit shown in Figure 82. The excitation branch is represented by a switch that closes when the CT is saturated and opens when the CT is not saturated. Therefore, during saturation no current flows through the CT secondary circuit as it is effectively shorted. It also assumes that the primary load is purely resistive.

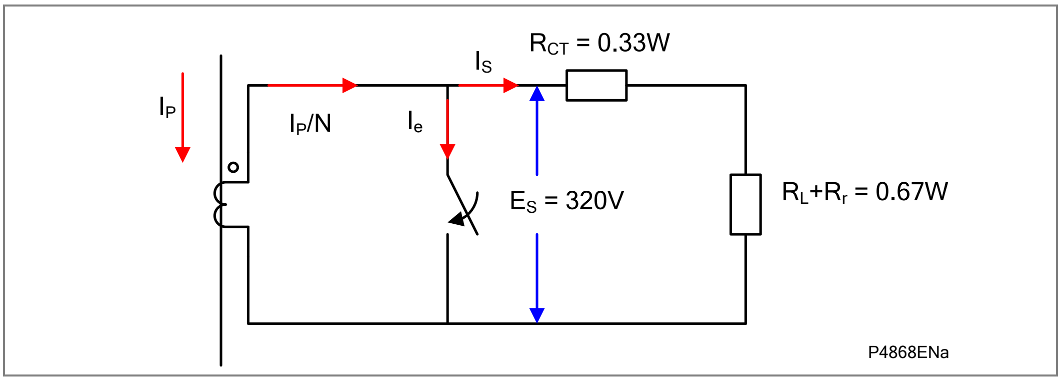


Figure 82 - Simplified CT equivalent circuit

The CT ratio is 800:5, 320 V knee point voltage, 0.33 Ω secondary winding resistance and the secondary winding turns is 160. Consider that the burden (leads and relay) connected to the CT secondary terminals is 0.67 Ω; the total burden is 0.33 Ω + 0.67 Ω = 1 Ω.

Consider that during full load, 5 A flows through the CT secondary circuit. Es is 5 V, therefore the CT operates in the linear region of the magnetizing characteristic shown in Figure 85.

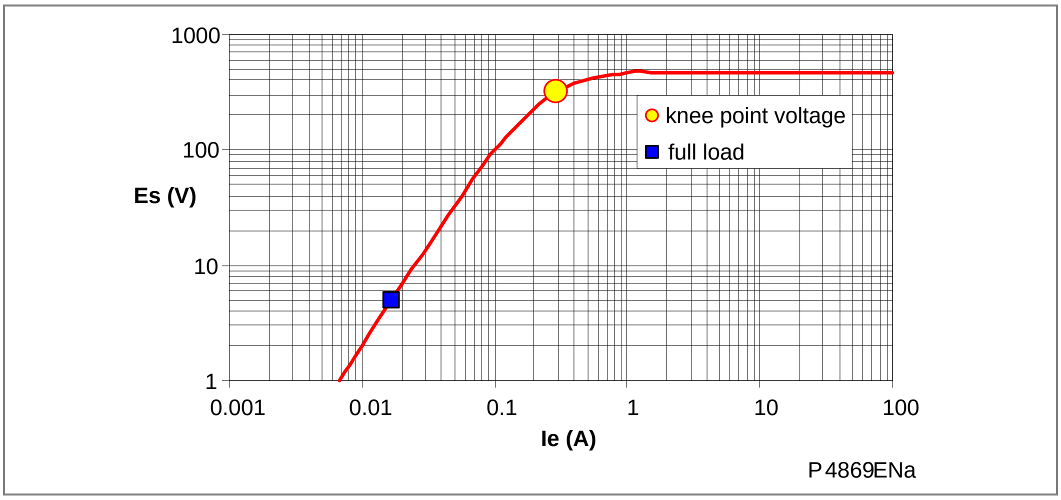


Figure 83 - CT exciting characteristic

The maximum steady state undistorted sinusoidal secondary current that may flow through the CT secondary circuit is Is = V/R = 320/1 = 320A. This corresponds to 320 × 160 = 51.2 kA primary current. 51.2 kA flowing through the CT primary circuit generates the required flux to induced E_S = 320 V in the CT secondary circuit.

The steady state primary current, secondary current, voltage and flux waveforms are as shown in Figure 84 and Figure 85. Note that the maximum change in flux is 17.86 mWb. The flux is the area below the voltage waveform divided by the secondary turns, i.e.

$\phi(t) = \int \frac{Es}{N} dt$.

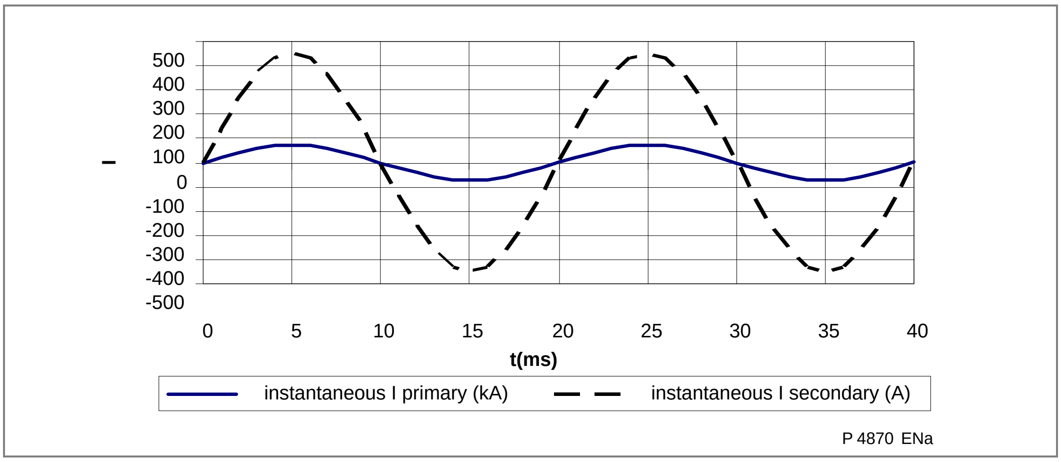


Figure 84 - Primary and secondary current waveforms at the knee point voltage

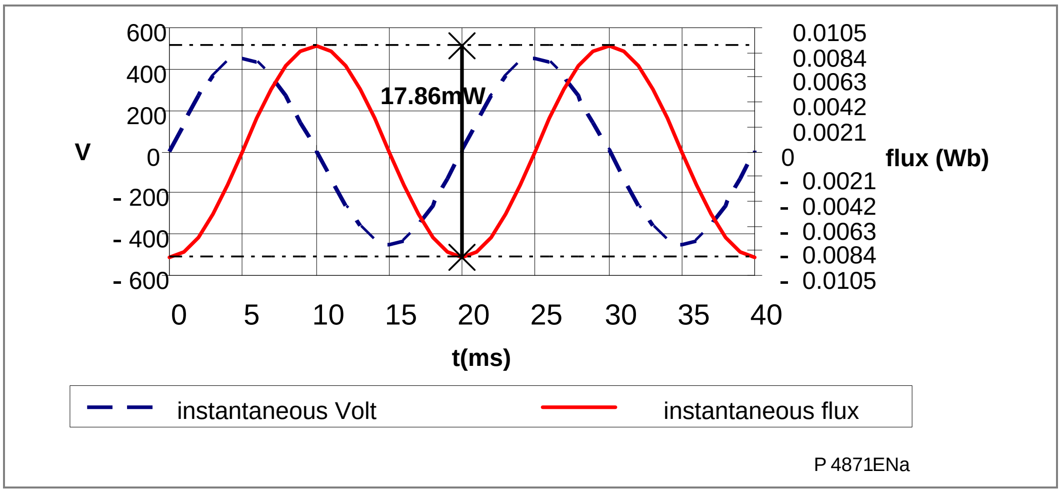


Figure 85 - CT voltage and flux waveforms at the knee point voltage

In this example, the flux must be within -8.93 mWb and 8.93 mWb to avoid saturation. If the primary current is greater than 51.2 kA, then the flux would be outside this range. Increasing the primary current to twice its value considering the simplified CT circuit increases the flux to twice its steady state value. The CT core saturates if the flux ≥ 8.93 mWb or flux ≤ -8.93 mWb. Considering the simplified CT equivalent circuit, during saturation the switch closes, as a result Es and Is collapse to zero where they remain until next primary current zero is reached. This process is repeated each half cycle and results in a pulse secondary current, voltage and flux waveforms as shown in Figure 86 and Figure 87.

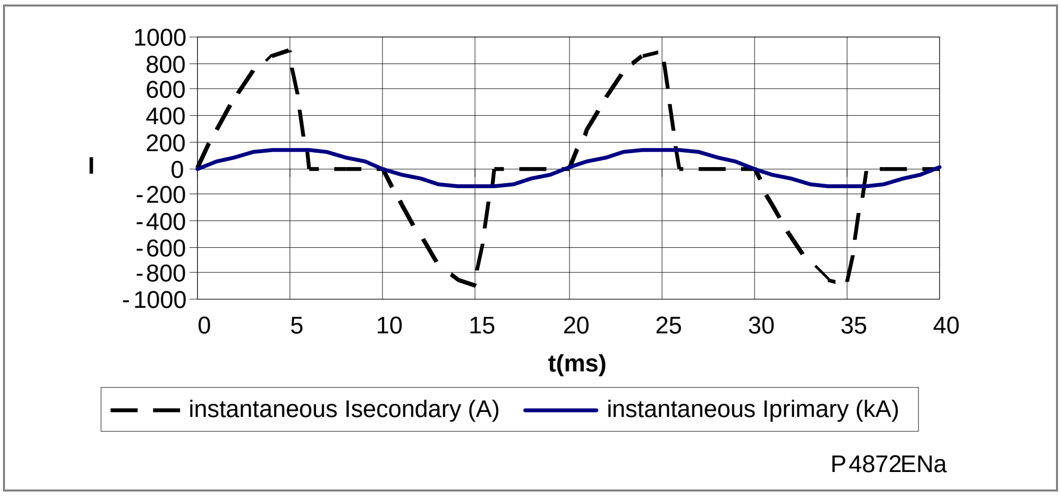


Figure 86 - Primary and secondary current waveforms – I_P = 102.4 kA

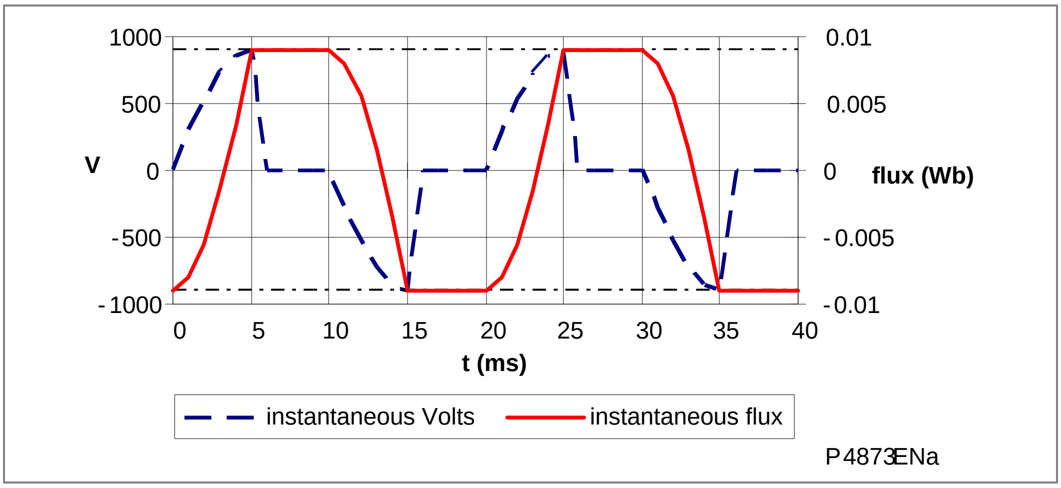


Figure 87 - Voltage and flux waveforms – I_P = 102.4 kA

4.1.2 Transient CT Saturation

Consider a primary system having and equivalent impedance equal to $Z\angle\phi$. V represents the voltage applied to the system and IP is the primary current flowing through the system. The primary current contains an AC and a DC component. The AC component is responsible for steady state CT saturation and the DC component for transient CT saturation.

The DC component is $I_P = -\frac{V_m}{Z} \times \sin(\theta - \phi) e^{-\frac{t}{\tau}}$

The AC component is $I_P = \frac{V_m}{Z} \times \sin(\omega t + \theta - \phi)$

$$V = V_m \times \sin(\omega t + \theta)$$

$$I_P = \frac{V_m}{Z}\left[\sin(\omega t + \theta - \phi) - \sin(\theta - \phi)e^{-\frac{t}{\tau}}\right]$$

$\theta = \text{angle of the voltage waveform at } t = 0\text{s}$

$Z = \text{primary system impedance}$

$$\tau = \frac{L}{R} = \frac{X_L}{2\pi f R}$$

$$\phi = \tan^{-1}\left(\frac{X_L}{R}\right)$$

Consider the same CT used in section 4.1.1 Steady state CT saturation.

$I_P = 8000 \times \sqrt{2} \times \left[\sin(\omega t - \frac{\pi}{2}) + e^{-\frac{t}{0.064}}\right]$ is shown in Figure 88. In this example, X/R is 20 and the maximum DC component is considered. The maximum DC component occurs when $\sin(\theta - \phi) = \pm 1$.

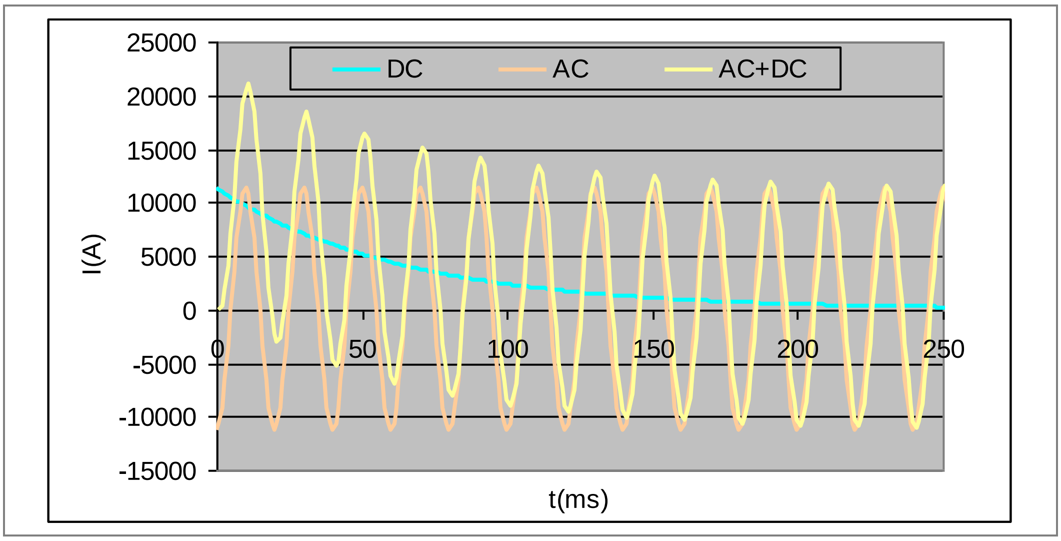


Figure 88 - Primary current – maximum DC offset

Consider that the magnetizing inductance is infinite and the CT ratio is 160; therefore the secondary current is as follows:

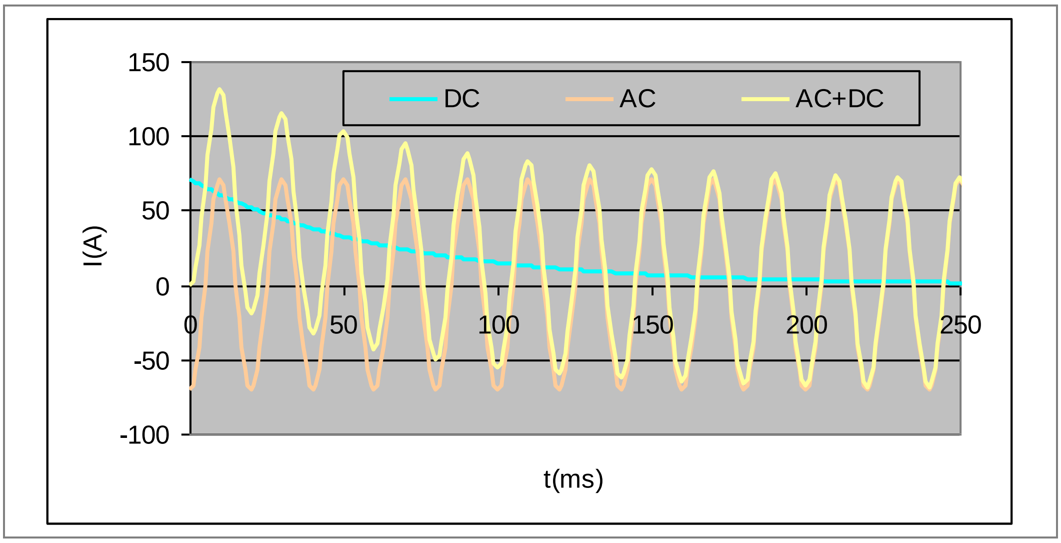


Figure 89 - Secondary current – infinite magnetizing inductance

Consider that the total secondary burden is resistive and equal to 1Ω, the voltage required to drive the secondary current shown in Figure 89 is as follows:

$$V = \frac{8000 \times \sqrt{2}}{160} \times R_{burden} \times \left[\sin(\omega t - \frac{\pi}{2}) + e^{-\frac{t}{0.064}} \right] = 70.7 \left[\sin(\omega t - \frac{\pi}{2}) + e^{-\frac{t}{0.064}} \right]$$

The total flux is calculated as $\phi(t) = 0.44 \left[\frac{-\cos(\omega t - \frac{\pi}{2})}{\omega} - 0.064 \times e^{-\frac{t}{0.064}} \right]$

The flux AC component is $\phi(t) = 0.44 \left[\frac{-\cos(\omega t - \frac{\pi}{2})}{\omega} \right]$

The flux DC component is $\phi(t) = 0.44 \left[-0.064 \times e^{-\frac{t}{0.064}} \right]$

The flux waveforms are shown in Figure 90 below. It can be observed the flux required to drive the current DC component is 20 times greater than the flux required to drive the current AC component.

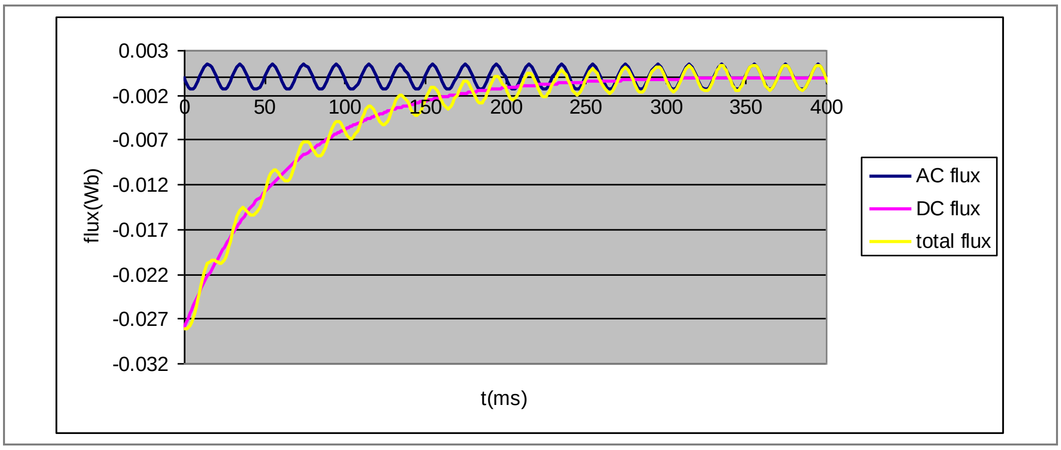


Figure 90 - Flux AC and DC components

The CT described in section 4.1.1 Steady state CT saturation will saturate under the flux DC component shown in Figure 90.

4.1.3 CT Errors

Table 18 shows the limits of error for protection CTs. At rated frequency and with rated burden connected the current error, phase displacement and composite error shall not exceed the values given in the table. For test purposes, when determining the current error and phase displacement, the burden shall have a power factor of 0.8 inductive except where the burden is less than 5 VA a power factor of 1.0 is permissible.

Limits of error for protection CTS				
Accuracy class	**Current error at rated primary Current (%)-**	**Phase displacement at rated primary current**		**Composite error at rated accuracy**
		Minutes	**Centiradians**	**Limit primary current (%)**
5P	± 1	± 60	± 1.8	5
10P	± 3			10

Table 18 - Limits of error for protection CTS

Considering the excitation impedance (Ze) as a constant, the vectorial relationships between Ip and Is is Ie. Ic constitutes the current error and Iq the component of Ie in quadrature with Is which results in the phase difference. This is shown in Figure 91.

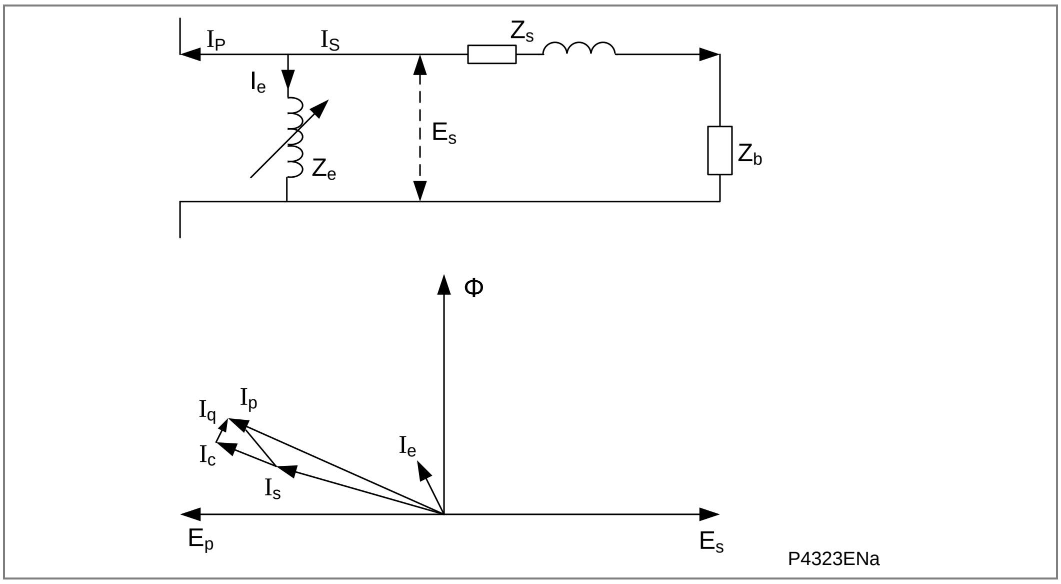


Figure 91 - CT error

If Ze was in fact a constant impedance, the vectorial error Ie of the diagram would be the composite error, but in practice the magnetizing impedance Ze is not constant with the result that the exciting current Ie contains some harmonics of the fundamental frequency which increases its rms value and therefore increases the composite error. This effect is most noticeable in the region approaching saturation of the core when the waveforms of the primary, secondary and exciting currents would be as shown.

Ratio Error (Current Error)

The ratio error is defined as the error in the secondary current due to the incorrect ratio and is expressed as a percentage, by

(KnIs – Ip)/Ip] × 100%

Where:
Kn = the nominal ratio (rated primary current/rated secondary current)
Is = is the actual secondary current
Ip = is the actual primary current

The ratio is considered positive when the actual secondary current of the transformer is larger than the rated current

Phase Angle Error

The phase angle error is the angle by which the secondary current vector, when reversed, differs in phase from the primary current. This angle is considered as positive if the reversed secondary current vector leads the primary current.

On very low burden power factors the phase angle error may be negative. Only on rare occasions is it necessary to determine the phase error of a CT used for relaying. These occasions occur when very low circuit settings, 1% to 5% of rated current, are used in relays which are directionalized by voltage transformer inputs. For example, sensitive reverse power relays may need phase error to be taken into account to ensure correct directional operation where very low power factor primary currents are involved. For example 1% to 3% power when certain types of prime movers are being motored such as steam turbines and hydro sets.

4.1.4 Current Transformer Ratings

Current Transformer Burden: All CT accuracy considerations require knowledge of the CT burden, which is the load applied to the secondary of the CT and should preferably be expressed in terms of the impedance of the load and its resistance and reactance components. In practice it is usual to quote the relay burdens, in the first place, in terms of V.A. (volt-amperes) and power factor. A burden of 12.5 VA at 5 A would have an ohmic value of $12.5/5^2$ = 0.5 ohm. CT burdens are usually given in preferred values, such as, 2.5, 5, 7.5, 10, 15, 30 VA.

Continuous Rated Current: This is the maximum current the current transformer can carry continuously. It is usually the rated primary current.

Short Time Rated Current: This is the amount of current which can flow for a given time period without any harmful effects. This is usually specified for 0.5, 1, 2 or 3 seconds and with the secondary short circuited.

Rated Secondary Current: This is the maximum continuous current the secondary is rated to carry. It is usually 1 or 5 A.

Accuracy Limit Factor (ALF): A current transformer is designed to maintain its ratio within specified limits up to a certain value of primary current, expressed as a multiple of its rated primary current. This multiple is termed its rated accuracy limit factor. In determining the accuracy limit factor it is necessary to consider the maximum value of primary current up to which the current transformer is required to maintain its ratio.

CT primary rating is usually chosen to be equal to or greater than the normal full load current of the protected circuit. The total secondary burden of a current transformer includes the internal impedance of the secondary winding, the impedance of the instruments and relays which are connected to it, and the resistance of the secondary leads.

4.2 Types of Protection Current Transformers

Generally, there are three different types of CTs:

- High remanence CTs

  The high remanence type has no given limit for the remanent flux. The CT has a magnetic core without any air gaps and the remanent flux might remain for almost infinite time. The remanent flux can be up to 70-80% of the saturation flux. Typical examples of high remanent type CTs are class P, PX, TPS, TPX according to IEC 60044 and non-gapped class C according to ANSI/IEEE.

- Low remanence CTs

  The low remanence type has a specified limit for the remanent flux. The magnetic core is provided with small air gaps to reduce the remanent flux to a level that does not exceed 10% of the saturation flux. Examples are class TPY according to IEC 60044-6 and class PR according to IEC 60044-1.

- Non remanence CTs

  The non remanence type CT has practically negligible level of remanent flux. The magnetic core has relatively large air gaps to reduce the secondary time constant of the CT (to lower the needed transient factor) which also reduces the remanent flux to practically zero level. An example is class TPZ according to IEC 60044-6.

4.3 Current Transformers Standards

4.3.1 IEC 60044-1

Class P: Usually specified in terms of:

- Rated Burden
- Class (5P or 10P)
- Accuracy Limit Factor

Consider the following example:

15 VA 10P20

With an external secondary burden of 15 VA the composite error will be 10% or less for primary currents up to 20 times rated current. To convert from VA and accuracy limit factor (ALF) into volts, we can use the expression:

$$V_K = \frac{VA}{I_N} \cdot ALF$$

or when the internal voltage drop in the ct needs to be taken into account

$$V_K = (ALF)\left(I_N R_{CT} + \frac{V_A}{I_N}\right)$$

Class P current transformers are typically used for general applications.

Class PR: A current transformer with less than 10% remanent flux due to small air gaps for which, in some cases, a value of the secondary loop time constant and/or a limiting value of the winding resistance may also be specified.

Class PX: The performance of Class X current transformers of the low (secondary) reactance type shall be specified in terms of each of the following characteristics:

- Rated primary current
- Turns ratio. (The error in turns ratio shall not exceed ± 0.25%)
- Knee-point voltage
- Exciting current at the knee-point voltage or at a stated percentage of the knee-point voltage.
- Resistance of secondary winding
- Class PX type CTs are used for high impedance circulating current protection and are also suitable for most protection schemes.

4.3.2 IEC 60044-6

This standard specifies the performance of inductive CTs for currents containing exponentially decaying DC components of defined time constant.

Class TPS: Protection current transformers specified in terms of complying with class TPS are generally applied to unit systems where balancing of outputs from each end of the protected plant is vital. This balance, or stability during through fault conditions, is essentially of a transient nature so the extent of the unsaturated (or linear) zones is of paramount importance. It is normal to derive, from heavy current test results, a formula stating the lowest permissible value of Vk if stable operation is to be guaranteed.

The performance of class TPS current transformers of the low (secondary) reactance type is defined by IEC 60044-6 for transient performance. They are specified in terms of each of the following characteristics:

- Rated primary current
- Turns ratio (the error in turns ratio shall not exceed ±0.25%)
- Secondary limiting voltage
- Resistance of secondary winding

Class TPS CTs are typically applied for high impedance circulating current protection.

Class TPX: The basic characteristics for class TPX current transformers are generally similar to those of class TPS current transformers except for the different error limits prescribed and possible influencing effects which may necessitate a physically larger construction. Class TPX CTs have no air gaps in the core and therefore a high remanence factor (70-80% remanent flux). The accuracy limit is defined by the peak instantaneous error during the specified transient duty cycle.

Class TPX CTs are typically used for line protection.

Class TPY: Class TPY CTs have a specified limit for the remanent flux. The magnetic core is provided with small air gaps to reduce the remanent flux to a level that does not exceed 10% of the saturation flux. They have a higher error in current measurement than TPX during unsaturated operation and the accuracy limit is defined by peak instantaneous error during the specified transient duty cycle.

Class TPY CTs are typically used for line protection with auto-reclose.

Class TPZ: For class TPZ CTs the remanent flux is practically negligible due to large air gaps in the core. These air gaps also minimize the influence of the DC component from the primary fault current, but reduce the measuring accuracy in the unsaturated (linear) region of operation. The accuracy limit is defined by peak instantaneous alternating current component error during single energization with maximum DC offset at specified secondary loop time constant.

Class TPZ CTs are typically used for special applications such as differential protection of large generators.

4.3.3 IEEE C57.13-1978

ANSI classifications define minimum steady-state performance of current transformers at high fault current levels. Performance is described by using a two-term identification system that consists of a letter and a number selected from: (C, T) (10, 20, 50, 100, 200, 400, 800), for example, C800.

The letter describes performance in terms of current transformer construction. C current transformers include bushing, window, or bar-type CTs with uniformly distributed windings. C current transformers do not have a primary winding. The primary conductor passes once through the center of a toroidal core. Since a single primary turn is used and the secondary winding is uniformly distributed, the flux that links the links the primary conductor also links the secondary winding. This type of CT has negligible leakage flux, therefore the leakage reactance is also negligible. As a result, excitation characteristic can be used directly to determine performance. The ratio correction at any current can be calculated adequately if the burden, secondary winding resistance, and the excitation characteristics are known.

Class T current transformers include wound-type CTs. These are usually constructed with more than one primary turn and undistributed windings. As a result of the physical space required for insulation and bracing of the primary winding and fringing effects of non-uniformly distributed windings, flux which does not link both primary and secondary windings results. The presence of the leakage flux has a significant effect on current transformer performance. When this flux is appreciable, it is not possible to calculate ratio correction knowing the burden and the excitation characteristic. Hence, ratio correction is determined by test.

The number is the secondary terminal voltage rating. It specifies the secondary voltage that can be delivered by the full winding at 20 times rated secondary current without exceeding 10 percent ratio correction.

As an example, an 800 V rating means that the ratio correction will not exceed 10 percent at any current from 1 to 20 times rated current with a standard 8.0Ω burden. (8.0Ω times 5 A times 20 times rated secondary current equals 800 V.) The ANSI voltage rating applies to the full secondary winding only. If other than the full winding is used, the voltage rating is reduced in proportion to turns used.

4.4 Differential Function

For accuracy, class X or class 5P Current Transformers (CTs) are strongly recommended.

The current transformer knee-point voltage requirements are based on these settings for transformer differential protection:

Is1 = 0.2 pu,
K1 = 30%,
Is2 = 1 pu,
K2 = 80%,
Is-HS1 = 10 pu,
Is-HS2 = 32 pu,
Ih(2)%> = 20%,
Cross blocking = enabled,
5th harm blocked = enabled,
Ih(5)%>=35%,
CTSat and NoGap = enabled or disabled.
The matching factors are 1.0 and the zero sequence filters are enabled.

To achieve through fault stability, the K dimensioning factor must comply with the following expressions:

System conditions	K (CT dimensioning factor)	Knee point voltage
$I_n < I_F \leq 40I_n$ $5 \leq X/R \leq 20$	K = 20	$V_K \geq 20 \times I_n \times (R_{CT} + 2R_L + R_r)$(1) $V_K \geq 20 \times I_n \times (R_{CT} + R_L + R_r)$(2)
$40I_n < I_F \leq 64I_n$ $5 \leq X/R \leq 20$	K = 30	$V_K \geq 30 \times I_n \times (R_{CT} + 2R_L + R_r)$(1) $V_K \geq 30 \times I_n \times (R_{CT} + R_L + R_r)$(2)
$I_n < I_F \leq 40I_n$ $20 < X/R \leq 120$	K = 30	$V_K \geq 30 \times I_n \times (R_{CT} + 2R_L + R_r)$(1) $V_K \geq 30 \times I_n \times (R_{CT} + R_L + R_r)$(2)
$40I_n < I_F \leq 64I_n$ $20 < X/R \leq 120$	K = 40	$V_K \geq 40 \times I_n \times (R_{CT} + 2R_L + R_r)$(1) $V_K \geq 40 \times I_n \times (R_{CT} + R_L + R_r)$(2)

Where:

K = CT dimensioning factor

I_F = maximum external fault current

X/R = primary system X/R ratio

I_n = Relay rated current

R_r = resistance of any other protective relays sharing the current transformer (Ω)

(1) = single phase fault or phase-phase-ground fault

(2) = three phase fault or phase-phase fault

To ensure that through fault stability is achieved the following ratios:

$V_{k\text{-}HV} / R_{tot\text{-}HV} : V_{k\text{-}LV} / R_{tot\text{-}LV}$

$V_{k\text{-}HV} / R_{tot\text{-}HV} : V_{k\text{-}TV} / R_{tot\text{-}TV}$

$V_{k\text{-}LV} / R_{tot\text{-}LV} : V_{k\text{-}TV} / R_{tot\text{-}TV}$

should not exceed a maximum disparity of 4:1. This ensures that during a through fault condition the flux density in the current transformers is not greatly different.

Where:

$V_{k\text{-}HV}$ = Knee point voltage of CT at HV side

$R_{tot\text{-}HV}$ = Total burden connected to CT at HV side
= $(R_{CT} + 2R_l + R_r)$ or $(R_{CT} + R_l + R_r)$

$V_{k\text{-}LV}$ = Knee point voltage of CT at LV side

$R_{tot\text{-}LV}$ = Total burden connected to CT at LV side
= $(R_{CT} + 2R_l + R_r)$ or $(R_{CT} + R_l + R_r)$

$V_{k\text{-}TV}$ = Knee point voltage of CT at TV side

$R_{tot\text{-}TV}$ = Total burden connected to CT at TV side
= $(R_{CT} + 2R_l + R_r)$ or $(R_{CT} + R_l + R_r)$

4.4.1 Differential Function - CT Requirements Calculation Example

All the possible system operating conditions must be analyzed to determine the appropriate CT requirements. The operating conditions of the power system are determined by the Utility practices. For example, the power system may operate under maximum or minimum generation; both conditions must be studied and the condition resulting in the highest knee point voltage must be considered. The highest knee point voltage is the minimum voltage required to maintain stability during through fault conditions. Consider the system shown in Figure 92. The equivalent sources 1 and 2 represent the system under maximum generation. Through faults 1 and 2 are considered to determine the highest knee point voltage. In this example, only three phase and single phase faults have been considered. In real applications, all fault types should be studied to determine the minimum knee point voltage required to maintain stability during through fault conditions.

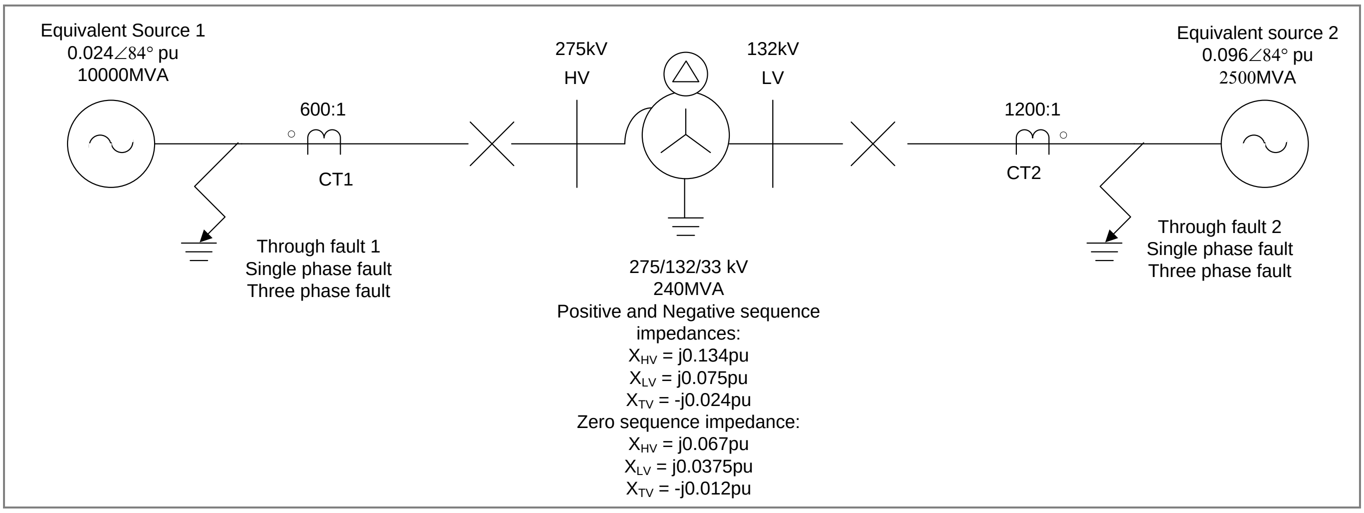

Equivalent Source 1
0.024∠84° pu
10000MVA
600:1
CT1
Through fault 1
Single phase fault
Three phase fault
275kV
HV
132kV
LV
275/132/33 kV
240MVA
Positive and Negative sequence impedances:
X_HV = j0.134pu
X_LV = j0.075pu
X_TV = -j0.024pu
Zero sequence impedance:
X_HV = j0.067pu
X_LV = j0.0375pu
X_TV = -j0.012pu
1200:1
CT2
Equivalent source 2
0.096∠84° pu
2500MVA
Through fault 2
Single phase fault
Three phase fault

Figure 92 - CT requirements calculation

Through Fault 1 – Single Phase Fault:

Through Fault 1 is an A phase to ground fault. The sequence network is shown in Figure 93. For a detailed calculation of the currents refer to Section 2.2. The current flowing through CT1 and CT2 has been calculated as well as X/R considering source 2 and the transformer impedance.

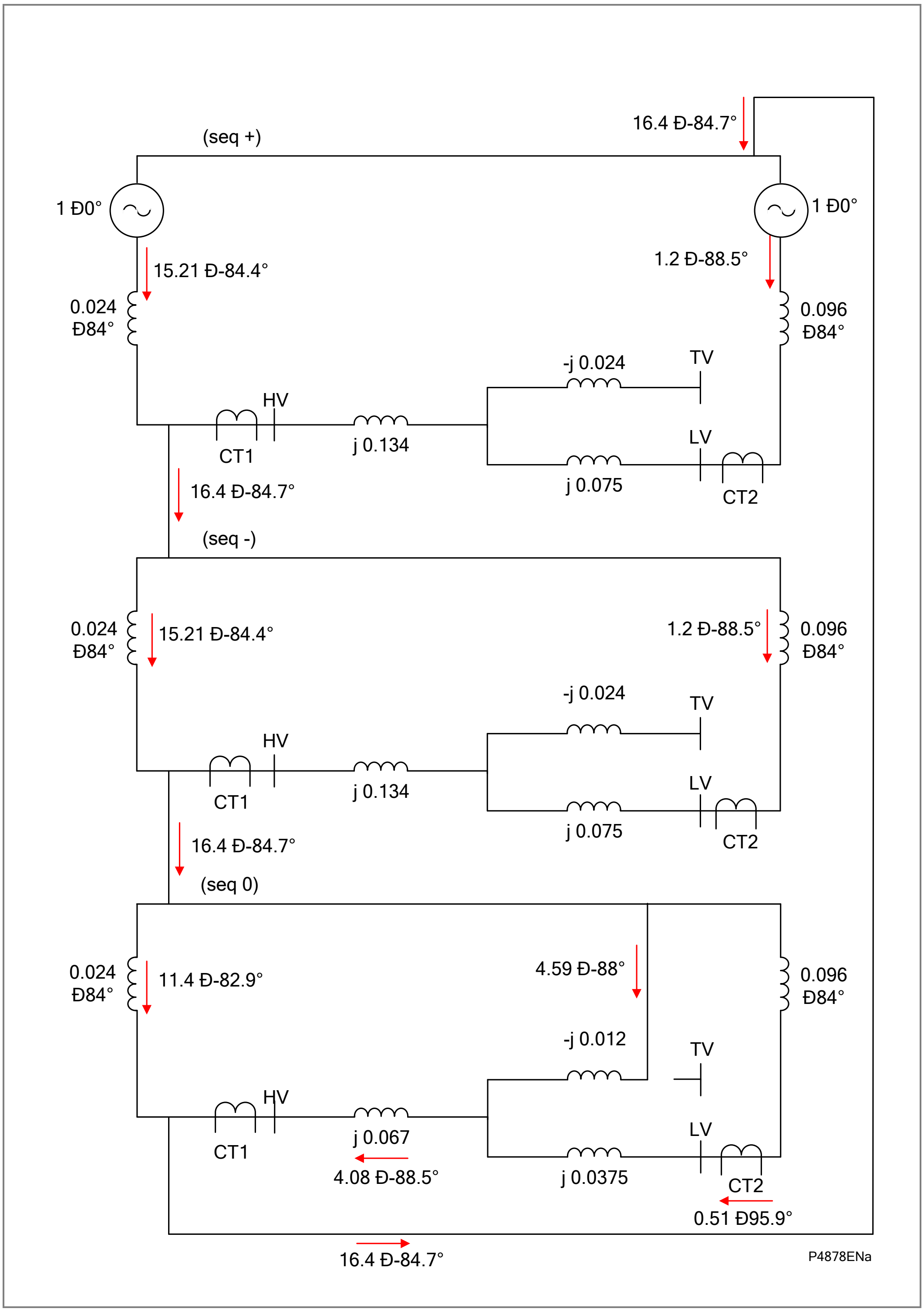

16.4 Ð-84.7°
(seq +)
1 Ð0°
1 Ð0°
15.21 Ð-84.4°
1.2 Ð-88.5°
0.024
Ð84°
0.096
Ð84°
-j 0.024
TV
HV
CT1
j 0.134
LV
j 0.075
CT2
16.4 Ð-84.7°
(seq -)
0.024
Ð84°
15.21 Ð-84.4°
1.2 Ð-88.5°
0.096
Ð84°
-j 0.024
TV
HV
CT1
j 0.134
LV
j 0.075
CT2
16.4 Ð-84.7°
(seq 0)
0.024
Ð84°
11.4 Ð-82.9°
4.59 Ð-88°
0.096
Ð84°
-j 0.012
TV
HV
CT1
j 0.067
4.08 Ð-88.5°
LV
j 0.0375
CT2
0.51 Ð95.9°
16.4 Ð-84.7°
P4878ENa

Figure 93 - Sequence network – single phase - through fault 1

The currents flowing through CT1 and CT2 are calculated as follows:

$$\begin{bmatrix} Ia \\ Ib \\ Ic \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \times \begin{bmatrix} I_0 \\ I_1 \\ I_2 \end{bmatrix}$$

Current flowing through CT1:

$$Ia = I_0 + I_1 + I_2 = 5.1\angle -88.8^\circ + 1.2\angle -88.5^\circ + 1.2\angle -88.5^\circ = 7.5\angle -88.7^\circ \text{pu}$$

$$\Rightarrow 7.5 \times \frac{240 \times 10^6}{\sqrt{3} \times 275 \times 10^3} = 3779 \text{Aprim}$$

$$\Rightarrow \frac{3779}{600} = 6.3 \text{A sec}$$

$$Ib = I_0 + a^2 \times I_1 + a \times I_2$$

$$Ib = 5.1\angle -88.8^\circ + 1\angle 240^\circ \times 1.2\angle -88.5^\circ + 1\angle 120^\circ \times 1.2\angle -88.5^\circ = 3.9\angle -88.9^\circ \text{pu}$$

$$Ic = I_0 + a \times I_1 + a^2 \times I_2$$

$$Ib = 5.1\angle -88.8^\circ + 1\angle 120^\circ \times 1.2\angle -88.5^\circ + 1\angle 240^\circ \times 1.2\angle -88.5^\circ = 3.9\angle -88.9^\circ \text{pu}$$

Current flowing through CT2:

$$Ia = I_0 + I_1 + I_2 = 0.51\angle 95.9^\circ + 1.2\angle -88.5^\circ + 1.2\angle -88.5^\circ = 1.89\angle -89.7^\circ \text{pu}$$

$$\Rightarrow 1.89 \times \frac{240 \times 10^6}{\sqrt{3} \times 132 \times 10^3} = 1984 \text{Aprim}$$

$$\Rightarrow \frac{1984}{1200} = 1.65 \text{A sec}$$

$$Ib = I_0 + a^2 \times I_1 + a \times I_2$$

$$Ib = 0.51\angle 95.9^\circ + 1\angle 240^\circ \times 1.2\angle -88.5^\circ + 1\angle 120^\circ \times 1.2\angle -88.5^\circ = 1.71\angle 92.8^\circ \text{pu}$$

$$Ic = I_0 + a \times I_1 + a^2 \times I_2$$

$$Ib = 0.51\angle 95.9^\circ + 1\angle 120^\circ \times 1.2\angle -88.5^\circ + 1\angle 240^\circ \times 1.2\angle -88.5^\circ = 1.71\angle 92.8^\circ \text{pu}$$

Equivalent X/R:

Figure 94 is the equivalent sequence network of Figure 93. The equivalent system responsible for the current flowing through CT1 and CT2 consists of source 2 and the autotransformer impedance. The equivalent system X/R is determined as follows:

$$V_A = V_0 + V_1 + V_2 = 1\angle 0^\circ \text{pu}$$

$$I_A = I_0 + I_1 + I_2 = 5.1\angle -88.8^\circ + 1.2\angle -88.5^\circ + 1.2\angle -88.5^\circ = 7.5\angle 88.7^\circ$$

$$Z = \frac{V_A}{I_A} = \frac{1\angle 0^\circ}{7.5\angle -88.7^\circ} = 0.133\angle 88.7^\circ \Rightarrow \frac{X}{R} = \tan(88.7) = 44$$

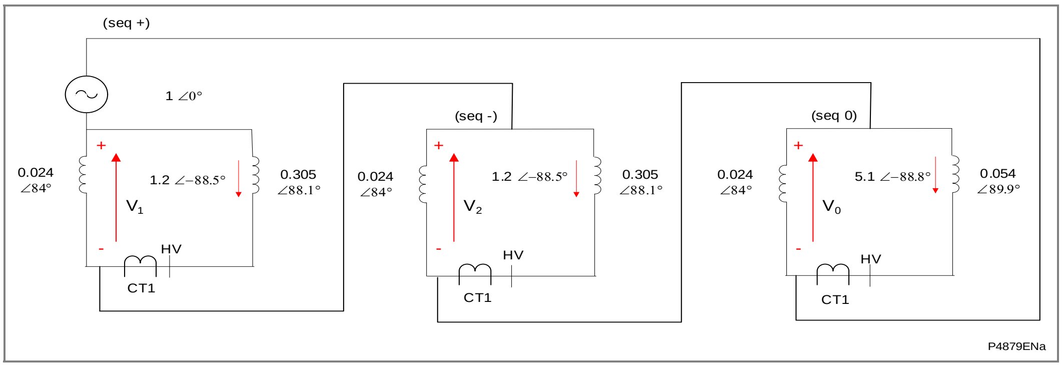

(seq +)
1 ∠0°
0.024 ∠84°
+
1.2 ∠−88.5°
V1
0.305 ∠88.1°
-
HV
CT1
(seq -)
0.024 ∠84°
+
1.2 ∠−88.5°
V2
0.305 ∠88.1°
-
HV
CT1
(seq 0)
0.024 ∠84°
+
5.1 ∠−88.8°
V0
0.054 ∠89.9°
-
HV
CT1
P4879ENa

Figure 94 - Sequence network – single phase - through fault 1

Through Fault 2 – Single Phase Fault:

Through Fault 2 sequence network is shown in Figure 95. The current flowing through CT1 and CT2 is calculated as well as X/R considering source 1 and the transformer impedance.

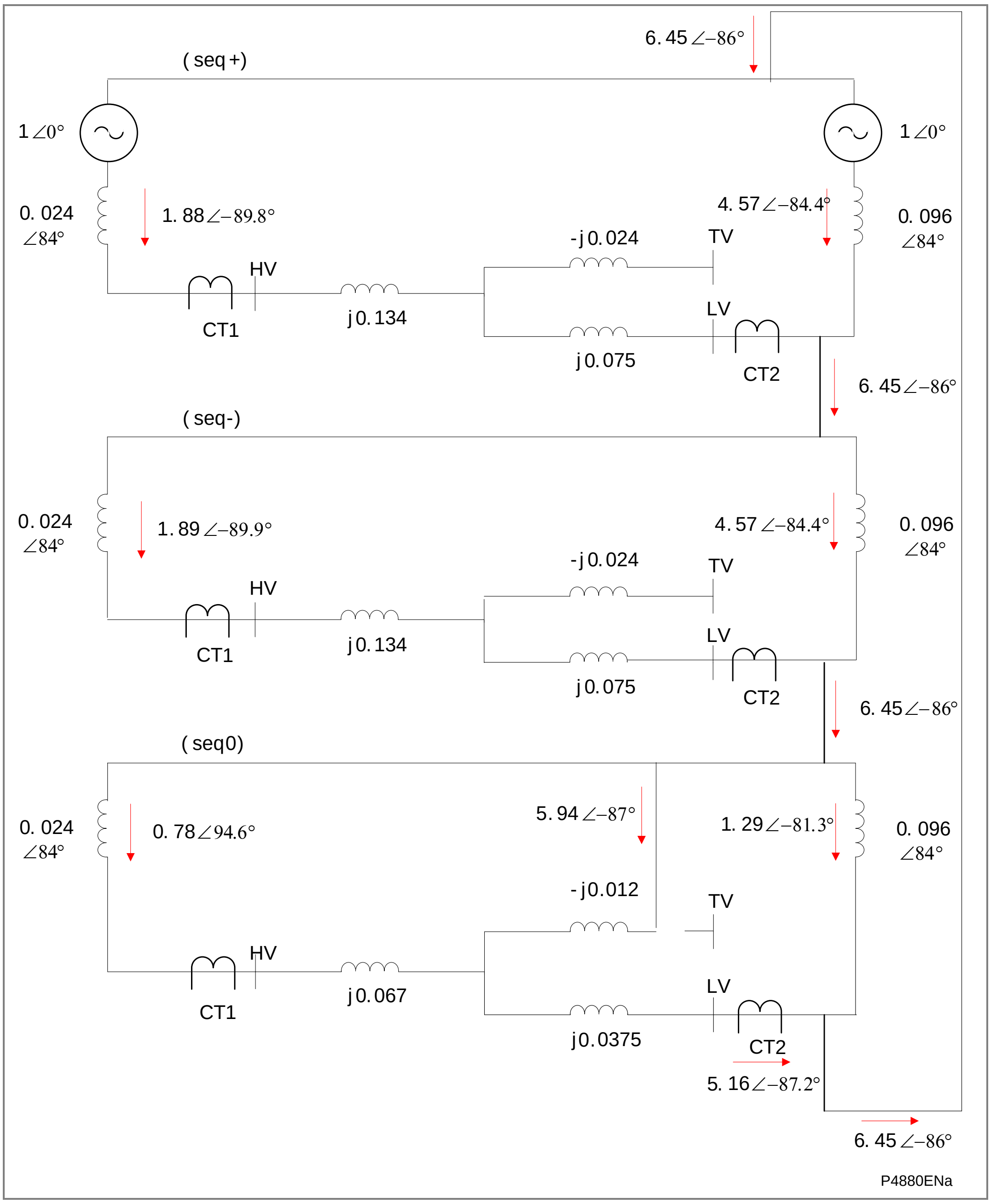

6. 45∠−86°
(seq +)
1∠0°
1∠0°
0. 024
∠84°
1. 88∠−89.8°
4. 57∠−84.4°
0. 096
∠84°
-j 0. 024
TV
HV
CT1
j 0. 134
LV
j 0. 075
CT2
6. 45∠−86°
(seq-)
0. 024
∠84°
1. 89∠−89.9°
4. 57∠−84.4°
0. 096
∠84°
-j 0. 024
TV
HV
CT1
j 0. 134
LV
j 0. 075
CT2
6. 45∠−86°
(seq0)
0. 024
∠84°
0. 78∠94.6°
5. 94∠−87°
1. 29∠−81.3°
0. 096
∠84°
- j0. 012
TV
HV
CT1
j 0. 067
LV
j0. 0375
CT2
5. 16∠−87.2°
6. 45∠−86°
P4880ENa

Figure 95 - Sequence network – single phase - through fault 2

The currents flowing through CT1 and CT2 are calculated as follows:

$$\begin{bmatrix} Ia \\ Ib \\ Ic \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & a^2 & a \\ 1 & a & a^2 \end{bmatrix} \times \begin{bmatrix} I_0 \\ I_1 \\ I_2 \end{bmatrix}$$

Current flowing through CT1:

$$Ia = I_0 + I_1 + I_2 = 0.78\angle 94.6^\circ + 1.88\angle -89.9^\circ + 1.88\angle -89.9^\circ = 2.98\angle -91^\circ \text{pu}$$

$$\Rightarrow 2.98 \times \frac{240 \times 10^6}{\sqrt{3} \times 275 \times 10^3} = 1502 \text{Aprim}$$

$$\Rightarrow \frac{1502}{600} = 2.5 \text{A sec}$$

$$Ib = I_0 + a^2 \times I_1 + a \times I_2$$

$$Ib = 0.78\angle 94.6^\circ + 1\angle 240^\circ \times 1.88\angle -89.9^\circ + 1\angle 120^\circ \times 1.88\angle -89.9^\circ = 2.66\angle 91.4^\circ \text{pu}$$

$$Ic = I_0 + a \times I_1 + a^2 \times I_2$$

$$Ib = 0.78\angle 94.6^\circ + 1\angle 120^\circ \times 1.88\angle -89.9^\circ + 1\angle 240^\circ \times 1.88\angle -89.9^\circ = 2.66\angle 91.4^\circ \text{pu}$$

Current flowing through CT2:

$$Ia = I_0 + I_1 + I_2 = 5.16\angle -87.2^\circ + 1.88\angle -89.9^\circ + 1.88\angle -89.9^\circ = 8.9\angle -88.3^\circ \text{pu}$$

$$\Rightarrow 8.9 \times \frac{240 \times 10^6}{\sqrt{3} \times 132 \times 10^3} = 9343 \text{Aprim}$$

$$\Rightarrow \frac{9343}{1200} = 7.8 \text{A sec}$$

$$Ib = I_0 + a^2 \times I_1 + a \times I_2$$

$$Ib = 5.16\angle -87.2^\circ + 1\angle 240^\circ \times 1.88\angle -89.9^\circ + 1\angle 120^\circ \times 1.88\angle -89.9^\circ = 3.28\angle -85.7^\circ \text{pu}$$

$$Ic = I_0 + a \times I_1 + a^2 \times I_2$$

$$Ib = 5.16\angle -87.2^\circ + 1\angle 120^\circ \times 1.88\angle -89.9^\circ + 1\angle 240^\circ \times 1.88\angle -89.9^\circ = 3.28\angle 85.7^\circ \text{pu}$$

Equivalent X/R:

Figure 96 is the equivalent sequence network of Figure 95. The equivalent system responsible for the current flowing through CT1 and CT2 consists of source 1 and the autotransformer impedance. The equivalent system X/R can be determined as follows:

$$V_A = V_0 + V_1 + V_2 = 1\angle 0^\circ \text{pu}$$

$$I_A = I_0 + I_1 + I_2 = 1.88\angle -89.9^\circ + 1.88\angle -89.9^\circ + 5.16\angle -87.2^\circ = 8.92\angle -88.3^\circ$$

$$Z = \frac{V_A}{I_A} = \frac{1\angle 0^\circ}{8.92\angle -88.3^\circ} = 0.112\angle 88.3^\circ \Rightarrow \frac{X}{R} = \tan(88.3) = 34$$

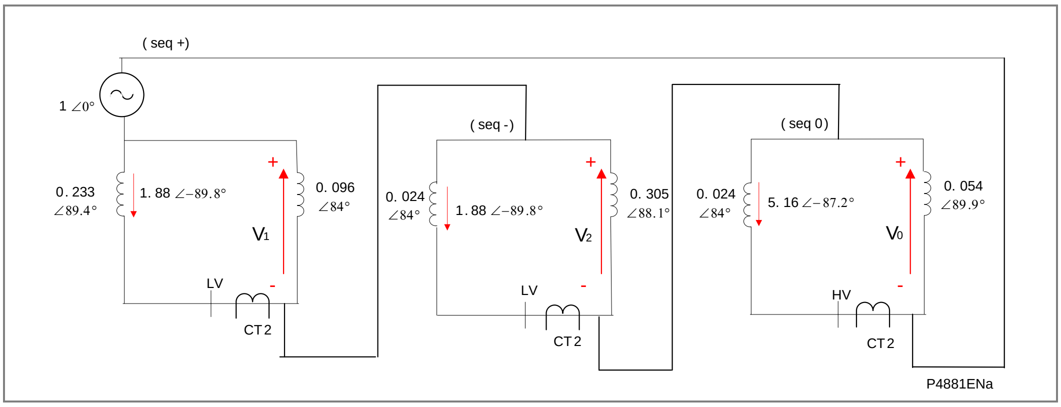


Figure 96 - Sequence network – single phase - through fault 2

Through Fault 1 – Three Phase Fault:

The three-phase through fault 1 sequence network is shown in Figure 97. The current flowing through CT1 and CT2 is calculated as well as the X/R considering source 2 and the transformer impedance.

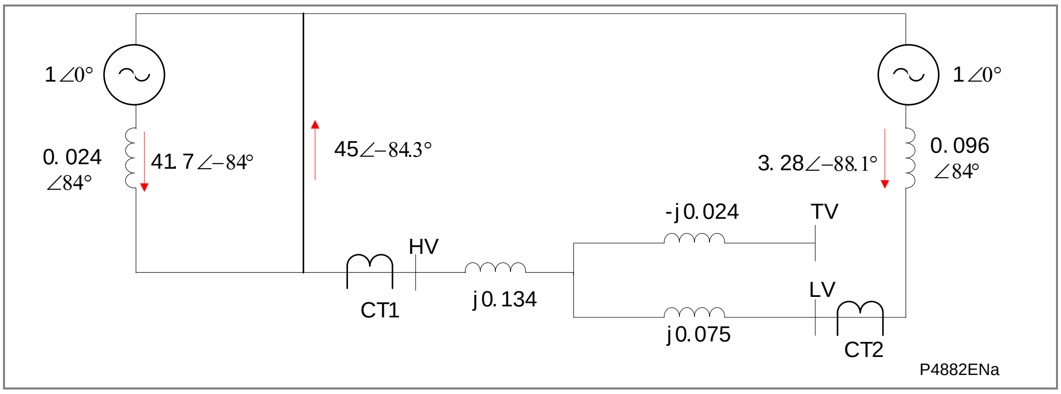


Figure 97 - Sequence network – three phase - through fault 1

Current flowing through CT1:

$$I = 3.28\angle -88.1^{\circ}\,\mathrm{pu}$$

$$\Rightarrow 3.28 \times \frac{240 \times 10^{6}}{\sqrt{3} \times 275 \times 10^{3}} = 1653\,\mathrm{A\,prim}$$

$$\Rightarrow \frac{1653}{600} = 2.75\,\mathrm{A\,sec}$$

Current flowing through CT2:

$$I = 3.28\angle -88.1^{\circ}\,\mathrm{pu}$$

$$\Rightarrow 3.28 \times \frac{240 \times 10^{6}}{\sqrt{3} \times 132 \times 10^{3}} = 3443\,\mathrm{A\,prim}$$

$$\Rightarrow \frac{3443}{1200} = 2.9\,\mathrm{A\,sec}$$

Equivalent X/R:

The system equivalent X/R is determined as follows:

$$V = 1\angle 0^{\circ}\,\mathrm{pu}$$

$$I = 3.28\angle -88.1^{\circ}$$

$$Z = \frac{V}{I} = \frac{1\angle 0^{\circ}}{3.28\angle -88.1^{\circ}} = 0.30\angle 88.1^{\circ} \Rightarrow \frac{X}{R} = \tan(88.1) = 30$$

Through Fault 2 – Three Phase Fault:

The three-phase through fault 2 sequence network is shown in Figure 98. The current flowing through CT1 and CT2 must be calculated as well as the X/R considering source 1 and the transformer impedance.

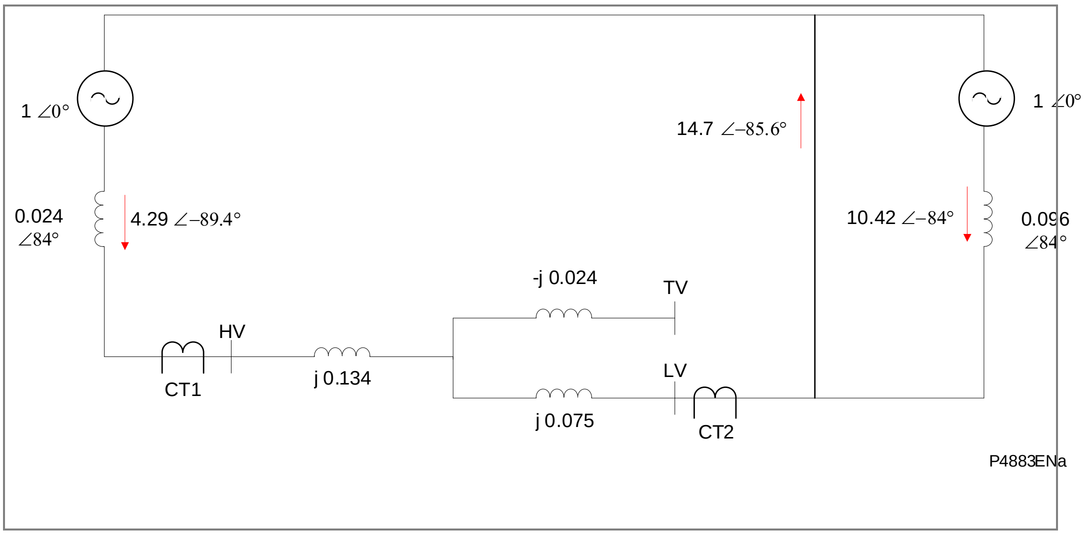


Figure 98 - Sequence network – three phase - through fault 2

Current flowing through CT1:

$$I = 4.29\angle -89.4^\circ \text{pu}$$

$$\Rightarrow 4.29 \times \frac{240 \times 10^6}{\sqrt{3} \times 275 \times 10^3} = 2162 \text{Aprim}$$

$$\Rightarrow \frac{2162}{600} = 3.6 \text{A sec}$$

Current flowing through CT2:

$$I = 4.29\angle -89.4^\circ \text{pu}$$

$$\Rightarrow 4.29 \times \frac{240 \times 10^6}{\sqrt{3} \times 132 \times 10^3} = 4503 \text{Aprim}$$

$$\Rightarrow \frac{4503}{1200} = 3.75 \text{A sec}$$

Equivalent X/R:

The equivalent system X/R can be determined as follows:

$$V = 1\angle 0^\circ \text{pu}$$

$$I = 4.29\angle -89.4^\circ$$

$$Z = \frac{V}{I} = \frac{1\angle 0^\circ}{4.29\angle -89.4^\circ} = 0.23\angle 89.4^\circ \Rightarrow \frac{X}{R} = \tan(89.4) = 95$$

The results have been summarized as follows:

	Through Fault 1 Single Phase	Through Fault 2 Single Phase	Through Fault 1 Three Phase	Through Fault 2 Three Phase
X/R	44	34	30	95
CT1	6.3 A sec	2.5 A sec	2.75 A sec	3.6 A sec
CT2	1.65 A sec	7.8 A sec	2.9 A sec	3.75 A sec

Table 19 - Through fault single and three-phase results summary

According to two situations the CT dimension factor K required is 55/25 and the CT knee point voltage must comply with

1. The operating time for internal faults ≤35ms (100%) and relay keeps stable for through faults. CT dimension factor K = 55.

   V_K ・ $= 55 \times I_n \times (R_{CT} + 2R_L + R_r)$ for single phase fault

   V_K ・ $= 55 \times I_n \times (R_{CT} + R_L + R_r)$ for three phase faults

2. The operating time for internal faults ≤ 35ms (85%) and 75ms (100%), and relay keeps stable for through fault. CT dimension factor K = 25.

   V_K ・ $= 25 \times I_n \times (R_{CT} + 2R_L + R_r)$ for single phase fault

   V_K ・ $= 25 \times I_n \times (R_{CT} + R_L + R_r)$ for three phase faults

Consider that $R_L = 2\ \Omega$ and $R_{CT1} = 0.4\ \Omega$ and $R_{CT2} = 0.8\ \Omega$, then the knee point voltages are as follows:

		Through Fault 1 Single Phase	Through Fault 2 Single Phase	Through Fault 1 Three Phase	Through Fault 2 Three Phase
K=55	CT1	242	242	132	132
	CT2	264	264	154	154
K=25	CT1	110	110	60	60
	CT2	120	120	70	70

Table 20 - Through fault single and three-phase results summary

Therefore, CT1 requires a minimum knee point voltage of 110 V and CT2 a minimum knee point voltage of 120 V.

The maximum disparity ratio allowed is 4:1, then Vk-HV / Rtot-HV: Vk-LV / Rtot-LV should not exceed 4:1. If CT1 and CT2 have 110 V and 120 V knee point voltages respectively, then the disparity ratio is 1:1.

In this example, only one system operating condition was studied. Note that the different system operating conditions must be analysed and the highest knee point voltage must be considered.

4.5 Low Impedance REF

For accuracy, class X or class 5P Current Transformers (CTs) are strongly recommended.

The CT requirements for low impedance REF protection are generally lower than those for differential protection. As the line CTs for low impedance REF protection are the same as those used for differential protection the differential CT requirements cover both differential and low impedance REF applications.

The CT knee-point voltage requirements are based on the following settings for transformer REF protection; IS1 = 27, IS2 = 270, K1 = 0%, K2 = 150%.

A series of internal and external faults were performed to determine the CT requirements for the REF function. These tests were performed under different X/R ratios, CT burdens, fault currents, fault types and point on wave.

The K dimensioning factor for the REF function is smaller than that for the transformer differential protection. Since the highest K factor must be considered, the CT requirements for transformer differential must be considered.

4.5.1 One Breaker Application

According to the CT requirements test results, to achieve through fault stability the K dimensioning factor must comply with the following expression:

System conditions	K (CT dimensioning factor)	Knee point voltage
$2I_n < I_F \leq 64I_n$ $5 \leq X/R \leq 120$	K = 12	$VK \geq 12 \times In \times (R_{CT} + 2R_L + R_r)$
Where: V_K = Minimum current transformer knee-point voltage K = CT dimensioning factor R_{ct} = Resistance of current transformer secondary winding (Ω) R_L = Resistance of a single lead from relay to current transformer (Ω) R_r = Resistance of any other protective relays sharing the current transformer (Ω) I_n = CT secondary nominal current (either 1A or 5) I_F = maximum external single phase fault		

Table 21 - CT dimensioning factor

To ensure that the quoted operating times and through fault stability limits are met the following ratios should not exceed a maximum disparity ratio of 7:1:

$V_{k\text{-}HV} / R_{tot\text{-}HV} : V_{k\text{-}TN1} / R_{tot\text{-}TN1}$

$V_{k\text{-}LV} / R_{tot\text{-}LV} : V_{k\text{-}TN2} / R_{tot\text{-}TN2}$

$V_{k\text{-}TV} / R_{tot\text{-}TV} : V_{k\text{-}TN3} / R_{tot\text{-}TN3}$

This ensures that during a through fault condition the flux density in the current transformers is not greatly different.

Where:
$V_{k\text{-}HV}$ = Knee point voltage of CT at HV side
$R_{tot\text{-}HV}$ = Total burden connected to CT at HV side = $(R_{CT} + 2R_l + R_r)$
$V_{k\text{-}LV}$ = Knee point voltage of CT at LV side
$R_{tot\text{-}LV}$ = Total burden connected to CT at LV side = $(R_{CT}+ 2R_l + R_r)$
$V_{k\text{-}TV}$ = Knee point voltage of CT at TV side
$R_{tot\text{-}TV}$ = Total burden connected to CT at TV side = $(R_{CT}+ 2R_l + R_r)$
$V_{k\text{-}TN1}$ = Knee point voltage of TN1 CT
$R_{tot\text{-}TN1}$ = Total burden connected to TN1 CT = $(R_{CT} + 2R_l + R_r)$
$V_{k\text{-}TN2}$ = Knee point voltage of TN2 CT
$R_{tot\text{-}TN2}$ = Total burden connected to TN2 CT = $(R_{CT} + 2R_l + R_r)$

$V_{k\text{-}TN3}$ = Knee point voltage of TN3 CT
$R_{tot\text{-}TN3}$ = Total burden connected to TN3 CT = $(R_{CT} + 2R_l + R_r)$

4.5.2 One and a Half Breaker Application and Autotransformer Application

According to the CT requirements test results, to achieve through fault stability the K dimensioning factor must comply with the following expression:

<table>
<tr><th>System conditions</th><th>K (CT dimensioning factor)</th><th>Knee point voltage</th></tr>
<tr><td>$2I_n < I_F \leq 64I_n$
$5 \leq X/R \leq 120$</td><td>K = 27</td><td>$VK \geq 27 \times I_n \times (R_{CT} + 2R_L + R_r)$</td></tr>
<tr><td colspan="3">Where:
V_K = Minimum CT knee-point voltage
K = CT dimensioning factor
R_{ct} = Resistance of CT secondary winding (Ω)
R_L = Resistance of a single lead from relay to CT (Ω)
R_r = Resistance of any other protective relays sharing the CT (Ω)
I_n = CT secondary nominal current (either 1A or 5)
I_F = maximum external single phase fault</td></tr>
</table>

Table 22 - CT dimensioning factor

To ensure that the quoted operating times and through fault stability limits are met the following ratios should not exceed a maximum disparity ratio of 4:1:

$V_{k\text{-}HV} / R_{tot\text{-}HV} : V_{k\text{-}TN1} / R_{tot\text{-}TN1}$

$V_{k\text{-}LV} / R_{tot\text{-}LV} : V_{k\text{-}TN2} / R_{tot\text{-}TN2}$

$V_{k\text{-}TV} / R_{tot\text{-}TV} : V_{k\text{-}TN3} / R_{tot\text{-}TN3}$

This ensures that during a through fault condition the flux density in the current transformers is not greatly different.

Where:
$V_{k\text{-}HV}$ = Knee point voltage of CT at HV side
$R_{tot\text{-}HV}$ = Total burden connected to CT at HV side = $(R_{CT} + 2R_l + R_r)$
$V_{k\text{-}LV}$ = Knee point voltage of CT at LV side
$R_{tot\text{-}LV}$ = Total burden connected to CT at LV side = $(R_{CT}+ 2R_l + R_r)$
$V_{k\text{-}TV}$ = Knee point voltage of CT at TV side
$R_{tot\text{-}TV}$ = Total burden connected to CT at TV side = $(R_{CT}+ 2R_l + R_r)$
$V_{k\text{-}TN1}$ = Knee point voltage of TN1 CT
$R_{tot\text{-}TN1}$ = Total burden connected to TN1 CT = $(R_{CT} + 2R_l + R_r)$
$V_{k\text{-}TN2}$ = Knee point voltage of TN2 CT
$R_{tot\text{-}TN2}$ = Total burden connected to TN2 CT = $(R_{CT} + 2R_l + R_r)$
$V_{k\text{-}TN3}$ = Knee point voltage of TN3 CT
$R_{tot\text{-}TN3}$ = Total burden connected to TN3 CT = $(R_{CT} + 2R_l + R_r)$

4.6 High Impedance REF

In a high impedance REF scheme, the general stability voltage requirement is described by $V_S \geq K \times I_F(2R_L + R_{CT})$. The required stability voltage setting (V_S) is expressed in terms of an external fault (I_F), burden ($2R_L + R_{CT}$) and a stability factor (K).

The assumption that one CT is completely saturated for an external fault does not describe what actually happens when asymmetric CT saturation occurs. The CT that saturates will only saturate during parts of each current waveform cycle. This means that the spill current waveform seen by the differential element will be highly non-sinusoidal. The sensitivity of the relay element to non-sinusoidal spill waveforms for through faults will be a function of the REF frequency response, the REF operating time, the REF current setting and the wave shapes.

The frequency response and the operating speed are factors that are inherent to the relay design. Spill current wave shapes will be related to the ratio of the CT kneepoint voltage (Vk) to relay circuit impedance. The stability voltage, $V_S = I_S R_{ST}$, is determined by the current setting and the stabilizing resistor. The stability of the high impedance REF function during through faults is determined by the ratio V_K/V_S. Where V_K is the CT knee point voltage and V_S is the stability voltage.

The relationship between the V_K/V_S ratio and the required stability factor K has been found to be of a general form for various relay designs that have undergone conjunctive testing by Schneider Electric. It is the absolute values of V_K/V_S and K that vary in the relationship for different relay designs.

Once stability has been considered, the next performance factor to take into account is the operating time for internal faults. The CT kneepoint voltage as a multiple of the protection stability voltage setting (V_K/V_S) will govern the operating time of a differential relay element for heavy internal faults with transiently offset fault current waveforms. With the aid of the operating time curves derived for the P64x, it is possible to identify the ratio V_K/V_S that is required to achieve a desired average operating speed for internal faults.

The approach with older electromechanical high impedance relays was to use an universally safe K factor of 1.0, but the older relays operated quickly with a lower Vk/Vs ratio (Vk/Vs = 2.0). With more modern relays it is desirable to identify the optimum K factor for stability, so that the required Vk/Vs ratio for stability and operating speed will not make CT kneepoint voltage requirements worse than traditional requirements.

The high impedance REF CT requirements are shown in Figure 99. They are valid when $5 \leq X/R \leq 120$ and $0.5I_n \leq I f \leq 40I_n$. A $V_K/V_S = 4$ is recommended as the average operating time is 38 ms and K is 1 approximately.

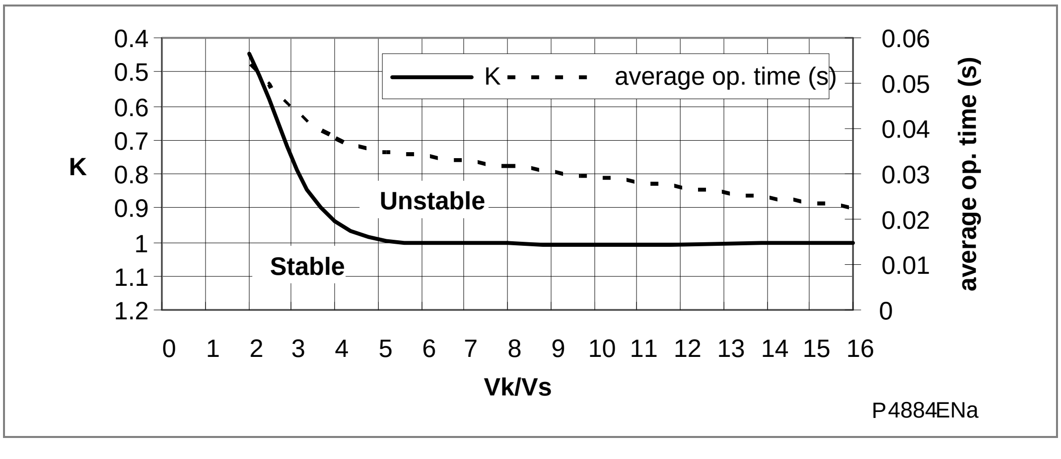


Figure 99 - High impedance REF CT requirements

4.7 Short-Interconnector Application

For accuracy, class X or class 5P current transformers (CTs) are strongly recommended.

The current transformer knee-point voltage requirements are based on the following settings for short-interconnector protection;
IS1 = 1.2 pu, IS2 = 0.4 pu, K1 = 20%, K2 = 80%,
Is-HS1 = 10 pu, HS2 Status = disabled, 2nd harm blocked = disabled,
5th harm blocked = disabled. The matching factors are 1.0 and the zero sequence filters are disabled.

A series of internal and external faults were performed to determine the CT requirements for short-interconnector protection applications. These tests were performed under different X/R ratios, CT burdens, fault currents, fault types and point on wave.

The system conditions, CT dimensioning factor and CT knee point voltage are indicated below:

System conditions	K (CT dimensioning factor)	Knee point voltage
$5I_n \leq I_F \leq 64I_n$ $5 \leq X/R < 120$	K = 28	$V_K \geq 28 \times I_n \times (R_{CT} + 2R_L + R_r)$

Where:
V_K = Minimum current transformer knee-point voltage
K = CT dimensioning factor
R_{ct} = Resistance of current transformer secondary winding (Ω)
R_L = Resistance of a single lead from relay to current transformer (Ω)
R_r = Resistance of any other protective relays sharing the current transformer (Ω)
I_n = CT secondary nominal current (either 1A or 5)
I_F = maximum external single phase fault

Table 23 - CT dimensioning factor

To ensure that the quoted operating times and through fault stability limits are met the following ratios should not exceed a maximum disparity ratio of 8:1:

$V_{k\text{-}HV} / R_{tot\text{-}HV} : V_{k\text{-}LV} / R_{tot\text{-}LV}$

$V_{k\text{-}HV} / R_{tot\text{-}HV} : V_{k\text{-}TV} / R_{tot\text{-}TV}$

$V_{k\text{-}LV} / R_{tot\text{-}LV} : V_{k\text{-}TV} / R_{tot\text{-}TV}$

This ensures that during a through fault condition the flux density in the current transformers is not greatly different.

Where:
$V_{k\text{-}HV}$ = Knee point voltage of CT at HV side
$R_{tot\text{-}HV}$ = Total burden connected to CT at HV side = $(R_{CT} + 2R_l + R_r)$
$V_{k\text{-}LV}$ = Knee point voltage of CT at LV side
$R_{tot\text{-}LV}$ = Total burden connected to CT at LV side = $(R_{CT}+ 2R_l + R_r)$
$V_{k\text{-}TV}$ = Knee point voltage of CT at TV side
$R_{tot\text{-}TV}$ = Total burden connected to CT at TV side = $(R_{CT}+ 2R_l + R_r)$

4.8 Converting IEC185 CT Standard Protection Classification to Knee-Point Voltage

The suitability of an IEC standard protection class CT can be checked against the knee-point voltage requirements specified previously.

If, for example, the available CTs have a 15 VA 5P 10 designation, then an estimated knee-point voltage can be obtained as follows:

$$V_k = \frac{\text{VA x ALF}}{\text{In}} + \text{ALF x } I_n \text{ x } R_{ct}$$

Where:

V_k = Required knee-point voltage
VA = CT rated burden (VA)
ALF = Accuracy limit factor
I_n = CT secondary rated current (A)
R_{ct} = Resistance of CT secondary winding (Ω)

If R_{ct} is not available, then the second term in the above equation can be ignored.

Example: 400/5 A, 15 VA 5P 10, R_{ct} = 0.2Ω

$$V_k = \frac{15 \text{ x } 10}{5} + 10 \text{ x } 5 \text{ x } 0.2$$

$$= 40 \text{ V}$$

4.9 Converting IEC185 CT Standard Protection Classification to ANSI/IEEE Standard Voltage

MiCOM Px40 series protection is compatible with ANSI/IEEE current transformers as specified in the IEEE C57.13 standard. The applicable class for protection is class "C", which specifies a non air-gapped core. The CT design is identical to IEC class P, or British Standard class X, but the rating is specified differently.

The ANSI/IEEE “C” Class standard voltage rating required will be lower than an IEC knee point voltage. This is because the ANSI/IEEE voltage rating is defined in terms of useful output voltage at the terminals of the CT, whereas the IEC knee point voltage includes the voltage drop across the internal resistance of the CT secondary winding added to the useful output. The IEC/BS knee point is also typically 5% higher than the ANSI/IEEE knee point.

Therefore:

Vc = [Vk - Internal voltage drop] / 1.05
= [Vk - (In . RCT . ALF)] / 1.05

Where:

Vc = “C” Class standard voltage rating
Vk = IEC Knee point voltage required
In = CT rated current = 5 A in USA
RCT = CT secondary winding resistance (for 5 A CTs, the typical resistance is 0.002 ohms/secondary turn)
ALF = The CT accuracy limit factor, the rated dynamic current output of a "C" class CT (Kssc) is always 20 x In

The IEC accuracy limit factor is identical to the 20 times secondary current ANSI/IEEE rating.

Therefore:

$$V_c = [V_k - (100 . R_{CT})] / 1.05$$

5 AUXILIARY SUPPLY FUSE RATING

In the Safety section of this manual, the maximum allowable fuse rating of 16 A is quoted. To allow time grading with fuses upstream, a lower fuselink current rating is often preferable. Use of standard ratings of between 6 A and 16 A is recommended. Low voltage fuselinks, rated at 250 V minimum and compliant with IEC60269-2 general application type gG are acceptable, with high rupturing capacity. This gives equivalent characteristics to HRC "red spot" fuses type NIT/TIA often specified historically.

Table 24 recommends advisory limits on relays connected per fused spur. This applies to MiCOM Px40 series devices with hardware suffix C and higher, as these have inrush current limitation on switch-on, to conserve the fuse-link.

Maximum number of MiCOM Px40 relays recommended per fuse				
Battery nominal voltage	6 A	10 A fuse	15 or 16 A fuse	Fuse rating > 16 A
24 to 54 V	2	4	6	Not permitted
60 to 125 V	4	8	12	Not permitted
138 to 250 V	6	10	16	Not permitted

Table 24 - Maximum number of MiCOM Px40 relays recommended per fuse

Alternatively, Miniature Circuit Breakers (MCBs) may be used to protect the auxiliary supply circuits.

PROGRAMMABLE LOGIC

CHAPTER NO 7

Date:	12/2013
Hardware Suffix:	J (P642) K (P643/P645)
Software Version:	04
Connection Diagrams:	10P642xx (xx = 1 to 10) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9)

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1 PROGRAMMABLE LOGIC

1.1 Overview

The purpose of the Programmable Scheme Logic (PSL) is to allow the relay users to configure an individual protection scheme to suit their own particular application. This is achieved through the use of programmable logic gates and delay timers.

The input to the PSL is any combination of the status of opto inputs. It is also used to assign the mapping of functions to the opto inputs and output contacts, the outputs of the protection elements, such as protection starts and trips, and the outputs of the fixed protection scheme logic. The fixed scheme logic provides the relay's standard protection schemes. The PSL consists of software logic gates and timers. The logic gates can be programmed to perform a range of different logic functions and can accept any number of inputs. The timers are used either to create a programmable delay or to condition the logic outputs, for example to create a pulse of fixed duration on the output regardless of the length of the pulse on the input. The outputs of the PSL are the LEDs on the front panel of the relay and the output contacts at the rear.

The execution of the PSL logic is event driven; the logic is processed whenever any of its inputs change, for example as a result of a change in one of the digital input signals or a trip output from a protection element. Also, only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This reduces the amount of processing time that is used by the PSL; even with large, complex PSL schemes the relay trip time will not lengthen.

This system provides flexibility for the users to create their own scheme logic design. However, it also means that the PSL can be configured into a very complex system, hence setting of the PSL is implemented through the PC support package MiCOM S1 Studio.

1.2 MiCOM S1 Studio Px40 PSL editors

To start the Px40 PSL editor, either click the icon or from the Micom S1 Studio main menu, select **Tools > PSL PSL editor (Px40)**.
The PSL editors enable you to connect to any MiCOM device front port, retrieve and edit its PSL files and send the modified file back to a MiCOM Px40 device.

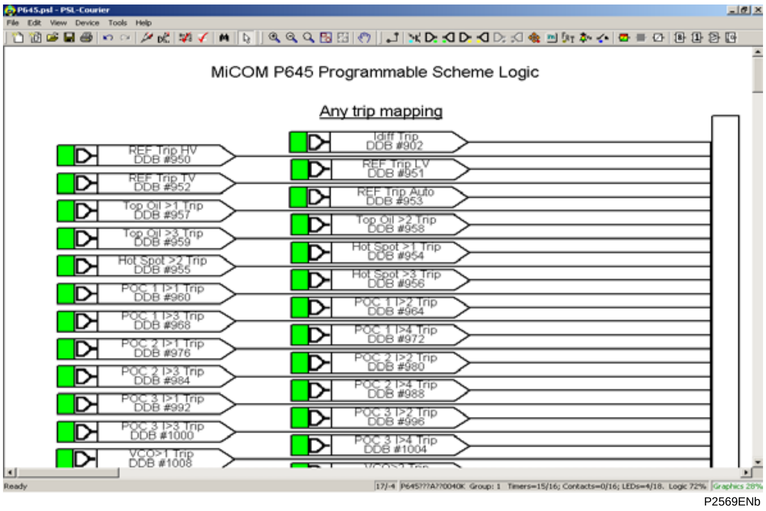

P645.psl - PSL-Courier
File Edit View Device Tools Help
MiCOM P645 Programmable Scheme Logic
Any trip mapping
Idiff Trip DDB #902
REF Trip HV DDB #950
REF Trip LV DDB #951
REF Trip TV DDB #952
REF Trip Auto DDB #953
Top Oil >1 Trip DDB #957
Top Oil >2 Trip DDB #958
Top Oil >3 Trip DDB #959
Hot Spot >1 Trip DDB #954
Hot Spot >2 Trip DDB #955
Hot Spot >3 Trip DDB #956
POC 1 I>1 Trip DDB #960
POC 1 I>2 Trip DDB #964
POC 1 I>3 Trip DDB #968
POC 1 I>4 Trip DDB #972
POC 2 I>1 Trip DDB #976
POC 2 I>2 Trip DDB #980
POC 2 I>3 Trip DDB #984
POC 2 I>4 Trip DDB #988
POC 3 I>1 Trip DDB #992
POC 3 I>2 Trip DDB #996
POC 3 I>3 Trip DDB #1000
POC 3 I>4 Trip DDB #1004
VCO>1 Trip DDB #1008
Ready
17/-4 P645???A??0040K Group: 1 Timers=15/16; Contacts=0/16; LEDs=4/18. Logic 72% Graphics 28%
P2569ENb

Figure 1 - PSL editor module

1.3 How to use MiCOM Px40 PSL editors

The MiCOM Px40 PSL editors let you:

- Start a new PSL diagram
- Extract a PSL file from a MiCOM Px40 IED
- Open a diagram from a PSL file
- Add logic components to a PSL file
- Move components in a PSL file
- Edit a link of a PSL file
- Add a link to a PSL file
- Highlight a path in a PSL file
- Use a conditioner output to control logic
- Download a PSL file to a MiCOM Px40 IED
- Print PSL files

1.4 Warnings

Checks are done before the scheme is sent to the relay. Various warning messages may be displayed as a result of these checks.

The Editor first reads in the model number of the connected relay, then compares it with the stored model number. A "wildcard" comparison is used. If a model mismatch occurs, a warning is generated before sending starts. Both the stored model number and the number read from the relay are displayed with the warning. However, the user must decide if the settings to be sent are compatible with the relay that is connected. Ignoring the warning could lead to undesired behavior of the relay.

If there are any obvious potential problems, a list is generated. The types of potential problems that the program attempts to detect are:

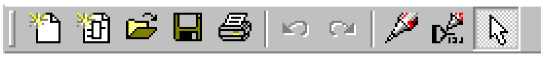
- One or more gates, LED signals, contact signals, or timers have their outputs linked directly back to their inputs. An erroneous link of this sort could lock up the relay, or cause other more subtle problems to arise.
- Inputs To Trigger (ITT) exceeds the number of inputs. If a programmable gate has its ITT value set to greater than the number of actual inputs, the gate can never activate. There is no lower ITT value check; a 0-value does not generate a warning.
- Too many gates. There is a theoretical upper limit of 256 gates in a scheme, but the practical limit is determined by the complexity of the logic. In practice the scheme would have to be very complex, and this error is unlikely to occur.
- Too many links. There is no fixed upper limit to the number of links in a scheme. However, as with the maximum number of gates, the practical limit is determined by the complexity of the logic. In practice the scheme would have to be very complex, and this error is unlikely to occur.

1.5 Toolbar and Commands

There are several toolbars available for easy navigation and editing of PSL.

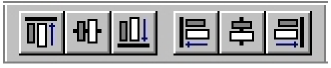
1.5.1 Standard Tools

For file management and printing.



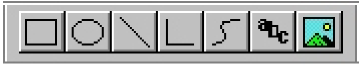
1.5.2 Alignment Tools

To align logic elements horizontally or vertically into groups.



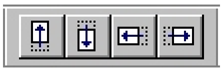
1.5.3 Drawing Tools

To add text comments and other annotations, for easier reading of PSL schemes.



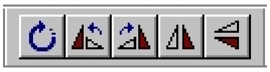
1.5.4 Nudge Tools

To move logic elements.



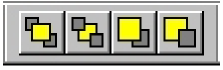
1.5.5 Rotation Tools

To spin, mirror and flip.



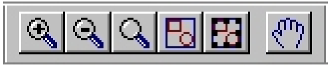
1.5.6 Structure Tools

To change the stacking order of logic components.



1.5.7 Zoom and Pan Tools

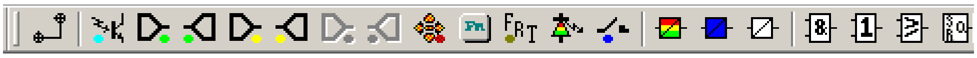
For scaling the displayed screen size, viewing the entire PSL, or zooming to a selection.



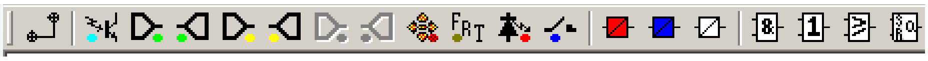
1.5.8 Logic Symbols

This toolbar provides icons to place each type of logic element into the scheme diagram. Not all elements are available in all devices. Icons are only displayed for those elements available in the selected device.

P643/P645 Logic Symbols:



P642 Logic Symbols:



Link

Create a link between two logic symbols.

Opto Signal

Create an opto signal.

Input Signal

Create an input signal.

Output Signal

Create an output signal.

GOOSE In

Create an input signal to logic to receive an IEC 61850 GOOSE message transmitted from another IED.

GOOSE Out

Create an output signal from logic to transmit an IEC 61850 GOOSE message to another IED.

Control In

Create an input signal to logic that can be operated from an external command.

Function Key

Create a function key input signal.

Trigger Signal

Create a fault record trigger.

LED Signal

P645: Create an LED input signal that repeats the status of a tri-color LED.

P642/P643/P645: Create an LED input signal that repeats the status of a red LED.

Contact Signal

Create a contact signal.

LED Conditioner

Create an LED conditioner for tri-color LED (P645)

Create an LED conditioner for red LED (P642/3/5)

Contact Conditioner

Create a contact conditioner.

Timer

Create a timer.

AND Gate

Create an AND Gate.

OR Gate

Create an OR Gate.

Programmable Gate

Create a programmable gate.

SR gate

Create an SR gate.

1.6 PSL Logic Signals Properties

The logic signal toolbar is used for the selection of logic signals.

1.6.1 Signals Properties Menu

The logic signal toolbar is used for the selection of logic signals. To use this:

Use the logic toolbar to select logic signals.
This is enabled by default but to hide or show it, select **View** > **Logic Toolbar**.

Zoom in or out of a logic diagram using the toolbar icon or select **View** > **Zoom Percent**.

Right-click any logic signal and a context-sensitive menu appears.

Certain logic elements show the **Properties…** option. Select this and a **Component Properties** window appears. The Component Properties window and the signals listed vary depending on the logic symbol selected.

The following subsections describe each of the available logic symbols.

1.6.2 Link Properties

Links form the logical link between the output of a signal, gate or condition and the input to any element.

Any link that is connected to the input of a gate can be inverted. Right-click the input and select **Properties…**. The **Link Properties** window appears.

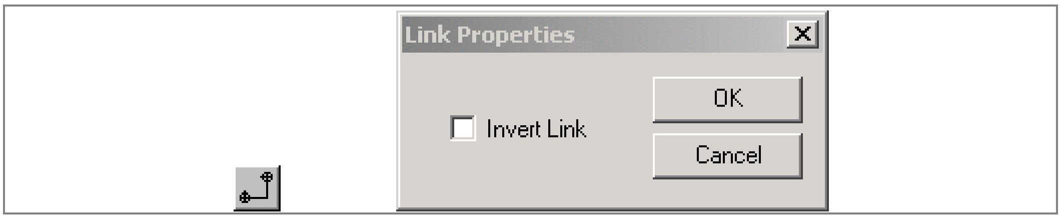


Figure 2 - Link properties

Rules for Linking Symbols

An inverted link is shown with a small circle on the input to a gate. A link must be connected to the input of a gate to be inverted.

Links can only be started from the output of a signal, gate, or conditioner, and can only be ended at an input to any element.

Signals can only be an input or an output. To follow the convention for gates and conditioners, input signals are connected from the left and output signals to the right. The Editor automatically enforces this convention.

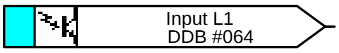
A link is refused for the following reasons:

- An attempt to connect to a signal that is already driven. The reason for the refusal may not be obvious because the signal symbol may appear elsewhere in the diagram.
  Right-click the link and select Highlight to find the other signal. Click anywhere on the diagram to disable the highlight.
- An attempt is made to repeat a link between two symbols. The reason for the refusal may not be obvious because the existing link may be represented elsewhere in the diagram.

1.6.3 Opto Signal Properties

Each opto input can be selected and used for programming in PSL. Activation of the opto input drives an associated DDB signal.

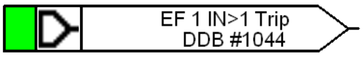
For example, activating opto input L1 asserts DDB 064 in the PSL.



1.6.4 Input Signal Properties

Relay logic functions provide logic output signals that can be used for programming in PSL. Depending on the relay functionality, operation of an active relay function drives an associated DDB signal in PSL.

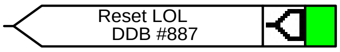
For example, DDB 1044 is asserted in the PSL if the HV earth fault, stage 1 protection operates or trips.



1.6.5 Output Signal Properties

Relay logic functions provide logic input signals that can be used for programming in PSL. Depending on the relay functionality, activation of the output signal drives an associated DDB signal in PSL and causes an associated response to the relay function.

For example, if DDB 887 is asserted in the PSL, it resets the loss of life.

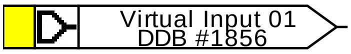


1.6.6 GOOSE Input Signal Properties

The PSL interfaces with the GOOSE Scheme Logic using virtual inputs. 64 virtual inputs are used in software versions 02, 03 and 04. The virtual inputs can be used a similar way to the opto input signals.

The logic that drives each of the virtual inputs is in the relay's GOOSE Scheme Logic file. Any number of bit-pairs, from any enrolled device, can be mapped using logic gates onto a virtual input.

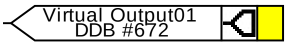
For example, in software versions 04, DDB 1856 is asserted in PSL if virtual input 1 and its associated bit pair operate.



1.6.7 GOOSE Output Signal Properties

The PSL interfaces with the GOOSE Scheme Logic using 32 virtual outputs. Virtual outputs can be mapped to bit-pairs for transmitting to any enrolled devices.

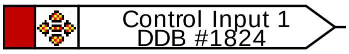
For example, in software version 04, if DDB 672 is asserted in PSL, virtual output 01 and its associated bit-pair mappings operate.



1.6.8 Control Input Signal Properties

There are 32 control inputs which can be activated using the relay menu, ‘hotkeys’ or using rear communications. Depending on the programmed setting (latched or pulsed), an associated DDB signal is activated in PSL when a control input is operated.

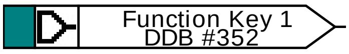
For example, operate control input 1 to assert DDB 1824 in the PSL.



1.6.9 Function Key Properties

Each function key can be selected and used for programming in PSL. Activation of the function key drives an associated DDB signal and the DDB signal remains active depending on the programmed setting (toggled or normal). Toggled mode means the DDB signal remains latched or unlatched on a key press. Normal mode means the DDB is only active for the duration of the key press.

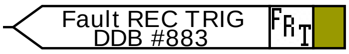
For example, operate function key 1 to assert DDB 352 in the PSL.



1.6.10 Fault Recorder Trigger Properties

The fault recording facility can be activated by driving the fault recorder trigger DDB signal.

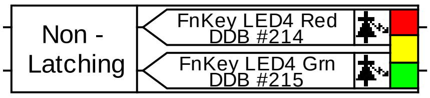
For example, assert DDB 883 to activate the fault recording in the PSL.

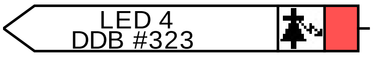


1.6.11 LED Signal Properties

All programmable LEDs drive associated DDB signals when the LED is activated.

For example, DDB 214 is asserted when tri-color LED 4 is activated (P643 and P645) and DDB 323 for red LED 4 (P642).

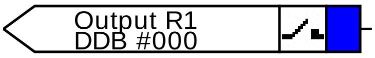




1.6.12 Contact Signal Properties

All relay output contacts drive an associated DDB signal when the output contact is activated.

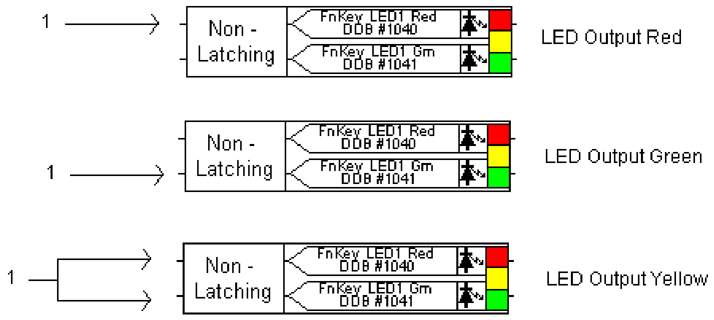
For example, DDB 000 is asserted when output R1 is activated.



1.6.13 LED Conditioner Properties

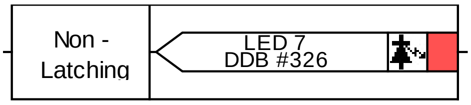
Tri-color LED Conditioner (P643/P645)

1. Select the LED name from the list (only shown when inserting a new symbol).
2. Configure the LED output to be Red, Yellow or Green.
3. Configure a Green LED by driving the Green DDB input.
4. Configure a RED LED by driving the RED DDB input.
5. Configure a Yellow LED by driving the RED and GREEN DDB inputs simultaneously.
6. Configure the LED output to be latching or non-latching.


1
Non - Latching
FnKey LED1 Red DDB #1040
FnKey LED1 Grn DDB #1041
LED Output Red
1
Non - Latching
FnKey LED1 Red DDB #1040
FnKey LED1 Grn DDB #1041
LED Output Green
1
Non - Latching
FnKey LED1 Red DDB #1040
FnKey LED1 Grn DDB #1041
LED Output Yellow

Red LED Conditioner (P642/P643/P645)

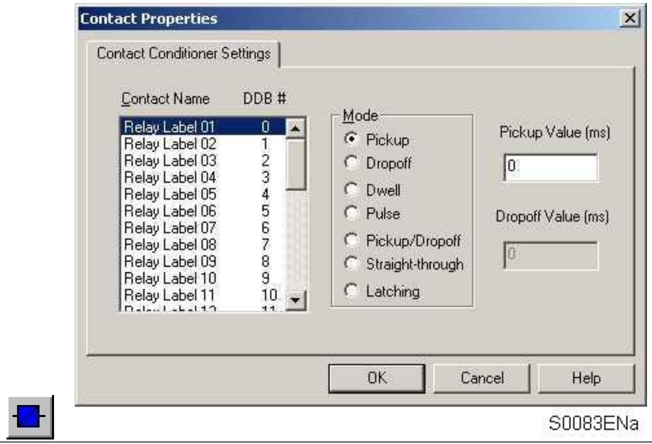
1. Select the LED name from the list (only shown when inserting a new symbol).
2. Configure the LED output to be latching or non-latching.


Non - Latching
LED 7
DDB #326

1.6.14 Contact Conditioner Properties

Each contact can be conditioned with an associated timer that can be selected for pick up, drop off, dwell, pulse, pick-up/drop-off, straight-through, or latching operation.

Straight-through means it is not conditioned at all whereas **Latching** is used to create a sealed-in or lockout type function.



Contact Properties

Contact Conditioner Settings

Contact Name	DDB #
Relay Label 01	0
Relay Label 02	1
Relay Label 03	2
Relay Label 04	3
Relay Label 05	4
Relay Label 06	5
Relay Label 07	6
Relay Label 08	7
Relay Label 09	8
Relay Label 10	9
Relay Label 11	10

Mode
● Pickup
○ Dropoff
○ Dwell
○ Pulse
○ Pickup/Dropoff
○ Straight-through
○ Latching

Pickup Value (ms): 0

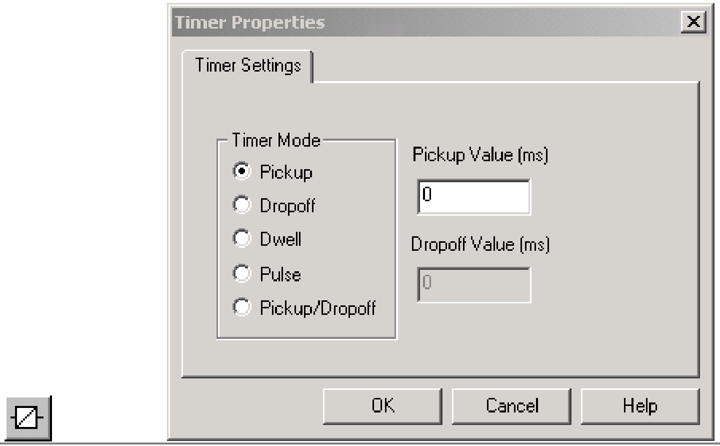
Dropoff Value (ms): 0

Figure 3 - Contact properties

1. Select the contact name from the Contact Name list (only shown when inserting a new symbol).
2. Choose the conditioner type required in the Mode tick list.
3. Set the Pick-up Time (in milliseconds), if required.
4. Set the Drop-off Time (in milliseconds), if required.

1.6.15 Timer Properties

Each timer can be selected for pick up, drop off, dwell, pulse or pick-up/drop-off operation.



Timer Properties

Timer Settings

Timer Mode
● Pickup
○ Dropoff
○ Dwell
○ Pulse
○ Pickup/Dropoff

Pickup Value (ms): 0

Dropoff Value (ms): 0

Figure 4 - Timer properties

1. Choose the operation mode from the **Timer Mode** list.
2. Set the pick-up time (in milliseconds), if required.
3. Set the drop-off time (in milliseconds), if required.

1.6.16 Gate Properties

A Gate may be an AND, OR, RS Flip-Flop or programmable gate.

- An **AND** gate requires that all inputs are TRUE for the output to be TRUE.

- An **OR** gate requires that one or more input is TRUE for the output to be TRUE.
- An **SR** gate is configured by an appropriate version of PSL Editor (S1v2.14 version 5.0.0 or greater) where an SRQ icon features on the toolbar.
- A **Programmable** gate requires that the number of inputs that are TRUE is equal to or greater than its ‘Inputs to Trigger’ setting for the output to be TRUE.

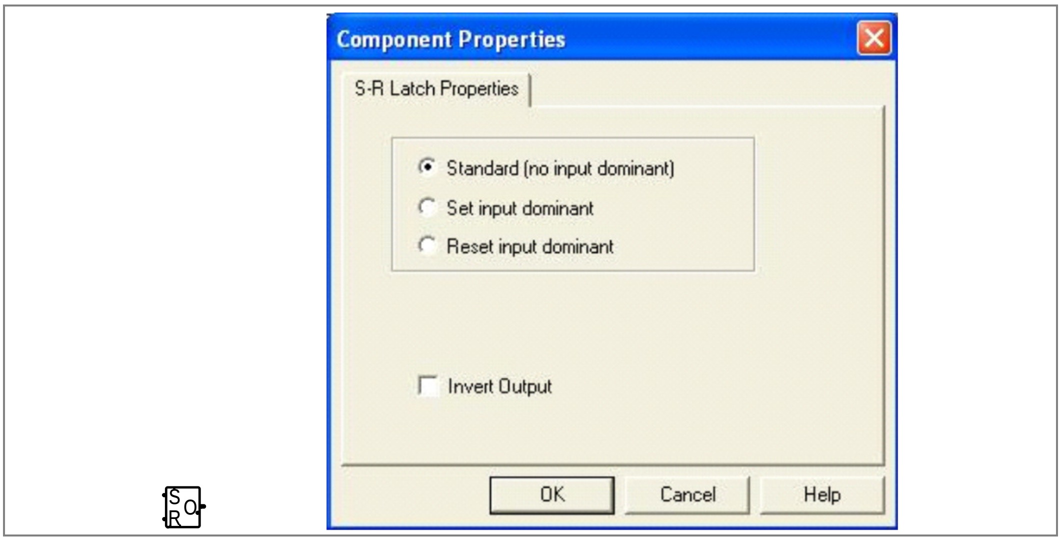
For many products a number of programmable SR Latches are added. They are configured by an appropriate version of PSL Editor (S1v2.14 version 5.0.0 or greater) where an SRQ icon features on the toolbar.

Each SR latch has a Q output. The Q output may be inverted in the PSL Editor under the SR Latch component properties window. The SR Latches may be configured as Standard (no input dominant), Set Dominant or Reset Dominant in the PSL Editor under the SR Latch component properties window. The truth table for the SR Latches is given below.

A **Programmable** SR gate can be selected to operate with these latch properties:

S input	R input	O - Standard	O – Set input dominant	O – Rest input dominant
0	0	0	0	0
0	1	0	0	0
1	0	1	1	1
1	1	0	1	1

Table 1 - SR programmable gate properties

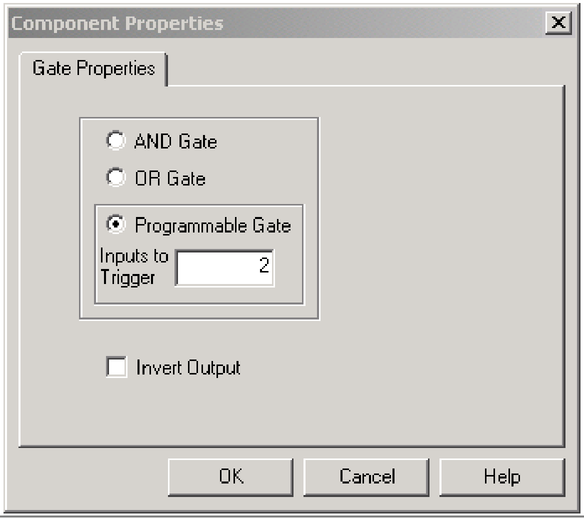


● Standard (no input dominant)
○ Set input dominant
○ Reset input dominant

☐ Invert Output

Figure 5 - SR latch component properties

Select if the output of the gate should be inverted using the Invert Output check box. An inverted output is indicated with a "bubble" on the gate output.



Component Properties
Gate Properties
OK
Cancel
Help

○ AND Gate

○ OR Gate

● Programmable Gate

Inputs to Trigger: 2

☐ Invert Output

Figure 6 - Gate properties

1. Select the Gate type: AND, OR, RS Flip-Flop or Programmable.
2. Set the number of inputs to trigger when **Programmable Gate** is selected.
3. Select whether the output of the gate should be inverted using the Invert Output check box. An inverted output is indicated with a small circle on the gate output.

2 DESCRIPTION OF LOGIC NODES

DDB no.	English text	Source	Description	Relay model
0	Output R1 (User definable)	SW	Output Relay 1 is on	P642 max 12 output P643 max 24 output P645 max 24 output
23	Output R24 (User definable)	SW	Output Relay 24 is on	P642 max 12 output P643 max 24 output P645 max 24 output
24 to 63	Not used			
64	Input L1 (User definable)	SW	Opto Isolator 1 is on	P642 max 12 opto P643 max 24 opto P645 max 24 opto
87	Input L24 (User definable)	SW	Opto Isolator 24 is on	P642 max 12 opto P643 max 24 opto P645 max 24 opto
88 to 127	Not used			
128	Relay Cond 1	PSL	Input signal driving relay 1 is on	P642 max 12 P643 max 24 P645 max 24
151	Relay Cond 24	PSL	Input signal driving relay 24 is on	P642 max 12 P643 max 24 P645 max 24
152 to 191	Not used			
192	LED1 Red	PSL	Tri-LED - 1 – Red	P643 / P645
193	LED1 Grn	PSL	Tri-LED - 1 – Green	P643 / P645
206	LED8 Red	PSL	Tri-LED - 8 – Red	P643 / P645
207	LED8 Grn	PSL	Tri-LED - 8 – Green	P643 / P645
208	FnKey LED1 Red	PSL	Tri-LED - 9 – Red	P643 / P645
209	FnKey LED1 Grn	PSL	Tri-LED - 9 – Green	P643 / P645
226	FnKey LED10 Red	PSL	Tri-LED - 18 – Red	P643 / P645
227	FnKey LED10 Grn	PSL	Tri-LED - 18 - Green	P643 / P645
228 to 255	Not used			
256	LED1 Con R	PSL	Tri-LED Conditioner - 1 - Red	P643 / P645
257	LED1 Con G	PSL	Tri-LED Conditioner- 1 - Green	P643 / P645
270	LED8 Con R	PSL	Tri-LED Conditioner - 8 - Red	P643 / P645
271	LED8 Con G	PSL	Tri-LED Conditioner - 8 - Green	P643 / P645
272	FnKey LED1 ConR	PSL	Tri-LED Conditioner - 9 - Red	P643 / P645
273	FnKey LED1 ConG	PSL	Tri-LED Conditioner - 9 - Green	P643 / P645
290	FnKey LED10 ConR	PSL	Tri-LED Conditioner - 18 - Red	P643 / P645
291	FnKey LED10 ConG	PSL	Tri-LED Conditioner - 18 - Green	P643 / P645
292 to 319	Not used			
320	LED 1	SW	LED 1	P642
327	LED 8	SW	LED 8	P642
328	LED Cond IN 1	PSL	LED Conditioner IN 1	P642
335	LED Cond IN 8	PSL	LED Conditioner IN 8	P642
336 to 351	Not used			
352	Function Key 1	SW	Function Key 1	P643 / P645

DDB no.	English text	Source	Description	Relay model
361	Function Key 10	SW	Function Key 10	P643 / P645
362 to 383	Not used			
384	Timer out 1	SW	Auxiliary Timer out 1	P642 / P643 / P645
399	Timer out 16	SW	Auxiliary Timer out 16	P642 / P643 / P645
400 to 415	Not used			
416	Timer in 1	PSL	Auxiliary Timer in 1	P642 / P643 / P645
431	Timer in 16	PSL	Auxiliary Timer in 16	P642 / P643 / P645
432 to 449	Not used			
450	SG-DDB Invalid	SW	Setting Group selection by DDB inputs invalid	P642 / P643 / P645
451	CB Status Alarm	SW	Circuit breaker status alarm (this DDB is not operative because the CB Monitoring function is not available)	P642 / P643 / P645
452	RTD Thermal Alm	FL	Operation of any RTD 1-10 Alarm	P642 / P643 / P645
453	RTD Open Cct	SW	RTD Open Circuit Failure	P642 / P643 / P645
454	RTD short Cct	SW	RTD Short Circuit Failure	P642 / P643 / P645
455	RTD Data Error	SW	RTD Data Inconsistency Error	P642 / P643 / P645
456	RTD Board Fail	SW	RTD Board Failure	P642 / P643 / P645
457	CL Input 1 Alarm	SW	Current Loop Input 1 Alarm	P642 / P643 / P645
458	CL Input 2 Alarm	SW	Current Loop Input 2 Alarm	P642 / P643 / P645
459	CL Input 3 Alarm	SW	Current Loop Input 3 Alarm	P642 / P643 / P645
460	CL Input 4 Alarm	SW	Current Loop Input 4 Alarm	P642 / P643 / P645
461	CLI1 I< Fail Alm	SW	Current Loop Input 1 Undercurrent Fail Alarm	P642 / P643 / P645
462	CLI2 I< Fail Alm	SW	Current Loop Input 2 Undercurrent Fail Alarm	P642 / P643 / P645
463	CLI3 I< Fail Alm	SW	Current Loop Input 3 Undercurrent Fail Alarm	P642 / P643 / P645
464	CLI4 I< Fail Alm	SW	Current Loop Input 4 Undercurrent Fail Alarm	P642 / P643 / P645
465	Prot'n Disabled	SW	Protection Disabled - typically out of service due to test mode	P642 / P643 / P645
466	F out of range	FL	Frequency out of range	P642 / P643 / P645
467 to 469	Not used			
470	CL Card I/P Fail	SW	Current loop card input fail	P642 / P643 / P645
471	CL Card O/P Fail	SW	Current loop card output fail	P642 / P643 / P645
472	VCO1 Config err	SW	The VCO1 configuration error alarm is issued when the current input configured in VCO>1 setting cell is not located at the same transformer terminal as the main VT.	P642 / P643 / P645
473	VCO2 Config err	SW	The VCO2 configuration error alarm is issued when the current input configured in VCO>2 setting cell is not located at the same transformer terminal as the main VT.	P642 / P643 / P645
474	Not used			
475	CT Fail Alarm	SW	The Current transformer supervision fail alarm is asserted when an unbalanced fault is detected in the current input secondary circuit.	P642 / P643 / P645
476	Circuity Flt Alm	SW	Circuity fault alarm (to be used in busbar applications only)	P642 / P643 / P645
477	VT Fail Alarm	SW	Voltage transformer supervision fail alarm	P642 / P643 / P645
478	ThermalPtrp Alm	SW	Thermal protection pretrip alarm	P642 / P643 / P645
479	FAA alarm	SW	Ageing acceleration factor alarm	P642 / P643 / P645
480	LOL alarm	SW	Loss of life alarm	P642 / P643 / P645
481	Breaker Fail	SW	Breaker failure alarm	P642 / P643 / P645
482	CT para mismatch	SW	The Current transformer para-mismatch alarm is issued when any of the matching factors is out of range.	P642 / P643 / P645

DDB no.	English text	Source	Description	Relay model
483	CT Selection Alm	SW	The CT selection alarm is asserted if one current input is assigned to more than one terminal.	P642 / P643 / P645
484	SinglePha CT Alm	SW	The single phase CT selection alarm is asserted if any of the single phase CTs is assigned at the same time to the high impedance REF and any other protection function such as earth fault current or circuit breaker failure.	P642 / P643 / P645
485	insuff No. of CT	SW	The insufficient number of CT alarm is asserted when only one CT is left for the differential function.	P642 / P643 / P645
486	Disc CT invalid	SW	The disconnected CT invalid status alarm is issued when the CT stored status does not match the status after the power supply is re-established.	P642 / P643 / P645
487	HV-LZREF sf OOR	SW	HV LowZ REF scaling factor out of range	P642 / P643 / P645
488	LV-LZREF sf OOR	SW	LV LowZ REF scaling factor out of range	P642 / P643 / P645
489	TV-LZREF sf OOR	SW	TV LowZ REF scaling factor out of range	P643 / P645
490	AutoLZREF sf OOR	SW	Auto LowZ REF scaling factor out of range	P642 / P643 / P645
491 to 500	Not used			
501	W1 V/Hz>1 Alarm	SW	Overfluxing element 1 alarm	P643 / P645 / Requires three phase VT input.
502	W1 V/Hz>2 PrTrp	SW	Overfluxing element 1 pre-trip alarm. It is asserted when the time left to trip is equal to the pre-trip time in the setting file.	P643 / P645 / Requires three phase VT input.
503	W2 V/Hz>1 Alarm	SW	Overfluxing element 2 alarm	P642 / P643 / P645
504	W2 V/Hz>2 PrTrp	SW	Overfluxing element 2 pre-trip alarm. It is asserted when the time left to trip is equal to the pre-trip time in the setting file.	P642 / P643 / P645
505 to 506	Not Used			
507	Freq Prot Alm	SW	Frequency Protection Alarm	P642 / P643 / P645
508	Through flt Alm	SW	Through fault monitoring alarm	P642 / P643 / P645
509 to 511	Not Used			
512	Battery Fail	SW	Battery Fail alarm indication	P642 / P643 / P645
513	Field Volts Fail	SW	Field Voltage Failure	P642 / P643 / P645
514	Not Used			
515	GOOSE IED Absent	SW	Enrolled GOOSE IED absent alarm indication	P642 / P643 / P645
516	NIC Not Fitted	SW	Network Interface Card not fitted/failed alarm	P642 / P643 / P645
517	NIC No Response	SW	Network Interface Card not responding alarm	P642 / P643 / P645
518	NIC Fatal Error	SW	Network Interface Card fatal error alarm indication	P642 / P643 / P645
519	NIC Soft. Reload	SW	Network Interface Card software reload alarm	P642 / P643 / P645
520	Bad TCP/IP Cfg.	SW	Bad TCP/IP Configuration Alarm	P642 / P643 / P645
521	Bad OSI Config.	SW	Bad OSI Configuration Alarm. Not in use as it corresponds to UCA2.	P642 / P643 / P645
522	NIC Link Fail	SW	Network Interface Card link fail alarm indication	P642 / P643 / P645
523	NIC SW Mis-Match	SW	Main card/NIC software mismatch alarm indication	P642 / P643 / P645
524	IP Addr Conflict	SW	IP address conflict alarm indication	P642 / P643 / P645
525 to 550	Not used			
551	Block Transdiff	PSL	Block Transformer Differential protection	P642 / P643 / P645
552	2nd Harmonic A	SW	The 2nd Harmonic A is asserted when the ratio of second harmonic to fundamental of the phase A differential current exceeds the setting. If the 2nd Harmonic A is asserted, then the low set phase A differential element is blocked.	P642 / P643 / P645

DDB no.	English text	Source	Description	Relay model
553	2nd Harmonic B	SW	The 2nd Harmonic B is asserted when the ratio of second harmonic to fundamental of the phase B differential current exceeds the setting. If the 2nd Harmonic B is asserted, then the low set phase B differential element is blocked.	P642 / P643 / P645
554	2nd Harmonic C	SW	The 2nd Harmonic C is asserted when the ratio of second harmonic to fundamental of the phase C differential current exceeds the setting. If the 2nd Harmonic C is asserted, then the low set phase C differential element is blocked.	P642 / P643 / P645
555	5nd Har Blk A	SW	The 5th Harmonic A is asserted when the ratio of fifth harmonic to fundamental of the phase A differential current exceeds the setting. If the 5th Harmonic A is asserted, then the low set phase A differential element is blocked.	P642 / P643 / P645
556	5nd Har Blk B	SW	The 5th Harmonic B is asserted when the ratio of fifth harmonic to fundamental of the phase B differential current exceeds the setting. If the 5th Harmonic B is asserted, then the low set phase B differential element is blocked.	P642 / P643 / P645
557	5nd Har Blk C	SW	The 5th Harmonic C is asserted when the ratio of second harmonic to fundamental of the phase C differential current exceeds the setting. If the 5th Harmonic C is asserted, then the low set phase C differential element is blocked.	P642 / P643 / P645
558 to 561	Not used			
562	V<1 timer block	PSL	Blocks phase under voltage stage 1 time delay trip	P643 / P645 / Requires three phase VT input.
563	V<2 timer block	PSL	Blocks phase under voltage stage 2 time delay trip	P643 / P645 / Requires three phase VT input.
564	V>1 timer block	PSL	Blocks phase over voltage stage 1 time delay trip	P643 / P645 / Requires three phase VT input.
565	V>2 timer block	PSL	Blocks phase over voltage stage 2 time delay trip	P643 / P645 / Requires three phase VT input.
566	VN>1 timer block	PSL	Blocks residual over voltage stage 1 time delay trip	P643 / P645 / Requires three phase VT input.
567	VN>2 timer block	PSL	Blocks residual over voltage stage 2 time delay trip	P643 / P645 / Requires three phase VT input.
568-570	Not used			
571	Inhibit CTS	PSL	Inhibits current transformer supervision logic	P642 / P643 / P645
572	CTS BLK	SW	Output from the current transformer supervision logic. It indicates that any of the CT circuits has a problem. It may be used to block the differential element if required. It is only operative if the CTS is set to restraint.	P642 / P643 / P645
573	CTS CT1	SW	Output from the current transformer supervision logic. It indicates that the current transformer 1 circuit has a problem. It is only operative if the CTS is set to restraint.	P642 / P643 / P645
577	CTS CT5	PSL	Output from the current transformer supervision logic. It indicates that the current transformer 5 circuit has a problem. It is only operative if the CTS is set to restraint.	P642 / P643 / P645
578	CT1 Fail	SW	Output from the current transformer supervision logic. It indicates that the current transformer 1 circuit has a problem. It is operative whether the CTS is set to restraint or indication.	P642 / P643 / P645
582	CT5 Fail	SW	Output from the current transformer supervision logic. It indicates that the current transformer 5 circuit has a problem. It is operative whether the CTS is set to restraint or indication.	P642 / P643 / P645
583 to 587	Not used			
588	Blk TOL	PSL	Input to the thermal overload function. When asserted, it blocks the thermal overload function.	P642 / P643 / P645

DDB no.	English text	Source	Description	Relay model
589	CTS HV	SW	HV winding current transformer supervision. It is asserted when any of the current transformer supervision associated to the current inputs assigned to the HV winding is asserted. It is only operative if the CTS is set to restraint.	P642 / P643 / P645
590	CTS LV	SW	LV winding current transformer supervision. It is asserted when any of the current transformer supervision associated to the current inputs assigned to the LV winding is asserted. It is only operative if the CTS is set to restraint.	P642 / P643 / P645
591	CTS TV	SW	TV winding current transformer supervision. It is asserted when any of the current transformer supervision associated to the current inputs assigned to the TV winding is asserted. It is only operative if the CTS is set to restraint.	P643 / P645
592	Inhibit VTS	PSL	Input to the voltage transformer supervision logic. When asserted, it inhibits the VTS.	P642 / P643 / P645 / Requires two single phase VT inputs in P642. / Requires three phase VT input in P643 and P645.
593	Not used			
594	Blk REF HV	PSL	Input to the high voltage restricted earth fault element. When asserted, it blocks the HV REF.	P642 / P643 / P645
595	Blk REF LV	PSL	Input to the low voltage restricted earth fault element. When asserted, it blocks the LV REF.	P642 / P643 / P645
596	Blk REF TV	PSL	Input to the tertiary voltage restricted earth fault element. When asserted, it blocks the TV REF.	P643 / P645
597	Blk REF Auto	PSL	Input to the autotransformer restricted earth fault element. When asserted, it blocks the autotransformer REF.	P642 / P643 / P645
598	POC 1 I>1 TBlk	PSL	Blocks the stage 1 time delayed trip of the phase overcurrent 1.	P642 / P643 / P645
601	POC 1 I>4 TBlk	PSL	Blocks the stage 4 time delayed trip of the phase overcurrent 1.	P642 / P643 / P645
602	Not used			
603	POC 2 I>1 TBlk	PSL	Blocks the stage 1 time delayed trip of the phase overcurrent 2.	P642 / P643 / P645
606	POC 2 I>4 TBlk	PSL	Blocks the stage 4 time delayed trip of the phase overcurrent 2.	P642 / P643 / P645
607	Not used			
608	POC 3 I>1 TBlk	PSL	Blocks the stage 1 time delayed trip of the phase overcurrent 3.	P643 / P645
611	POC 3 I>4 TBlk	PSL	Blocks the stage 4 time delayed trip of the phase overcurrent 3.	P643 / P645
612	CBF1 Timer1 Blk	PSL	Blocks timer 1 of the circuit breaker failure function associated to breaker 1.	P642 / P643 / P645
613	CBF1 Timer2 Blk	PSL	Blocks timer 2 of the circuit breaker failure function associated to breaker 1.	P642 / P643 / P645
614	CBF2 Timer1 Blk	PSL	Blocks timer 1 of the circuit breaker failure function associated to breaker 2.	P642 / P643 / P645
615	CBF2 Timer2 Blk	PSL	Blocks timer 2 of the circuit breaker failure function associated to breaker 2.	P642 / P643 / P645
616	CBF3 Timer1 Blk	PSL	Blocks timer 1 of the circuit breaker failure function associated to breaker 3.	P643 / P645
617	CBF3 Timer2 Blk	PSL	Blocks timer 2 of the circuit breaker failure function associated to breaker 3.	P643 / P645
618	CBF4 Timer1 Blk	PSL	Blocks timer 1 of the circuit breaker failure function associated to breaker 4.	P645
619	CBF4 Timer2 Blk	PSL	Blocks timer 2 of the circuit breaker failure function associated to breaker 4.	P645
620	CBF5 Timer1 Blk	PSL	Blocks timer 1 of the circuit breaker failure function associated to breaker 5.	P645

DDB no.	English text	Source	Description	Relay model
621	CBF5 Timer2 Blk	PSL	Blocks timer 2 of the circuit breaker failure function associated to breaker 5.	P645
622 to 637	Not used			
638	F<1 Timer Block	PSL	Blocks the underfrequency stage 1 time delayed trip.	P642 / P643 / P645
641	F<4 Timer Block	PSL	Blocks the underfrequency stage 4 time delayed trip.	P642 / P643 / P645
642	F>1 Timer Block	PSL	Blocks the overfrequency stage 1 time delayed trip.	P642 / P643 / P645
643	F>2 Timer Block	PSL	Blocks the overfrequency stage 4 time delayed trip.	P642 / P643 / P645
644	HV StubBus Enabl	PSL	Input to the high voltage stub bus element. When asserted, it enables the HV stub bus element. This DDB considers the status of the HV winding isolator.	P642 / P643 / P645
645	LV StubBus Enabl	PSL	Input to the low voltage stub bus element. When asserted, it enables the LV stub bus element. This DDB considers the status of the LV winding isolator.	P642 / P643 / P645
646	TV StubBus Enabl	PSL	Input to the tertiary voltage stub bus element. When asserted, it enables the TV stub bus element. This DDB considers the status of the TV winding isolator.	P643 / P645
647	HV StubBus Act	PSL	Output from the HV stub bus logic. If asserted, the HV stub bus is active.	P642 / P643 / P645
648	LV StubBus Act	PSL	Output from the LV stub bus logic. If asserted, the LV stub bus is active.	P642 / P643 / P645
649	TV StubBus Act	PSL	Output from the TV stub bus logic. If asserted, the TV stub bus is active.	P643 / P645
650	Stop Freq Track	PSL	Internal signal from the frequency tracking element. It is not available for customer use.	P642 / P643 / P645
651	EF1 IN>1 TimeBlk	PSL	Blocks the stage 1 time delayed trip of earth fault 1.	P642 / P643 / P645
654	EF1 IN>4 TimeBlk	PSL	Blocks the stage 4 time delayed trip of earth fault 1.	P642 / P643 / P645
655	EF2 IN>1 TimeBlk	PSL	Blocks the stage 1 time delayed trip of earth fault 2.	P642 / P643 / P645
658	EF2 IN>4 TimeBlk	PSL	Blocks the stage 4 time delayed trip of earth fault 2.	P642 / P643 / P645
659	EF3 IN>1 TimeBlk	PSL	Blocks the stage 1 time delayed trip of earth fault 3.	P643 / P645
662	EF3 IN>4 Timer Blk	PSL	Blocks the stage 4 time delayed trip of earth fault 3.	P643 / P645
663	V2>1 Accelerate	PSL	If V2>1 is asserted, then the operating time of the function is accelerated from typically 80 ms to 40 ms when set to instantaneous.	P642 / P643 / P645
664	VCO VAB<1	SW	Voltage controlled overcurrent stage 1 phase A start signal	P642 / P643 / P645
665	VCO VBC<1	SW	Voltage controlled overcurrent stage 1 phase B start signal	P642 / P643 / P645
666	VCO VCA<1	SW	Voltage controlled overcurrent stage 1 phase C start signal	P642 / P643 / P645
667	VCO VAB<2	SW	Voltage controlled overcurrent stage 2 phase A start signal	P642 / P643 / P645
668	VCO VBC<2	SW	Voltage controlled overcurrent stage 2 phase B start signal	P642 / P643 / P645
669	VCO VCA<2	SW	Voltage controlled overcurrent stage 2 phase C start signal	P642 / P643 / P645
670	VCO I>1 TimeBlk	PSL	Blocks stage 1 time delayed trip of the voltage controlled overcurrent element.	P642 / P643 / P645
671	VCO I>21 TimeBlk	PSL	Blocks stage 2 time delayed trip of the voltage controlled overcurrent element.	P642 / P643 / P645
672	Virtual output 01	PSL	Goose output 01	P642 / P643 / P645
703	Virtual output 32	PSL	Goose output 32	P642 / P643 / P645
704	CT1 excluded	SWPSL	CT1 is excluded from the protection functions.	P642 / P643 / P645

DDB no.	English text	Source	Description	Relay model
705	CT2 excluded	SWPSL	CT2 is excluded from the protection functions.	P642 / P643 / P645
706	CT3 excluded	SWPSL	CT3 is excluded from the protection functions.	P643 / P645
707	CT4 excluded	SWPSL	CT4 is excluded from the protection functions.	P645
708	CT5 excluded	SWPSL	CT5 is excluded from the protection functions.	P645
709	CM Select 1X	PSL	CM Select 1X is used together with CM Select X1 to configure the cooling mode selector in PSL. This selector allows choosing one of four cooling modes.	P642 / P643 / P645
710	CM Select X1	PSL	CM Select 1X is used together with CM Select X1 to configure the cooling mode selector in PSL. This selector allows choosing one of four cooling modes.	P642 / P643 / P645
711	Not used			
712	BLK W1 VPERHZ>1	PSL	Blocks the stage 1 of overfluxing element 1	P643 / P645 / Requires three phase VT input.
713	BLK W2 VPERHZ>1	PSL	Blocks the stage 1 of overfluxing element 2	P643 / P645 / Requires three phase VT input.
714	CL Input 1 Blk	PSL	Blocks Current Loop Input 1 protection	P642 / P643 / P645
717	CL Input 4 Blk	PSL	Blocks Current Loop Input 4 protection	P642 / P643 / P645
718	CB1 Alarm	PSL	Circuit breaker 1 alarm indication	P642 / P643 / P645
719	CB1 Closed	PSL	Monitors the status of circuit breaker 1. The status of the CB is required by the dead pole logic.	P642 / P643 / P645
726	CB5 Alarm	PSL	Circuit breaker 5 alarm indication	P645
727	CB5 Closed	PSL	Monitors the status of circuit breaker 5. The status of the CB is required by the dead pole logic.	P645
728-735	Not used			
736	CT Exclu Ena	PSL	Input to the current transformer exclusion logic. It is one of the conditions that must be true for T1/2/3/4/5 CTCT1 to be excluded from the protection functions.	P642 / P643 / P645
737	CT1 Exclu Ena	PSL	Input to the current transformer exclusion logic. It is one of the conditions that must be true for T1 CTCT1 to be excluded from the protection functions.	P642 / P643 / P645
738	CT2 Exclu Ena	PSL	Input to the current transformer exclusion logic. It is one of the conditions that must be true for T2 CTCT2 to be excluded from the protection functions.	P642 / P643 / P645
739	CT3 Exclu Ena	PSL	Input to the current transformer exclusion logic. It is one of the conditions that must be true for T3 CTCT3to be excluded from the protection functions.	P643 / P645
740	CT4 Exclu Ena	PSL	Input to the current transformer exclusion logic. It is one of the conditions that must be true for T4 CTCT4 to be excluded from the protection functions.	P645
741	CT5 Exclu Ena	PSL	Input to the current transformer exclusion logic. It is one of the conditions that must be true for T5 CTCT5 to be excluded from the protection functions.	P645
742	CT Saturation A	SW	Current transformer saturation is detected in phase A of the differential current.	P642 / P643 / P645
743	CT Saturation B	SW	Current transformer saturation is detected in phase B of the differential current.	P642 / P643 / P645
744	CT Saturation C	SW	Current transformer saturation is detected in phase C of the differential current.	P642 / P643 / P645
745	MAX_OVER_A	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it indicates that the maximum phase A differential current is above the positive threshold.	P642 / P643 / P645

DDB no.	English text	Source	Description	Relay model
746	MAX_OVER_B	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it indicates that the maximum phase B differential current is above the positive threshold.	P642 / P643 / P645
747	MAX_OVER_C	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it indicates that the maximum phase C differential current is above the positive threshold.	P642 / P643 / P645
748	MIN_UNDER_A	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it indicates that the minimum phase A differential current is below the negative threshold.	P642 / P643 / P645
749	MIN_UNDER_B	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it indicates that the minimum phase B differential current is below the negative threshold.	P642 / P643 / P645
750	MIN_UNDER_C	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it indicates that the minimum phase C differential current is below the negative threshold.	P642 / P643 / P645
751	SEG_VALID_A	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it indicates that angle between the maximum and minimum phase A differential current is greater than the threshold.	P642 / P643 / P645
752	SEG_VALID_B	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it indicates that angle between the maximum and minimum phase B differential current is greater than the threshold.	P642 / P643 / P645
753	SEG_VALID_C	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it indicates that angle between the maximum and minimum phase C differential current is greater than the threshold.	P642 / P643 / P645
754	1_MAX_DEL3_A	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it is related to the maximum third derivative of phase A differential current.	P642 / P643 / P645
755	1_MAX_DEL3_B	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it is related to the maximum third derivative of phase B differential current.	P642 / P643 / P645
756	1_MAX_DEL3_C	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it is related to the maximum third derivative of phase C differential current.	P642 / P643 / P645
757	MAX_DEL1_A	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it is related to the maximum first derivative of phase A differential current.	P642 / P643 / P645
758	MAX_DEL1_B	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it is related to the maximum first derivative of phase B differential current.	P642 / P643 / P645
759	MAX_DEL1_C	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it is related to the maximum first derivative of phase C differential current.	P642 / P643 / P645
760	DEL3 > Thres A	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it indicates that the maximum third derivative of phase A differential current exceeds the threshold.	P642 / P643 / P645
761	DEL3 > Thres B	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic and it indicates that the maximum third derivative of phase B differential current exceeds the threshold.	P642 / P643 / P645
762	DEL3 > Thres C	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic and it indicates that the maximum third derivative of phase C differential current exceeds the threshold.	P642 / P643 / P645

DDB no.	English text	Source	Description	Relay model
763	1>2K DEL3 A	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it is related to the third derivative of phase A differential current.	P642 / P643 / P645
764	1>2K DEL3 B	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it is related to the third derivative of phase B differential current.	P642 / P643 / P645
765	1>2K DEL3 C	SW	This is a hidden DDB not available for customer use. It is used by the CT saturation detection logic, and it is related to the third derivative of phase C differential current.	P642 / P643 / P645
766-767	Not used			
768	User alarm 1	PSL	User alarm 1 follows the status of the signal associated to it in PSL. For example, if opto-input 1 is configured to user alarm 1, then user alarm 1 follows the status of opto-input 1.	P642 / P643 / P645
799	User alarm 32	PSL	User alarm 32 follows the status of the signal associated to it in PSL. For example, if opto-input 1 is configured to user alarm 32, then user alarm 32 follows the status of opto-input 1.	P642 / P643 / P645
800	User alarm in 1	FL	User alarm 1 is asserted. If the user alarm 1 is configured as manual reset, then User alarm in 1 is non-volatile.	P642 / P643 / P645
831	User alarm in 32	FL	User alarm 32 is asserted. If the user alarm 32 is configured as manual reset, then User alarm in 32 is non-volatile.	P642 / P643 / P645
832-838	Not used			
839	External Fault A	SW	External/internal fault detector A phase output. It blocks the effect of A phase CT saturation or no gap detection algorithms during A phase external faults. It indicates that there is an external A phase fault when asserted.	P642 / P643 / P645
840	External Fault B	SW	External/internal fault detector B phase output. It blocks the effect of B phase CT saturation or no gap detection algorithms during B phase external faults. It indicates that there is an external A phase fault when asserted.	P642 / P643 / P645
841	External Fault C	SW	External/internal fault detector C phase output. It blocks the effect of C phase CT saturation or no gap detection algorithms during C phase external faults. It indicates that there is an external C phase fault when asserted.	P642 / P643 / P645
842-844	Not used			
845	Phase A Circuity Flt	SW	Phase A circuitry fault alarm indicates there is a problem in the phase A - AC wiring.	P642 / P643 / P645
846	Phase B Circuity Flt	SW	Phase B circuitry fault alarm indicates there is a problem in the phase B - AC wiring.	P642 / P643 / P645
847	Phase C Circuity Flt	SW	Phase C circuitry fault alarm indicates there is a problem in the phase C - AC wiring.	P642 / P643 / P645
848	Not used			
849	Inhibit NPSOC 1	PSL	Inhibits the element 1 negative phase sequence overcurrent function.	P642 / P643 / P645
850	NOC 1 I2>1 TBlk	PSL	Blocks the element 1 negative phase sequence overcurrent stage 1 time delayed trip.	P642 / P643 / P645
853	NOC 1 I2>4 TBlk	PSL	Blocks the element 1 negative phase sequence overcurrent stage 4 time delayed trip.	P642 / P643 / P645
854	Inhibit NPSOC 2	PSL	Inhibits the element 2 negative phase sequence overcurrent function.	P642 / P643 / P645
855	NOC 2 I2>1 TBlk	PSL	Blocks the element 2 negative phase sequence overcurrent stage 1 time delayed trip.	P642 / P643 / P645
858	NOC 2 I2>4 TBlk	PSL	Blocks the element 2 negative phase sequence overcurrent stage 4 time delayed trip.	P642 / P643 / P645
859	Inhibit NPSOC 3	PSL	Inhibits the element 3 negative phase sequence overcurrent function.	P643 / P645

DDB no.	English text	Source	Description	Relay model
860	NOC 3 I2>1 TBlk	PSL	Blocks the element 3 negative phase sequence overcurrent stage 1 time delayed trip	P643 / P645
863	NOC 3 I2>4 TBlk	PSL	Blocks the element 3 negative phase sequence overcurrent stage 4 time delayed trip	P643 / P645
864	Commissioning Test	SW	Monitor Port 1	P642 / P643 / P645
871	Commissioning Test	SW	Monitor Port 8	P642 / P643 / P645
872 to 873	Not Used			
874	MCB/VTS	PSL	Input to the VTS logic. Signal from external miniature circuit breaker.	P642 / P643 / P645 / Requires two single phase VT inputs in P642. / Requires three phase VT input in P643 and P645.
875	Not used			
876	Reset Relays/LED	PSL	Reset Latched Relays & LEDs	P642 / P643 / P645
877	Not used			
878	TFR de-energized	PSL	When asserted, the transformer is not connected to the power system so all circuit breakers are open. This signal is linked by software to the thermal function.	P642 / P643 / P645
879	Monitor Blocked	PSL	IEC60870-5-103 Monitor Blocking	P642 / P643 / P645
880	Command Blocked	PSL	IEC60870-5-103 Command Blocking	P642 / P643 / P645
881	Time Synch	PSL	Time synchronism by opto-input to nearest minute on 0-1 change	P642 / P643 / P645
882	Test Mode	PSL	Initiate Test Mode	P642 / P643 / P645
883	Fault REC TRIG	PSL	Fault Record Trigger Input	P642 / P643 / P645
884	SG Select x1	PSL	Setting Group Selector x1 (bit 0)	P642 / P643 / P645
885	SG Select 1x	PSL	Setting Group Selector 1x (bit 1)	P642 / P643 / P645
886	Any Trip	PSL	Any Trip	P642 / P643 / P645
887	Reset LOL	PSL	Resets Loss of life	P642 / P643 / P645
888	Reset Thermal	PSL	Resets Thermal Overload	P642 / P643 / P645
889	W1 Reset V/Hz	PSL	Resets overflux element 1	P643 / P645 / Requires three phase VT input.
890	W2 Reset V/Hz	PSL	Resets overlux element 2	P642 / P643 / P645 / Requires two single phase VT inputs in P642. / Requires three phase VT input in P643 and P645.
891	Trip Initial	FL	Trip Initial (DDB input signal), equivalent to the Any Trip signal (DDB output signal)	P642 / P643 / P645
892	Reset CcT Fail	PSL	Resets the circuitry fault alarm	P642 / P643 / P645
893-898	Not used			
899	Idiff Trip A	SW	Phase A differential trip	P642 / P643 / P645
900	Idiff Trip B	SW	Phase B differential trip	P642 / P643 / P645
901	Idiff Trip C	SW	Phase C differential trip	P642 / P643 / P645
902	Idiff Trip	SW	Differential trip	P642 / P643 / P645
903	Idiff HS1 Trip A	SW	Phase A high set 1 differential trip	P642 / P643 / P645
904	Idiff HS1 Trip B	SW	Phase B high set 1 differential trip	P642 / P643 / P645
905	Idiff HS1 Trip C	SW	Phase C high set 1 differential trip	P642 / P643 / P645
906	Idiff HS2 Trip A	SW	Phase A high set 2 differential trip	P642 / P643 / P645
907	Idiff HS2 Trip B	SW	Phase B high set 2 differential trip	P642 / P643 / P645

DDB no.	English text	Source	Description	Relay model
908	Idiff HS2 Trip C	SW	Phase C high set 2 differential trip	P642 / P643 / P645
909	Id Bias Trip A	SW	Phase A low biased differential trip	P642 / P643 / P645
910	Id Bias trip B	SW	Phase B low biased differential trip	P642 / P643 / P645
911	Id Bias trip C	SW	Phase C low biased differential trip	P642 / P643 / P645
912	No Gap A	SW	No Gap A is an output from the no gap detection algorithm used to detect slight CT saturation on phase A differential current.	P642 / P643 / P645
913	No Gap B	SW	No Gap B is an output from the no gap detection algorithm used to detect slight CT saturation on phase B differential current.	P642 / P643 / P645
914	No Gap C	SW	No Gap A is an output from the no gap detection algorithm used to detect slight CT saturation on phase C differential current.	P642 / P643 / P645
915-949	Not used			
950	REF Trip HV	SW	HV highZ or lowZ restricted earth fault trip	P642 / P643 / P645
951	REF Trip LV	SW	LV highZ or lowZ restricted earth fault trip	P642 / P643 / P645
952	REF Trip TV	SW	TV highZ or lowZ restricted earth fault trip	P643 / P645
953	REF Trip Auto	SW	Autotransformer highZ or lowZ restricted earth fault trip	P642 / P643 / P645
954	Hot Spot >1 Trip	SW	Hottest spot temperature stage 1 trip	P642 / P643 / P645
955	Hot Spot >2 Trip	SW	Hottest spot temperature stage 2 trip	P642 / P643 / P645
956	Hot Spot >3 Trip	SW	Hottest spot temperature stage 3 trip	P642 / P643 / P645
957	Top Oil >1 Trip	SW	Top oil temperature stage 1 trip	P642 / P643 / P645
958	Top Oil >2 Trip	SW	Top oil temperature stage 2 trip	P642 / P643 / P645
959	Top Oil >3 Trip	SW	Top oil temperature stage 3 trip	P642 / P643 / P645
960	POC 1 I>1 Trip	SW	Element 1 phase overcurrent stage 1 trip	P642 / P643 / P645
961	POC 1 I>1 Trip A	SW	Element 1 phase A overcurrent stage 1 trip	P642 / P643 / P645
962	POC 1 I>1 Trip B	SW	Element 1 phase B overcurrent stage 1 trip	P642 / P643 / P645
963	POC 1 I>1 Trip C	SW	Element 1 phase C overcurrent stage 1 trip	P642 / P643 / P645
972	POC 1 I>4 Trip	SW	Element 1 phase overcurrent stage 4 trip	P642 / P643 / P645
973	POC 1 I>4 Trip A	SW	Element 1 phase A overcurrent stage 4 trip	P642 / P643 / P645
974	POC 1 I>4 Trip B	SW	Element 1 phase B overcurrent stage 4 trip	P642 / P643 / P645
975	POC 1 I>4 Trip C	SW	Element 1 phase C overcurrent stage 4 trip	P642 / P643 / P645
976	POC 2 I>1 Trip	SW	Element 2 phase overcurrent stage 1 trip	P642 / P643 / P645
977	POC 2 I>1 Trip A	SW	Element 2 phase A overcurrent stage 1 trip	P642 / P643 / P645
978	POC 2 I>1 Trip B	SW	Element 2 phase B overcurrent stage 1 trip	P642 / P643 / P645
979	POC 2 I>1 Trip C	SW	Element 2 phase C overcurrent stage 1 trip	P642 / P643 / P645
988	POC 2 I>4 Trip	SW	Element 2 phase overcurrent stage 4 trip	P642 / P643 / P645
989	POC 2 I>4 Trip A	SW	Element 2 phase A overcurrent stage 4 trip	P642 / P643 / P645
990	POC 2 I>4 Trip B	SW	Element 2 phase B overcurrent stage 4 trip	P642 / P643 / P645
991	POC 2 I>4 Trip C	SW	Element 2 phase C overcurrent stage 4 trip	P642 / P643 / P645
992	POC 3 I>1 Trip	SW	Element 3 phase overcurrent stage 1 trip	P643 / P645
993	POC 3 I>1 Trip A	SW	Element 3 phase A overcurrent stage 1 trip	P643 / P645
994	POC 3 I>1 Trip B	SW	Element 3 phase B overcurrent stage 1 trip	P643 / P645
995	POC 3 I>1 Trip C	SW	Element 3 phase C overcurrent stage 1 trip	P643 / P645
1004	POC 3 I>4 Trip	SW	Element 3 phase overcurrent stage 4 trip	P643 / P645
1005	POC 3 I>4 Trip A	SW	Element 3 phase A overcurrent stage 4 trip	P643 / P645
1006	POC 3 I>4 Trip B	SW	Element 3 phase B overcurrent stage 4 trip	P643 / P645
1007	POC 3 I>4 Trip C	SW	Element 3 phase C overcurrent stage 4 trip	P643 / P645

DDB no.	English text	Source	Description	Relay model
1008	VCO>1 Trip	SW	Voltage controlled overcurrent stage 1 trip	P642 / P643 / P645
1009	VCO>1 Trip A	SW	Phase A voltage controlled overcurrent stage 1 trip	P642 / P643 / P645
1010	VCO>1 Trip B	SW	Phase B voltage controlled overcurrent stage 1 trip	P642 / P643 / P645
1011	VCO>1 Trip C	SW	Phase C voltage controlled overcurrent stage 1 trip	P642 / P643 / P645
1012	VCO>2 Trip	SW	Voltage controlled overcurrent stage 2 trip	P642 / P643 / P645
1013	VCO>2 Trip A	SW	Phase A voltage controlled overcurrent stage 2 trip	P642 / P643 / P645
1014	VCO>2 Trip B	SW	Phase B voltage controlled overcurrent stage 2 trip	P642 / P643 / P645
1015	VCO>2 Trip C	SW	Phase C voltage controlled overcurrent stage 2 trip	P642 / P643 / P645
1016-1043	Not used			
1044	EF 1 IN>1 Trip	SW	Element 1 earth fault stage 1 trip	P642 / P643 / P645
1047	EF 1 IN>4 Trip	SW	Element 1 earth fault stage 4 trip	P642 / P643 / P645
1048	EF 2 IN>1 Trip	SW	Element 2 earth fault stage 1 trip	P642 / P643 / P645
1051	EF 2 IN>4 Trip	SW	Element 2 earth fault stage 4 trip	P642 / P643 / P645
1052	EF 3 IN>1 Trip	SW	Element 3 earth fault stage 1 trip	P643 / P645
1055	EF 3 IN>4 Trip	SW	Element 3 earth fault stage 4 trip	P643 / P645
1056	Quality VIP 1	SW	IEC61850-8-1. GOOSE Virtual input 1 Quality bit	P642 / P643 / P645
1119	Quality VIP 64	SW	IEC61850-8-1. GOOSE Virtual input 64 Quality bit	P642 / P643 / P645
1120	PubPresPublisher VIP 1	SW	IEC61850-8-1. GOOSE Virtual input 1 Publisher bit	P642 / P643 / P645
1183	PubPresPublisher VIP 64	SW	IEC61850-8-1. GOOSE Virtual input 1 Publisher bit	P642 / P643 / P645
1184-1187	Not used			
1188	RTD 1 Trip	SW	RTD 1 Trip	P642 / P643 / P645
1197	RTD 10 Trip	SW	RTD 10 Trip	P642 / P643 / P645
1198	Any RTD Trip	FL	Any RTD Trip	P642 / P643 / P645
1199	CL Input 1 Trip	SW	Current Loop Input 1 Trip	P642 / P643 / P645
1200	CL Input 2 Trip	SW	Current Loop Input 2 Trip	P642 / P643 / P645
1201	CL Input 3 Trip	SW	Current Loop Input 3 Trip	P642 / P643 / P645
1202	CL Input 4 Trip	SW	Current Loop Input 4 Trip	P642 / P643 / P645
1203	V<1 Trip A/AB	SW	Phase undervoltage stage 1 Trip A/AB	P643 / P645 / Requires three phase VT input.
1204	V<1 Trip B/BC	SW	Phase undervoltage stage 1 Trip B/BC	P643 / P645 / Requires three phase VT input.
1205	V<1 Trip C/CA	SW	Phase undervoltage stage 1 Trip C/CA	P643 / P645 / Requires three phase VT input.
1206	V<2 Trip A/AB	SW	Phase undervoltage stage 2 Trip A/AB	P643 / P645 / Requires three phase VT input.
1207	V<2 Trip B/BC	SW	Phase undervoltage stage 2 Trip B/BC	P643 / P645 / Requires three phase VT input.
1208	V<2 Trip C/CA	SW	Phase undervoltage stage 2 Trip C/CA	P643 / P645 / Requires three phase VT input.
1209	V>1 Trip A/AB	SW	Phase overvoltage stage 1 Trip A/AB	P643 / P645 / Requires three phase VT input.
1210	V>1 Trip B/BC	SW	Phase overvoltage stage 1 Trip B/BC	P643 / P645 / Requires three phase VT input.
1211	V>1 Trip C/CA	SW	Phase overvoltage stage 1 Trip C/CA	P643 / P645 / Requires three phase VT input.
1212	V>2 Trip A/AB	SW	Phase overvoltage stage 2 Trip A/AB	P643 / P645 / Requires three phase VT input.

DDB no.	English text	Source	Description	Relay model
1213	V>2 Trip B/BC	SW	Phase overvoltage stage 2 Trip B/BC	P643 / P645 / Requires three phase VT input.
1214	V>2 Trip C/CA	SW	Phase overvoltage stage 2 Trip C/CA	P643 / P645 / Requires three phase VT input.
1215	V2> Trip	SW	Negative phase sequence overvoltage trip	P642 / P643 / P645 / Requires two single phase VT inputs in P642. / Requires three phase VT input in P643 and P645.
1216	NPOC1 I2>1 Trip	SW	Element 1 negative phase sequence overcurrent stage 1 trip	P642 / P643 / P645
1219	NPOC1 I2>4 Trip	SW	Element 1 negative phase sequence overcurrent stage 4 trip	P642 / P643 / P645
1220	NPOC2 I2>1 Trip	SW	Element 2 negative phase sequence overcurrent stage 1 trip	P642 / P643 / P645
1223	NPOC2 I2>4 Trip	SW	Element 2 negative phase sequence overcurrent stage 4 trip	P642 / P643 / P645
1224	NPOC3 I2>1 Trip	SW	Element 3 negative phase sequence overcurrent stage 1 trip	P643 / P645
1227	NPOC3 I2>4 Trip	SW	Element 3 negative phase sequence overcurrent stage 4 trip	P643 / P645
1228	F>1 Trip	SW	Overfrequency Stage 1 Trip	P642 / P643 / P645
1229	F>2 Trip	SW	Overfrequency Stage 2 Trip	P642 / P643 / P645
1230	F<1 Trip	SW	Underfrequency Stage 1 Trip	P642 / P643 / P645
1233	F<4 Trip	SW	Underfrequency Stage 4 Trip	P642 / P643 / P645
1234	V<1 Trip	SW	Undervoltage stage 1 trip	P643 / P645 / Requires three phase VT input.
1235	V<2 Trip	SW	Undervoltage stage 2 trip	P643 / P645 / Requires three phase VT input.
1236	V>1 Trip	SW	Overvoltage stage 1 trip	P643 / P645 / Requires three phase VT input.
1237	V>2 Trip	SW	Overvoltage stage 2 trip	P643 / P645 / Requires three phase VT input.
1238	VN>1 Trip	SW	Residual overvoltage stage 1 trip	P643 / P645 / Requires three phase VT input.
1239	VN>2 Trip	SW	Residual overvoltage stage 2 trip	P643 / P645 / Requires three phase VT input.
1240	W1 V/Hz>1 Trip	SW	Overflux element 1 stage 1 trip	P643 / P645 / Requires three phase VT input.
1243	W1 V/Hz>4 Trip	SW	Overflux element 1 stage 4 trip	P643 / P645 / Requires three phase VT input.
1244	W2 V/Hz>1 Trip	SW	Overflux element 2 stage 1 trip	P642 / P643 / P645 / Requires two single phase VT inputs in P642. / Requires three phase VT input in P643 and P645.
1247	W2 V/Hz>4 Trip	SW	Overflux element 2 stage 4 trip	P642 / P643 / P645 / Requires two single phase VT inputs in P642. / Requires three phase VT input in P643 and P645.
1248-1256	Not used			
1257	Extern CB1 Trip	PSL	Input to the circuit breaker logic. It is asserted when an external protection trips CB1.	P642 / P643 / P645
1261	Extern CB5 Trip	PSL	Input to the circuit breaker logic. It is asserted when an external protection trips CB5.	P645 /
1262-1311	Not used			

DDB no.	English text	Source	Description	Relay model
1312	Any Start	FL	Any protection element starts.	P642 / P643 / P645
1313	Id Bias Start A	SW	Phase A low biased differential element starts.	P642 / P643 / P645
1314	Id Bias Start B	SW	Phase B low biased differential element starts.	P642 / P643 / P645
1315	Id Bias Start C	SW	Phase C low biased differential element starts.	P642 / P643 / P645 /
1316-1333	Not used			
1334	Hot Spot>1 Start	SW	Hottest spot temperature stage 1 start	P642 / P643 / P645
1335	Hot Spot>2 Start	SW	Hottest spot temperature stage 2 start	P642 / P643 / P645
1336	Hot Spot>3 Start	SW	Hottest spot temperature stage 2 start	P642 / P643 / P645
1337	Top Oil >1 start	SW	Top oil temperature stage 1 start	P642 / P643 / P645
1338	Top Oil >2 start	SW	Top oil temperature stage 2 start	P642 / P643 / P645
1339	Top Oil >3 start	SW	Top oil temperature stage 3 start	P642 / P643 / P645
1340	POC1 I>1 Start	SW	Element 1 phase overcurrent stage 1 start	P642 / P643 / P645
1341	POC1 I>1 Start A	SW	Element 1 phase A overcurrent stage 1 start	P642 / P643 / P645
1342	POC1 I>1 Start B	SW	Element 1 phase B overcurrent stage 1 start	P642 / P643 / P645
1343	POC1 I>1 Start C	SW	Element 1 phase C overcurrent stage 1 start	P642 / P643 / P645
1352	POC1 I>4 Start	SW	Element 1 phase overcurrent stage 4 start	P642 / P643 / P645
1353	POC1 I>4 Start A	SW	Element 1 phase A overcurrent stage 4 start	P642 / P643 / P645
1354	POC1 I>4 Start B	SW	Element 1 phase B overcurrent stage 4 start	P642 / P643 / P645
1355	POC1 I>4 Start C	SW	Element 1 phase C overcurrent stage 4 start	P642 / P643 / P645
1356	POC2 I>1 Start	SW	Element 2 phase overcurrent stage 1 start	P642 / P643 / P645
1357	POC2 I>1 Start A	SW	Element 2 phase A overcurrent stage 1 start	P642 / P643 / P645
1358	POC2 I>1 Start B	SW	Element 2 phase B overcurrent stage 1 start	P642 / P643 / P645
1359	POC2 I>1 Start C	SW	Element 2 phase C overcurrent stage 1 start	P642 / P643 / P645
1368	POC2 I>4 Start	SW	Element 2 phase overcurrent stage 4 start	P642 / P643 / P645
1369	POC2 I>4 Start A	SW	Element 2 phase A overcurrent stage 4 start	P642 / P643 / P645 /
1370	POC2 I>4 Start B	SW	Element 2 phase B overcurrent stage 4 start	P642 / P643 / P645
1371	POC2 I>4 Start C	SW	Element 2 phase C overcurrent stage 4 start	P642 / P643 / P645
1372	POC3 I>1 Start	SW	Element 3 phase overcurrent stage 1 start	P643 / P645
1373	POC3 I>1 Start A	SW	Element 3 phase A overcurrent stage 1 start	P643 / P645
1374	POC3 I>1 Start B	SW	Element 3 phase B overcurrent stage 1 start	P643 / P645
1375	POC3 I>1 Start C	SW	Element 3 phase C overcurrent stage 1 start	P643 / P645
1384	POC3 I>4 Start	SW	Element 3 phase overcurrent stage 4 start	P643 / P645
1385	POC3 I>4 Start A	SW	Element 3 phase A overcurrent stage 4 start	P643 / P645
1386	POC3 I>4 Start B	SW	Element 3 phase B overcurrent stage 4 start	P643 / P645
1387	POC3 I>4 Start C	SW	Element 3 phase C overcurrent stage 4 start	P643 / P645
1388	VCO>1 Start	SW	Voltage controlled overcurrent stage 1 start	P642 / P643 / P645 / Requires two single phase VT inputs in P642. / Requires three phase VT input in P643 and P645.
1389	VCO>1 Start A	SW	Phase A Voltage controlled overcurrent stage 1 start	P642 / P643 / P645 / Requires two single phase VT inputs in P642. / Requires three phase VT input in P643 and P645.

DDB no.	English text	Source	Description	Relay model
1390	VCO>1 Start B	SW	Phase B Voltage controlled overcurrent stage 1 start	P642 / P643 / P645 / Requires two single phase VT inputs in P642. / Requires three phase VT input in P643 and P645.
1391	VCO>1 Start C	SW	Phase C Voltage controlled overcurrent stage 1 start	P642 / P643 / P645 / Requires two single phase VT inputs in P642. / Requires three phase VT input in P643 and P645.
1392	VCO>2 Start	SW	Voltage controlled overcurrent stage 2 start	P642 / P643 / P645 / Requires two single phase VT inputs in P642. / Requires three phase VT input in P643 and P645.
1393	VCO>2 Start A	SW	Phase A Voltage controlled overcurrent stage 2 start	P642 / P643 / P645 / Requires two single phase VT inputs in P642. / Requires three phase VT input in P643 and P645.
1394	VCO>2 Start B	SW	Phase B Voltage controlled overcurrent stage 2 start	P642 / P643 / P645 / Requires two single phase VT inputs in P642. / Requires three phase VT input in P643 and P645.
1395	VCO>2 Start C	SW	Phase C Voltage controlled overcurrent stage 2 start	P642 / P643 / P645 / Requires two single phase VT inputs in P642. / Requires three phase VT input in P643 and P645.
1396-1483	Not used			
1484	EF 1 IN>1 Start	SW	Element 1 earth fault stage 1 start	P642 / P643 / P645
1487	EF 1 IN>4 Start	SW	Element 1 earth fault stage 4 start	P642 / P643 / P645
1488	EF 2 IN>1 Start	SW	Element 2 earth fault stage 1 start	P642 / P643 / P645
1491	EF 2 IN>4 Start	SW	Element 2 earth fault stage 4 start	P642 / P643 / P645
1492	EF 3 IN>1 Start	SW	Element 3 earth fault stage 1 start	P643 / P645
1495	EF 3 IN>4 Start	SW	Element 3 earth fault stage 4 start	P643 / P645
1496-1507	Not used			
1508	Any Diff Start	FL	Asserted if either the 87 (differential protection) or the 64 (restricted earth fault) starts. This signal is linked by software to the through fault monitoring logic.	P642 / P643 / P645
1509-1510	Not used			
1511	REF HV Start	SW	HV winding high or low impedance REF start	P642 / P643 / P645
1512	REF LV Start	SW	LV winding high or low impedance REF start	P642 / P643 / P645
1513	REF TV Start	SW	TV winding high or low impedance REF start	P643 / P645
1514	REF Auto Star	SW	Autotransformer high or low impedance REF start	P642 / P643 / P645
1515-1527	Not used			
1528	CB1 ReTrip 3ph	SW	Circuit breaker 1 re-trip 3ph	P642 / P643 / P645
1529	CB1 BkTrip 3ph	SW	Circuit breaker 1 back-trip 3ph	P642 / P643 / P645
1536	CB5 ReTrip 3ph	SW	Circuit breaker 5 re-trip 3ph	P645
1537	CB5 BkTrip 3ph	SW	Circuit breaker 5 back-trip 3ph	P645
1538-1567	Not used			

DDB no.	English text	Source	Description	Relay model
1568	NPOC1 I2>1 Start	SW	Element 1 negative phase sequence overcurrent stage 1 start	P642 / P643 / P645
1571	NPOC1 I2>4 Start	SW	Element 1 negative phase sequence overcurrent stage 4 start	P642 / P643 / P645
1572	NPOC2 I2>1 Start	SW	Element 2 negative phase sequence overcurrent stage 1 start	P642 / P643 / P645
1575	NPOC2 I2>4 Start	SW	Element 2 negative phase sequence overcurrent stage 4 start	P642 / P643 / P645
1576	NPOC3 I2>1 Start	SW	Element 3 negative phase sequence overcurrent stage 1 start	P643 / P645
1579	NPOC3 I2>4 Start	SW	Element 3 negative phase sequence overcurrent stage 4 start	P643 / P645
1580	V<1 Start	SW	Phase undervoltage stage 1 start 3ph	P643 / P645
1581	V<1 Start A/AB	SW	Phase undervoltage stage 1 start A/AB	P643 / P645
1582	V<1 Start B/BC	SW	Phase undervoltage stage 1 start B/BC	P643 / P645
1583	V<1 Start C/CA	SW	Phase undervoltage stage 1 start C/CA	P643 / P645
1584	V<2 Start	SW	Phase undervoltage stage 2 start 3ph	P643 / P645
1585	V<2 Start A/AB	SW	Phase undervoltage stage 2 start A/AB	P643 / P645
1586	V<2 Start B/BC	SW	Phase undervoltage stage 2 start B/BC	P643 / P645
1587	V<2 Start C/CA	SW	Phase undervoltage stage 2 start C/CA	P643 / P645
1588	V>1 Start	SW	Phase overvoltage stage 1 start 3ph	P643 / P645
1589	V>1 Start A/AB	SW	Phase overvoltage stage 1 start A/AB	P643 / P645
1590	V>1 Start B/BC	SW	Phase overvoltage stage1 start B/BC	P643 / P645
1591	V>1 Start C/CA	SW	Phase overvoltage stage1 start C/CA	P643 / P645
1592	V>2 Start	SW	Phase overvoltage stage 2 start 3ph	P643 / P645
1593	V>2 Start A/AB	SW	Phase overvoltage stage 2 start A/AB	P643 / P645
1594	V>2 Start B/BC	SW	Phase overvoltage stage 2 start B/BC	P643 / P645
1595	V>2 Start C/CA	SW	Phase overvoltage stage 2 start C/CA	P643 / P645
1596	VN>1 Start	SW	Residual overvoltage stage 1 start	P643 / P645
1597	VN>2 Start	SW	Residual overvoltage stage 2 start	P643 / P645
1598	W1 V/Hz> AlmStrt	SW	Overflux element 1 start	P643 / P645
1599	W1 V/Hz>1 Start	SW	Overflux element 1 stage 1 start	P643 / P645
1602	W1 V/Hz>4 Start	SW	Overflux element 1 stage 4 start	P643 / P645
1603	W2 V/Hz> AlmStrt	SW	Overflux element 2 start	P642 / P643 / P645
1604	W2 V/Hz>1 Start	SW	Overflux element 2 stage 1 start	P642 / P643 / P645
1607	W2 V/Hz>4 Start	SW	Overflux element 2 stage 4 start	P642 / P643 / P645
1608	F<1 Start	SW	Underfrequency Stage 1 Start	P642 / P643 / P645
1611	F<4 Start	SW	Underfrequency Stage 4 Start	P642 / P643 / P645
1612	F>1 Start	SW	Overfrequency Stage 1 Start	P642 / P643 / P645
1613	F>2 Start	SW	Overfrequency Stage 2 Start	P642 / P643 / P645
1614	CLI1 Alarm Start	SW	Current Loop Input 1 Alarm Start	P642 / P643 / P645
1617	CLI4 Alarm Start	SW	Current Loop Input 4 Alarm Start	P642 / P643 / P645
1618	CLI1 Trip Start	SW	Current Loop Input 1 Trip Start	P642 / P643 / P645
1621	CLI4 Trip Start	SW	Current Loop Input 4 Trip Start	P642 / P643 / P645
1622	V2> Start	SW	Negative phase sequence overvoltage start	P642 / P643 / P645
1623-1657	Not used			
1658	CT1A ZCD	SW	Hidden DDB, not available for customer use. CT1 phase A zero crossing detector used by CBF logic.	P642 / P643 / P645
1659	CT1B ZCD	SW	Hidden DDB, not available for customer use. CT1 phase B zero crossing detector used by CBF logic.	P642 / P643 / P645

DDB no.	English text	Source	Description	Relay model
1660	CT1C ZCD	SW	Hidden DDB, not available for customer use. CT1 phase C zero crossing detector used by CBF logic.	P642 / P643 / P645
1661	CT2A ZCD	SW	Hidden DDB, not available for customer use. CT2 phase A zero crossing detector used by CBF logic.	P642 / P643 / P645
1662	CT2B ZCD	SW	Hidden DDB, not available for customer use. CT2 phase B zero crossing detector used by CBF logic.	P642 / P643 / P645
1663	CT2C ZCD	SW	Hidden DDB, not available for customer use. CT2 phase C zero crossing detector used by CBF logic.	P643 / P645
1664	CT3A ZCD	SW	Hidden DDB, not available for customer use. CT3 phase A zero crossing detector used by CBF logic.	P643 / P645
1665	CT3B ZCD	SW	Hidden DDB, not available for customer use. CT3 phase B zero crossing detector used by CBF logic.	P643 / P645
1666	CT3C ZCD	SW	Hidden DDB, not available for customer use. CT3 phase C zero crossing detector used by CBF logic.	P643 / P645
1667	CT4A ZCD	SW	Hidden DDB, not available for customer use. CT4 phase A zero crossing detector used by CBF logic.	P643 / P645
1668	CT4B ZCD	SW	Hidden DDB, not available for customer use. CT4 phase B zero crossing detector used by CBF logic.	P643 / P645
1669	CT4C ZCD	SW	Hidden DDB, not available for customer use. CT4 phase C zero crossing detector used by CBF logic.	P643 / P645
1670	CT5A ZCD	SW	Hidden DDB, not available for customer use. CT5 phase A zero crossing detector used by CBF logic.	P643 / P645
1671	CT5B ZCD	SW	Hidden DDB, not available for customer use. CT5 phase B zero crossing detector used by CBF logic.	P643 / P645
1672	CT5C ZCD	SW	Hidden DDB, not available for customer use. CT5 phase C zero crossing detector used by CBF logic.	P643 / P645
1673	CT1 In ZCD	SW	Hidden DDB, not available for customer use. CT1 neutral current zero crossing detector used by CBF logic.	P642 / P643 / P645
1674	CT2 In ZCD	SW	Hidden DDB, not available for customer use. CT2 neutral current zero crossing detector used by CBF logic.	P642 / P643 / P645
1675	CT3 In ZCD	SW	Hidden DDB, not available for customer use. CT3 neutral current zero crossing detector used by CBF logic.	/ P643 / P645
1676	CT4 In ZCD	SW	Hidden DDB, not available for customer use. CT4 neutral current zero crossing detector used by CBF logic.	/ P643 / P645
1677	CT5 In ZCD	SW	Hidden DDB, not available for customer use. CT5 neutral current zero crossing detector used by CBF logic.	/ P643 / P645
1678	CT1A UndCurrent	SW	CT1 Phase A fast undercurrent used by BK1 CBF logic.	P642 / P643 / P645
1679	CT1B UndCurrent	SW	CT1 Phase B fast undercurrent used by BK1 CBF logic.	P642 / P643 / P645
1680	CT1C UndCurrent	SW	CT1 Phase C fast undercurrent used by BK1 CBF logic.	P642 / P643 / P645
1690	CT5A UndCurrent	SW	CT5 Phase A fast undercurrent used by BK5 CBF logic.	P643 / P645
1691	CT5B UndCurrent	SW	CT5 Phase B fast undercurrent used by BK5 CBF logic.	P643 / P645
1692	CT5C UndCurrent	SW	CT5 Phase C fast undercurrent used by BK5 CBF logic.	P643 / P645
1693	HV UndCurrent	SW	HV fast undercurrent used by HV stub bus	P642 / P643 / P645
1694	LV UndCurrent	SW	LV fast undercurrent used by LV stub bus	P642 / P643 / P645
1695	TV UndCurrent	SW	TV fast undercurrent used by TV stub bus	P643 / P645
1696	CT1 PhA UnderCur	SW	Hidden DDB, not available for customer use. CT1 Phase A undercurrent signal required by the CT exclusion logic.	P642 / P643 / P645
1697	CT1 PhB UnderCur	SW	Hidden DDB, not available for customer use. CT1 Phase B undercurrent signal required by the CT exclusion logic.	P642 / P643 / P645

DDB no.	English text	Source	Description	Relay model
1698	CT1 PhC UnderCur	SW	Hidden DDB, not available for customer use. CT1 Phase C undercurrent signal required by the CT exclusion logic.	P642 / P643 / P645
1699	CT2 PhA UnderCur	SW	Hidden DDB, not available for customer use. CT2 Phase A undercurrent signal required by the CT exclusion logic.	P642 / P643 / P645
1700	CT2 PhB UnderCur	SW	Hidden DDB, not available for customer use. CT2 Phase B undercurrent signal required by the CT exclusion logic.	P642 / P643 / P645
1701	CT2 PhC UnderCur	SW	Hidden DDB, not available for customer use. CT2 Phase C undercurrent signal required by the CT exclusion logic.	P642 / P643 / P645
1702	CT3 PhA UnderCur	SW	Hidden DDB, not available for customer use. CT3 Phase A undercurrent signal required by the CT exclusion logic.	/ P643 / P645
1703	CT3 PhB UnderCur	SW	Hidden DDB, not available for customer use. CT3 Phase B undercurrent signal required by the CT exclusion logic.	/ P643 / P645
1704	CT3 PhC UnderCur	SW	Hidden DDB, not available for customer use. CT3 Phase C undercurrent signal required by the CT exclusion logic.	/ P643 / P645
1705	CT4 PhA UnderCur	SW	Hidden DDB, not available for customer use. CT4 Phase A undercurrent signal required by the CT exclusion logic.	P643 / P645
1706	CT4 PhB UnderCur	SW	Hidden DDB, not available for customer use. CT4 Phase B undercurrent signal required by the CT exclusion logic.	P643 / P645
1707	CT4 PhC UnderCur	SW	Hidden DDB, not available for customer use. CT4 Phase C undercurrent signal required by the CT exclusion logic.	P643 / P645
1708	CT5 PhA UnderCur	SW	Hidden DDB, not available for customer use. CT5 Phase A undercurrent signal required by the CT exclusion logic.	P643 / P645
1709	CT5 PhB UnderCur	SW	Hidden DDB, not available for customer use. CT5 Phase B undercurrent signal required by the CT exclusion logic.	P643 / P645
1710	CT5 PhC UnderCur	SW	Hidden DDB, not available for customer use. CT5 Phase C undercurrent signal required by the CT exclusion logic.	P643 / P645
1711	CT1 In Undercur	SW	CT1 IN fast undercurrent used by BK1 CBF logic.	P642 / P643 / P645
1712	CT2 In Undercur	SW	CT2 IN fast undercurrent used by BK2 CBF logic.	P642 / P643 / P645
1713	CT3 In Undercur	SW	CT3 IN fast undercurrent used by BK3 CBF logic.	P643 / P645
1714	CT4 In Undercur	SW	CT4 IN fast undercurrent used by BK4 CBF logic.	P643 / P645
1715	CT5 In Undercur	SW	CT5 IN fast undercurrent used by BK5 CBF logic.	P643 / P645
1716-1722	Not used			
1723	CTexcl disa prot	SW	This DDB is an output from the CT exclusion logic and the relay is disabled if it is asserted.	P642 / P643 / P645
1724	Not used			
1725	VTS VAB>	SW	Hidden DDB, not available for customer use. Vab over threshold used by the VTS logic in the P642.	P642 / P643 / P645
1726	VTS VBC>	SW	Hidden DDB, not available for customer use. Vbc over threshold used by the VTS logic in the P642.	P642 / P643 / P645
1727	VTS VCA>	SW	Hidden DDB, not available for customer use. Vca over threshold used by the VTS logic in the P642.	P642 / P643 / P645
1728	RTD 1 Alarm	SW	RTD 1 Alarm	P642 / P643 / P645
1737	RTD 10 Alarm	SW	RTD 10 Alarm	P642 / P643 / P645
1738	VTS Acc Ind	FL	Hidden DDB, not available for customer use. VTS Accelerate Indication	P642 / P643 / P645
1739	VTS Volt Dep	FL	Hidden DDB, not available for customer use. Any Voltage Dependent function	P642 / P643 / P645
1740	VTS IA>	SW	Hidden DDB, not available for customer use. Ia Over current Threshold	P642 / P643 / P645

DDB no.	English text	Source	Description	Relay model
1741	VTS IB>	SW	Hidden DDB, not available for customer use. Ib Over current Threshold	P642 / P643 / P645
1742	VTS IC>	SW	Hidden DDB, not available for customer use. Ic Over current Threshold	P642 / P643 / P645
1743	VTS VA>	SW	Hidden DDB, not available for customer use. Va Over voltage Threshold. Not available in the P642.	/ P643 / P645
1744	VTS VB>	SW	Hidden DDB, not available for customer use. Vb Overvoltage Threshold. Not available in the P642.	/ P643 / P645
1745	VTS VC>	SW	Hidden DDB, not available for customer use. Vc Overvoltage Threshold. Not available in the P642.	/ P643 / P645
1746	VTS I2>	SW	Hidden DDB, not available for customer use. I2 Overvoltage Threshold.	P642 / P643 / P645
1747	VTS V2>	SW	Hidden DDB, not available for customer use. V2 Overvoltage Threshold.	P642 / P643 / P645
1748	VTS IA delta>	SW	Hidden DDB, not available for customer use. Superimposed Ia Over Threshold.	P642 / P643 / P645
1749	VTS IB delta>	SW	Hidden DDB, not available for customer use. Superimposed Ib Over Threshold.	P642 / P643 / P645
1750	VTS IC delta>	SW	Hidden DDB, not available for customer use. Superimposed Ic Over Threshold.	P642 / P643 / P645
1751	Freq High	SW	High frequency	P642 / P643 / P645
1752	Freq Low	SW	Low frequency	P642 / P643 / P645
1753	Freq Not found	SW	Frequency not found	P642 / P643 / P645
1754-1771	Not used			
1772	All Poles Dead	SW	All Poles Dead	P642 / P643 / P645
1773	Any Pole Dead	SW	Any Pole Dead	P642 / P643 / P645
1774	Pole Dead A	SW	Pole Dead A	P642 / P643 / P645
1775	Pole Dead B	SW	Pole Dead B	P642 / P643 / P645
1776	Pole Dead C	SW	Pole Dead C	P642 / P643 / P645
1777	TF OC Start	SW	Hidden DDB, not available for customer use. Internal signal used in the through fault monitoring function.	P642 / P643 / P645
1778	TF OC End	SW	Hidden DDB, not available for customer use. Internal signal used in the through fault monitoring function.	P642 / P643 / P645
1779	TF Recorder trig	SW	This DDB can be used to trigger the fault recorder.	P642 / P643 / P645
1790	CB1F Non I Tr-1	Fixed logic	Hidden DDB, not available for customer use. Internal signal used in the circuit breaker failure logic.	P642 / P643 / P645
1790	CB1F Non I Trip	Fixed logic	Hidden DDB, not available for customer use. Internal signal used in the circuit breaker failure logic.	P642 / P643 / P645
1792 to 1799	Not used			
1800	VTS Fast Block	SW	VT Supervision Fast Block - blocks elements which would otherwise mal-operate immediately after a fuse failure event occurs	P642 / P643 / P645
1801	VTS Slow Block	SW	VT Supervision Slow Block - blocks elements which would otherwise mal-operate some time after a fuse failure event occurs	P642 / P643 / P645
1802 to 1823	Not used			
1824	Control Input 1	SW	Control Input 1	P642 / P643 / P645
1855	Control Input 32	SW	Control Input 32	P642 / P643 / P645
1856	Virtual Input 01	SW	IEC61850-8-1. Virtual Input 01	P642 / P643 / P645
1919	Virtual Input 64	SW	IEC61850-8-1. Virtual Input 64	P642 / P643 / P645
1920	PSL Int. 1	PSL	PSL Internal connection	P642 / P643 / P645

DDB no.	English text	Source	Description	Relay model
2047	PSL Int. 128	PSL	PSL Internal connection	P642 / P643 / P645

Table 2 - Description of available logic nodes

2.1 Factory Default Programmable Scheme Logic (PSL)

The following section details the default settings of the PSL.

The P642/P643/P645 model options are shown in Table 3:

Model	Opto inputs	Relay outputs
P642xxxxxxxxxxJ	8-12	8-12
P643xxxxxxxxxxK	16-24	16-24
P645xxxxxxxxxxK	16-24	16-24

Table 3 - P642/P643/P645 model options

2.2 Logic Input Mapping

The default mappings for the opto-isolated inputs are shown in Table 4, Table 5 and Table 6.

2.2.1 Logic Input Mapping for P642

Opto-Input No	P642 Relay Text	Function
1	Input L1	(L1 Setting Group) DDB_SG_SELECTOR_X1
2	Input L2	(L2 Setting Group) DDB_SG_SELECTOR_1X
3	Input L3	(L3 Ext CB1 Trip) DDB_EXT_3PH_TRIP1
4	Input L4	(L4 Ext CB2 Trip) DDB_EXT_3PH_TRIP2
5	Input L5	(L5 RESET Rly & LEDS) DDB_RESET_RELAYS_LEDS
6	Input L6	(L6 Unused)
7	Input L7	(L7 CB1 Closed) DDB_CB1_AUX_3PH_CLOSED
8	Input L8	(L8 CB2 Closed) DDB_CB2_AUX_3PH_CLOSED

Table 4 - Logic input mappings for P642

2.2.2 Logic Input Mapping for P643

Opto-Input No	P643 Relay Text	Function
1	Input L1	(L1 Setting Group) DDB_SG_SELECTOR_X1
2	Input L2	(L2 Setting Group) DDB_SG_SELECTOR_1X
3	Input L3	(L3 Ext CB1 Trip) DDB_EXT_3PH_TRIP1

Opto-Input No	P643 Relay Text	Function
4	Input L4	(L4 Ext CB2 Trip) DDB_EXT_3PH_TRIP2
5	Input L5	(L5 RESET Rly & LEDS) DDB_RESET_RELAYS_LEDS
6	Input L6	(L6 Ext CB3 Trip) DDB_EXT_3PH_TRIP3
7	Input L7	(L7 CB1 Closed) DDB_CB1_AUX_3PH_CLOSED
8	Input L8	(L8 CB2 Closed) DDB_CB2_AUX_3PH_CLOSED
9	Input L9	(L9 CB3 Closed) DDB_CB3_AUX_3PH_CLOSED

Table 5 - Logic input mappings for P643

2.2.3 Logic Input Mapping for P645

Opto-Input No	P645 Relay Text	Function
1	Input L1	(L1 Setting Group) DDB_SG_SELECTOR_X1
2	Input L2	(L2 Setting Group) DDB_SG_SELECTOR_1X
3	Input L3	(L3 Ext CB1 Trip) DDB_EXT_3PH_TRIP1
4	Input L4	(L4 Ext CB2 Trip) DDB_EXT_3PH_TRIP2
5	Input L5	(L5 RESET Rly & LEDS) DDB_RESET_RELAYS_LEDS
6	Input L6	(L6 Ext CB3 Trip) DDB_EXT_3PH_TRIP3
7	Input L7	(L7 CB1 Closed) DDB_CB1_AUX_3PH_CLOSED
8	Input L8	(L8 CB1 Closed) DDB_CB2_AUX_3PH_CLOSED
9	Input L9	(L9 CB1 Closed) DDB_CB3_AUX_3PH_CLOSED
10	Input L10	(L10 CB1 Closed) DDB_CB4_AUX_3PH_CLOSED
11	Input L11	(L11 CB1 Closed) DDB_CB5_AUX_3PH_CLOSED
12	Input L12	(L12 Ext CB4 Trip) DDB_EXT_3PH_TRIP4
13	Input L13	(L13 Ext CB5 Trip) DDB_EXT_3PH_TRIP5

Table 6 - Logic input mappings for P645

2.3 Relay Output Contact Mapping

The default mappings for the relay output contacts are shown in Table 7.

Relay Model	Relay Contact No	Relay Text	Relay Conditioner	Function
P642, P643, P645	1	Output R1	Pickup (P642) Dwell Timer 100 ms (P643, P645)	DDB_OUTPUT_CON_1 (R1 HV Backup TRIP)
P642, P643, P645	2	Output R2	Pickup (P642) Dwell Timer 100 ms (P643, P645)	DDB_OUTPUT_CON_2 (R2 LV Backup TRIP)
P642, P643, P645	3	Output R3	Pickup (P642) Dwell Timer 100 ms (P643, P645)	DDB_OUTPUT_CON_3 (R3 ANY TRIP)
P642, P643, P645	4	Output R4	Pickup (P642) Delayed Drop-off timer 500 ms (P643, P645)	DDB_OUTPUT_CON_4 (R4 GENERAL ALARM)
P642, P643, P645	5	Output R5	Pickup (P642) Dwell Timer 100 ms (P643, P645)	DDB_OUTPUT_CON_5 (R5 CB FAIL)
P642, P643, P645	6	Output R6	Pickup (P642) Dwell Timer 100 ms (P643,P645)	DDB_OUTPUT_CON_6 (R6 CB FAIL)
P643, P645	7	Output R7	Pickup (P642) Dwell Timer 100 ms (P643, P645)	DDB_OUTPUT_CON_7 (R7 ANY DIFF TRIP)
P643, P645	8	Output R8	Pickup (P642) Dwell Timer 100 ms (P643, P645)	DDB_OUTPUT_CON_8 (R8 ANY DIFF TRIP)
P643, P645	9	Output R9	Dwell Timer 100 ms (P643, P645 only)	DDB_OUTPUT_CON_9 (R9 ANY TRIP)
P643, P645	10	Output R10	Dwell Timer 100 ms (P645 only)	DDB_OUTPUT_CON_10 (R10 ANY TRIP)
P643, P645	11	Output R11	Delayed Drop-off timer 500 ms (P643, P645 only)	DDB_OUTPUT_CON_11 (R11 V/Hz PRE-TRIP ALM)
P643, P645	12	Output R12	Delayed Drop-off timer 500 ms (P643, P645 only)	DDB_OUTPUT_CON_12 (R12 TOL PRE-TRIP ALM)
P643, P645	13	Output R13	Dwell Timer 100 ms (P643, P645 only)	DDB_OUTPUT_CON_13 (R13 TV BACKUP TRIP)
P643, P645	14	Output R14	Dwell Timer 100 ms (P643, P645 only)	DDB_OUTPUT_CON_14 (R14 CB FAIL)
P645	15	Output R15	Dwell Timer 100 ms (P645 only)	DDB_OUTPUT_CON_15 (R15 CB FAIL)
P645	16	Output R16	Dwell Timer 100 ms (P645 only)	DDB_OUTPUT_CON_16 (R16 CB FAIL)
P645	17 to 32	Not Used		
Note	To generate a fault record, connect one or several contacts to the “Fault Record Trigger” in PSL. The triggering contact should be ‘self reset’ and not latching. If a latching contact is used the fault record is not generated until the contact has fully reset.			

Table 7 - Relay output contact mapping

2.4 Programmable LED Output Mapping

The default mappings for the programmable LEDs are shown in Table 8. The P642 has RED LEDs only, whereas the P643 and P645 also have tri-colour LEDS (red/yellow/green).

Relay Model	LED No	LED Input Connection/Text	Latched	P645 LED Function Indication
P642, P643, P645	1	LED 1 Red	Yes	Diff Trip
P642, P643, P645	2	LED 2 Red	Yes	Ref Trip
P642, P643, P645	3	LED 3 Red	Yes	Top Oil and Spot Thermal Trip
P642, P643, P645	4	LED 4 Red	Yes	V or F Trip
P642, P643, P645	5	LED 5 Red	Yes	HV Backup Trip
P642, P643, P645	6	LED 6 Red	Yes	LV Backup Trip
P643, P645	7	LED 7 Red	Yes	TV Backup Trip
P642, P643, P645	8	LED 8 Red	Yes	CB Fail
P645	9	Fnkey Led1	No	Spare
P645	10	Fnkey Led2	No	Spare
P645	11	Fnkey LED3	No	Spare
P645	12	Fnkey Led4 Red (Fnct Key is Toggled Mode)	No	Spare
P645	13	Fnkey LED5 Red (Fnct Key is Toggled Mode)	No	Setting Group 2 Enabled
P645	14	Fnkey LED6 Yellow	No	Overfluxing Reset
P645	15	Fnkey LED7 Yellow (Fnct Key Is Normal Mode)	No	Thermal Overload Reset
P645	16	Fnkey LED8 Yellow (Fnct Key Is Normal Mode)	No	Loss Of Life Reset
P645	17	Fnkey LED9 Yellow (Fnct Key Is Normal Mode)	No	Relay and LED Reset
P645	18	Fnkey LED10 Yellow (Fnct Key Is Normal Mode)	No	Disturbance Recorder Trigger
P645	19 to 24	Not Used		

Table 8 - Programmable LED output mapping

2.5 Fault Recorder Start Mapping

The default mapping for the signal which initiates a fault record is shown in Table 9.

Initiating signals	Output from OR gate (fault trigger)
DDB_TRIP_INITIATE	DDB_FAULT_RECORDER_START (Initiate fault recording from main protection trip)
DDB_THROUGH_FAULT_ALM	

Table 9 - Fault recorder start mapping

2.6 PSL Data Column

The MiCOM P64x relay contains a PSL DATA column that can be used to track PSL modifications. A total of 12 cells are contained in the PSL DATA column, 3 for each setting group. The function for each cell is in Table 10:

Grp. PSL Ref.	When downloading a PSL to the relay, enter the PSL group and a reference identifier. The first 32 characters of the reference ID are displayed in this cell. Use the ◁ and ▷ keys to scroll through 32 characters because only 16 can be displayed at any one time.
18 Nov 2002 08:59:32.047	This cell displays the date and time when the PSL was down loaded to the relay.
Grp. 1 PSL ID - 2062813232	This is a unique number for the PSL that has been entered. Any change in the PSL causes a different number to be displayed.

Note *The above cells are repeated for each setting group.*

Table 10 - Cell functions

3 VIEWING AND PRINTING DEFAULT PSL DIAGRAMS

It is possible to view and print the default PSL diagrams for the device. Typically, these diagrams allow you to see these mappings:

- Opto Input Mappings
- Output Relay Mappings
- LED Mappings
- Start Indications
- Phase Trip Mappings
- System Check Mapping

To download and print the default PSL diagrams for the device:

1. Close MiCOM S1 Studio.
2. Select **Programs** > then navigate through to > **MiCOM S1 Studio** > **Data Model Manager**.
3. Click **Add** then **Next**.
4. Click **Internet** then **Next**.
5. Select your language then click **Next**.
6. From the tree view, select the model and software version.
7. Click **Install**. When complete click **OK**.
8. Close the Data Model Manager and start MiCOM S1 Studio.
9. Select Tools > PSL Editor (Px40).
10. In the PSL Editor select **File** > **Open**. The downloaded psl files are in C:\Program Files\ directory located in the \MiCOM S1\Courier\PSL\Defaults sub-directory.
11. Highlight the required psl diagram and select **File** > **Print**.

4 MICOM P642 PSL DIAGRAMS

4.1 Any Trip Mapping

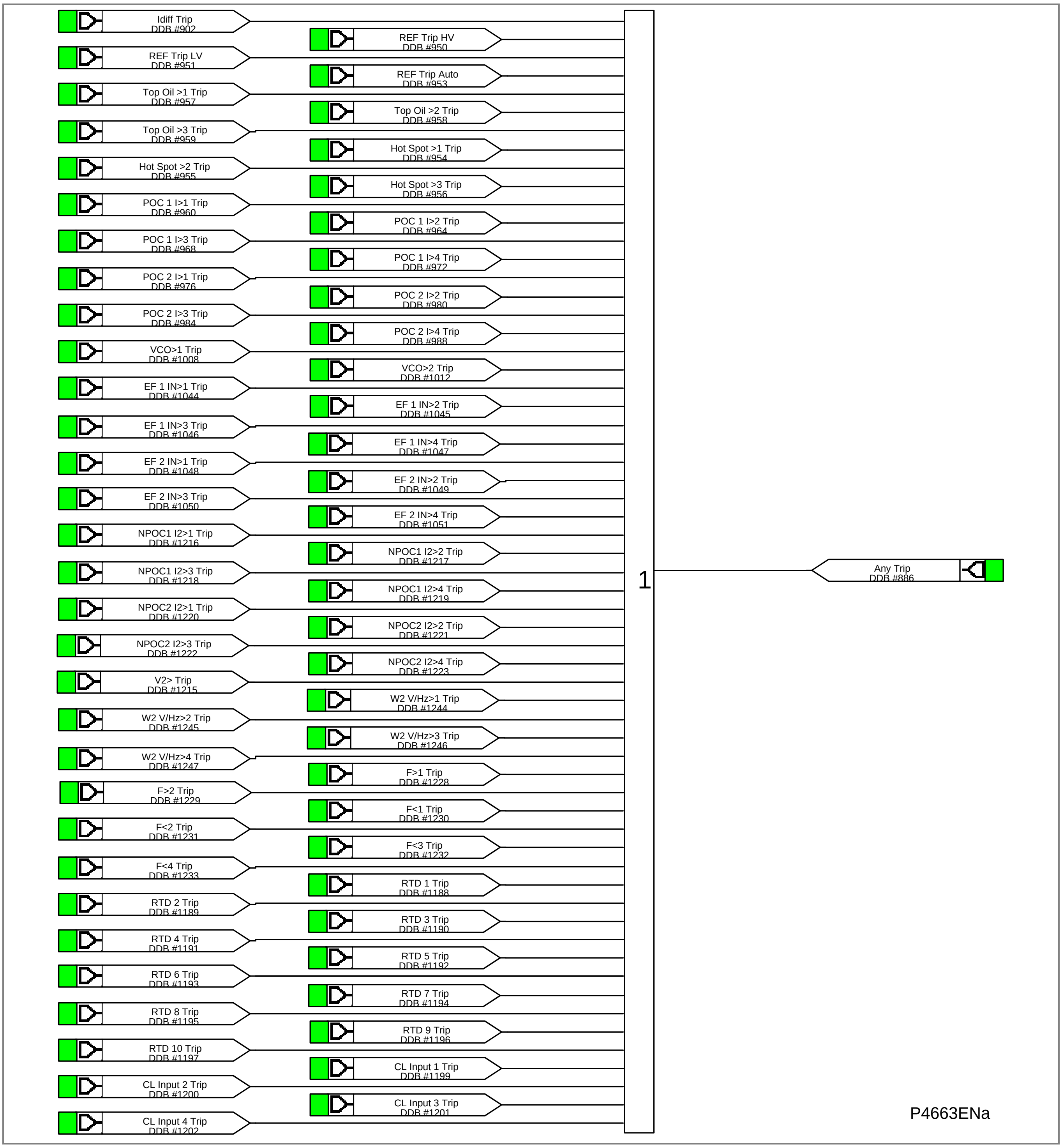

Idiff Trip DDB #902
REF Trip HV DDB #950
REF Trip LV DDB #951
REF Trip Auto DDB #953
Top Oil >1 Trip DDB #957
Top Oil >2 Trip DDB #958
Top Oil >3 Trip DDB #959
Hot Spot >1 Trip DDB #954
Hot Spot >2 Trip DDB #955
Hot Spot >3 Trip DDB #956
POC 1 I>1 Trip DDB #960
POC 1 I>2 Trip DDB #964
POC 1 I>3 Trip DDB #968
POC 1 I>4 Trip DDB #972
POC 2 I>1 Trip DDB #976
POC 2 I>2 Trip DDB #980
POC 2 I>3 Trip DDB #984
POC 2 I>4 Trip DDB #988
VCO>1 Trip DDB #1008
VCO>2 Trip DDB #1012
EF 1 IN>1 Trip DDB #1044
EF 1 IN>2 Trip DDB #1045
EF 1 IN>3 Trip DDB #1046
EF 1 IN>4 Trip DDB #1047
EF 2 IN>1 Trip DDB #1048
EF 2 IN>2 Trip DDB #1049
EF 2 IN>3 Trip DDB #1050
EF 2 IN>4 Trip DDB #1051
NPOC1 I2>1 Trip DDB #1216
NPOC1 I2>2 Trip DDB #1217
NPOC1 I2>3 Trip DDB #1218
NPOC1 I2>4 Trip DDB #1219
NPOC2 I2>1 Trip DDB #1220
NPOC2 I2>2 Trip DDB #1221
NPOC2 I2>3 Trip DDB #1222
NPOC2 I2>4 Trip DDB #1223
V2> Trip DDB #1215
W2 V/Hz>1 Trip DDB #1244
W2 V/Hz>2 Trip DDB #1245
W2 V/Hz>3 Trip DDB #1246
W2 V/Hz>4 Trip DDB #1247
F>1 Trip DDB #1228
F>2 Trip DDB #1229
F<1 Trip DDB #1230
F<2 Trip DDB #1231
F<3 Trip DDB #1232
F<4 Trip DDB #1233
RTD 1 Trip DDB #1188
RTD 2 Trip DDB #1189
RTD 3 Trip DDB #1190
RTD 4 Trip DDB #1191
RTD 5 Trip DDB #1192
RTD 6 Trip DDB #1193
RTD 7 Trip DDB #1194
RTD 8 Trip DDB #1195
RTD 9 Trip DDB #1196
RTD 10 Trip DDB #1197
CL Input 1 Trip DDB #1199
CL Input 2 Trip DDB #1200
CL Input 3 Trip DDB #1201
CL Input 4 Trip DDB #1202
1
Any Trip DDB #886
P4663ENa

Figure 7 - P642 - Any trip mappings

4.2 Back up Trip Logic

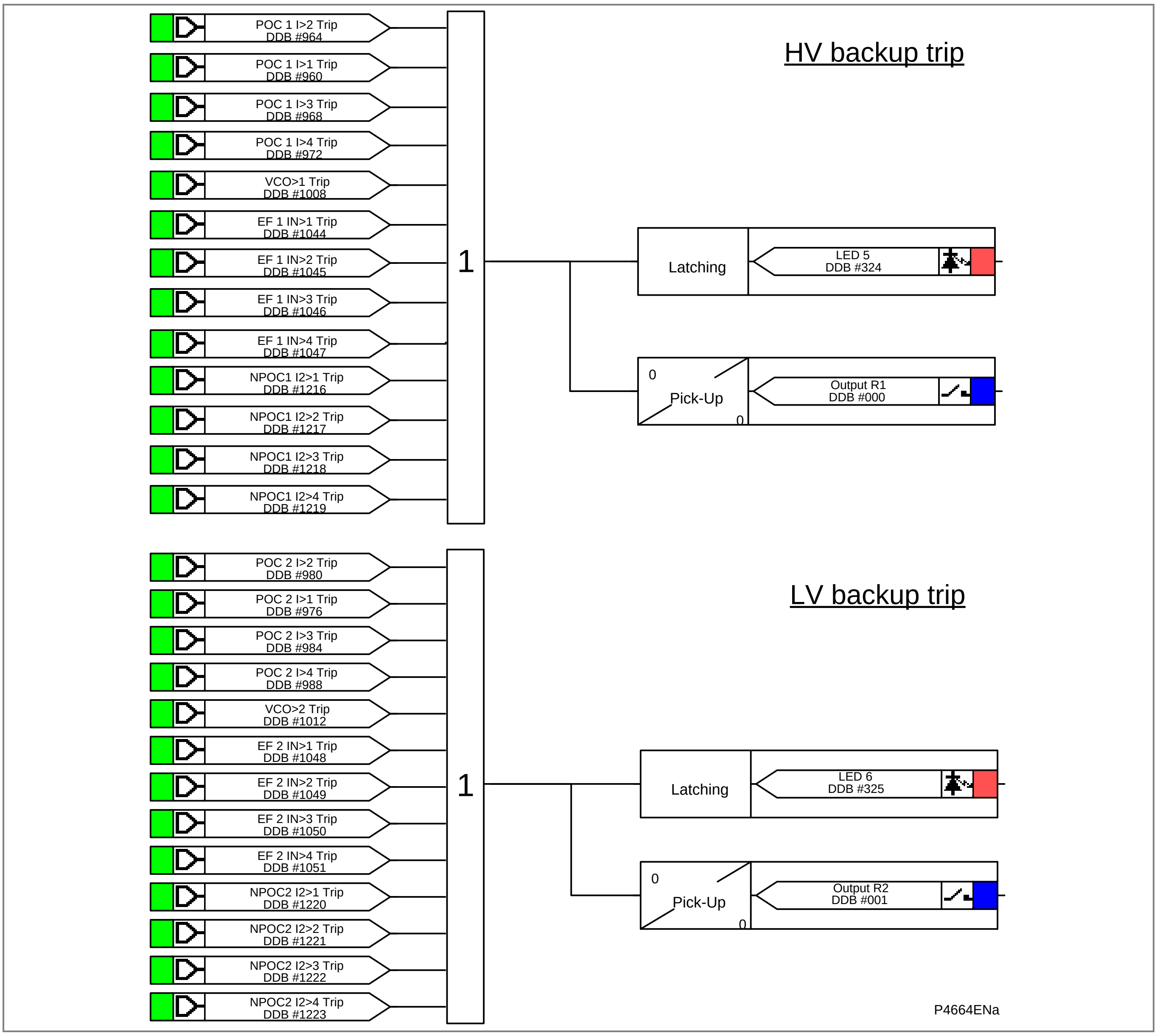

POC 1 I>2 Trip DDB #964
POC 1 I>1 Trip DDB #960
POC 1 I>3 Trip DDB #968
POC 1 I>4 Trip DDB #972
VCO>1 Trip DDB #1008
EF 1 IN>1 Trip DDB #1044
EF 1 IN>2 Trip DDB #1045
EF 1 IN>3 Trip DDB #1046
EF 1 IN>4 Trip DDB #1047
NPOC1 I2>1 Trip DDB #1216
NPOC1 I2>2 Trip DDB #1217
NPOC1 I2>3 Trip DDB #1218
NPOC1 I2>4 Trip DDB #1219
1
HV backup trip
Latching
LED 5 DDB #324
0
Pick-Up
0
Output R1 DDB #000
POC 2 I>2 Trip DDB #980
POC 2 I>1 Trip DDB #976
POC 2 I>3 Trip DDB #984
POC 2 I>4 Trip DDB #988
VCO>2 Trip DDB #1012
EF 2 IN>1 Trip DDB #1048
EF 2 IN>2 Trip DDB #1049
EF 2 IN>3 Trip DDB #1050
EF 2 IN>4 Trip DDB #1051
NPOC2 I2>1 Trip DDB #1220
NPOC2 I2>2 Trip DDB #1221
NPOC2 I2>3 Trip DDB #1222
NPOC2 I2>4 Trip DDB #1223
1
LV backup trip
Latching
LED 6 DDB #325
0
Pick-Up
0
Output R2 DDB #001
P4664ENa

Figure 8 - P642 - Backup trip logic mappings

4.3 General Alarm

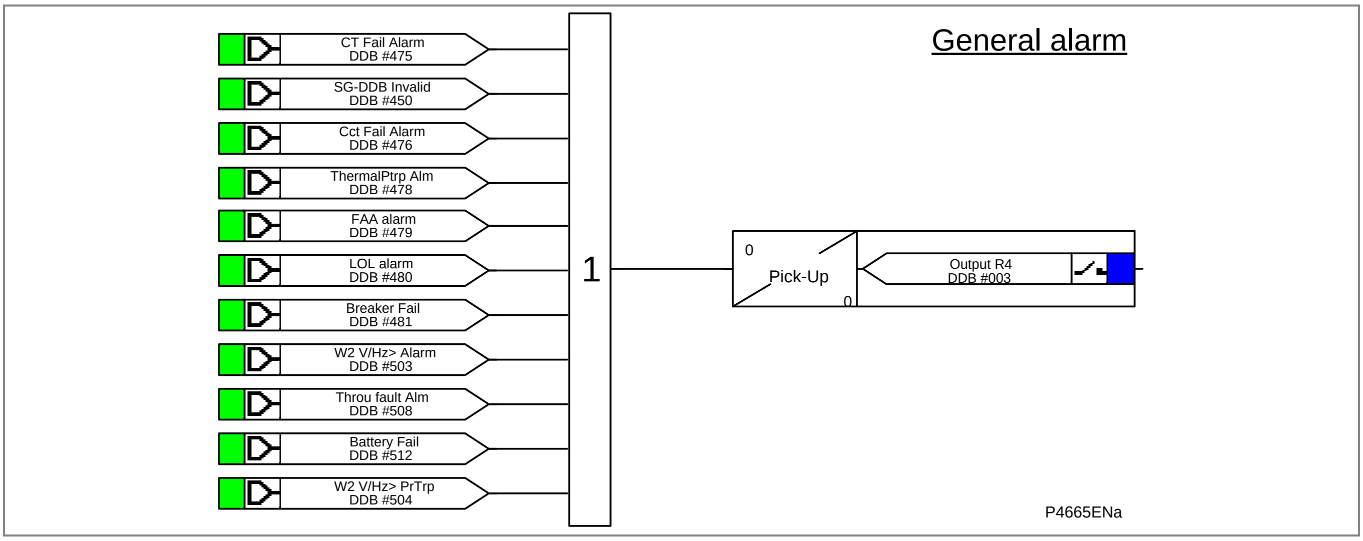

General alarm
CT Fail Alarm
DDB #475
SG-DDB Invalid
DDB #450
Cct Fail Alarm
DDB #476
ThermalPtrp Alm
DDB #478
FAA alarm
DDB #479
LOL alarm
DDB #480
Breaker Fail
DDB #481
W2 V/Hz> Alarm
DDB #503
Throu fault Alm
DDB #508
Battery Fail
DDB #512
W2 V/Hz> PrTrp
DDB #504
1
0
Pick-Up
0
Output R4
DDB #003
P4665ENa

Figure 9 - P642 - General alarm mappings

4.4 Breaker Failure

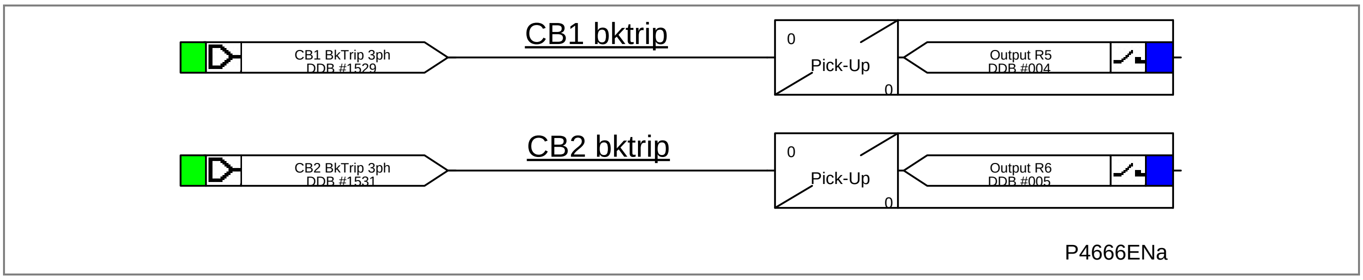

CB1 bktrip
CB1 BkTrip 3ph
DDB #1529
0
Pick-Up
0
Output R5
DDB #004
CB2 bktrip
CB2 BkTrip 3ph
DDB #1531
0
Pick-Up
0
Output R6
DDB #005
P4666ENa

Figure 10 - P642 - Breaker failure mappings

4.5 Any Differential Trip

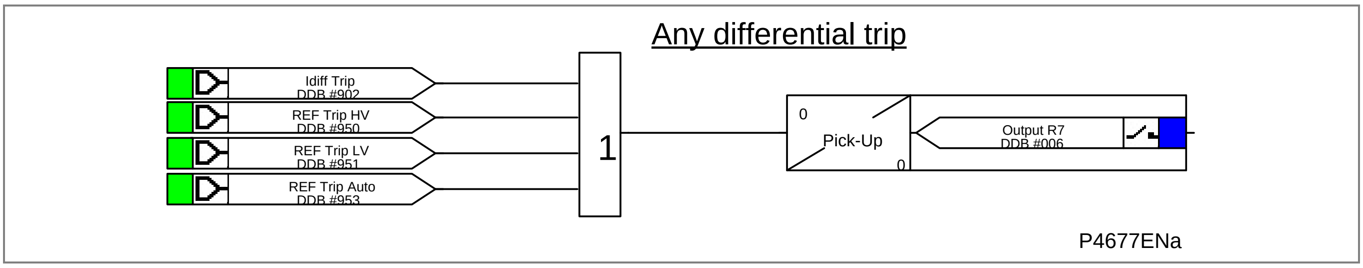

Any differential trip
Idiff Trip
DDB #902
REF Trip HV
DDB #950
REF Trip LV
DDB #951
REF Trip Auto
DDB #953
1
0
Pick-Up
0
Output R7
DDB #006
P4677ENa

Figure 11 - P642 - Any differential trip mappings

4.6 Any Trip

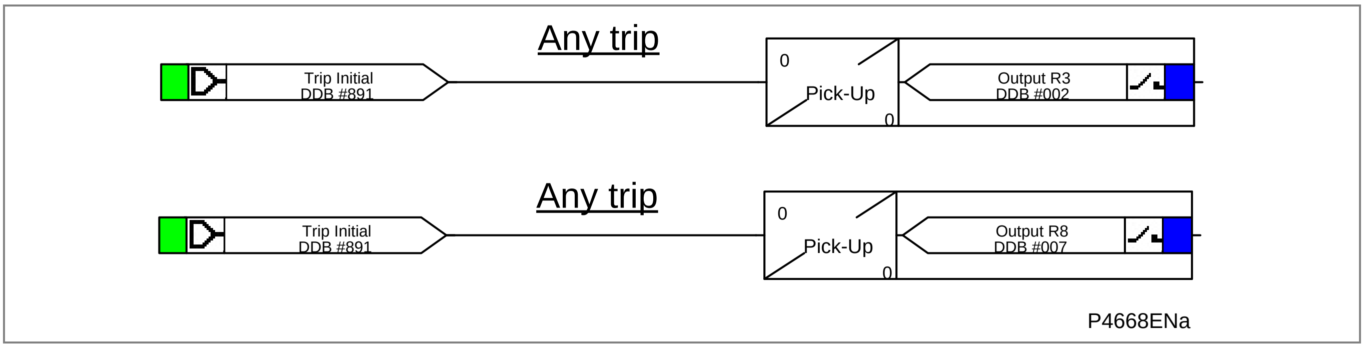

Any trip
Trip Initial
DDB #891
0
Pick-Up
0
Output R3
DDB #002
Any trip
Trip Initial
DDB #891
0
Pick-Up
0
Output R8
DDB #007
P4668ENa

Figure 12 - P642 - Any trip mappings

4.7 Fault Recorder Trigger

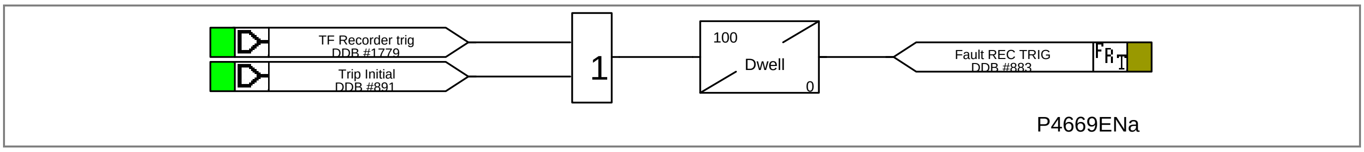

TF Recorder trig
DDB #1779
Trip Initial
DDB #891
1
100
Dwell
0
Fault REC TRIG
DDB #883
P4669ENa

Figure 13 - P642 - Fault recorder trigger mappings

4.8 Opto Isolator Mappings

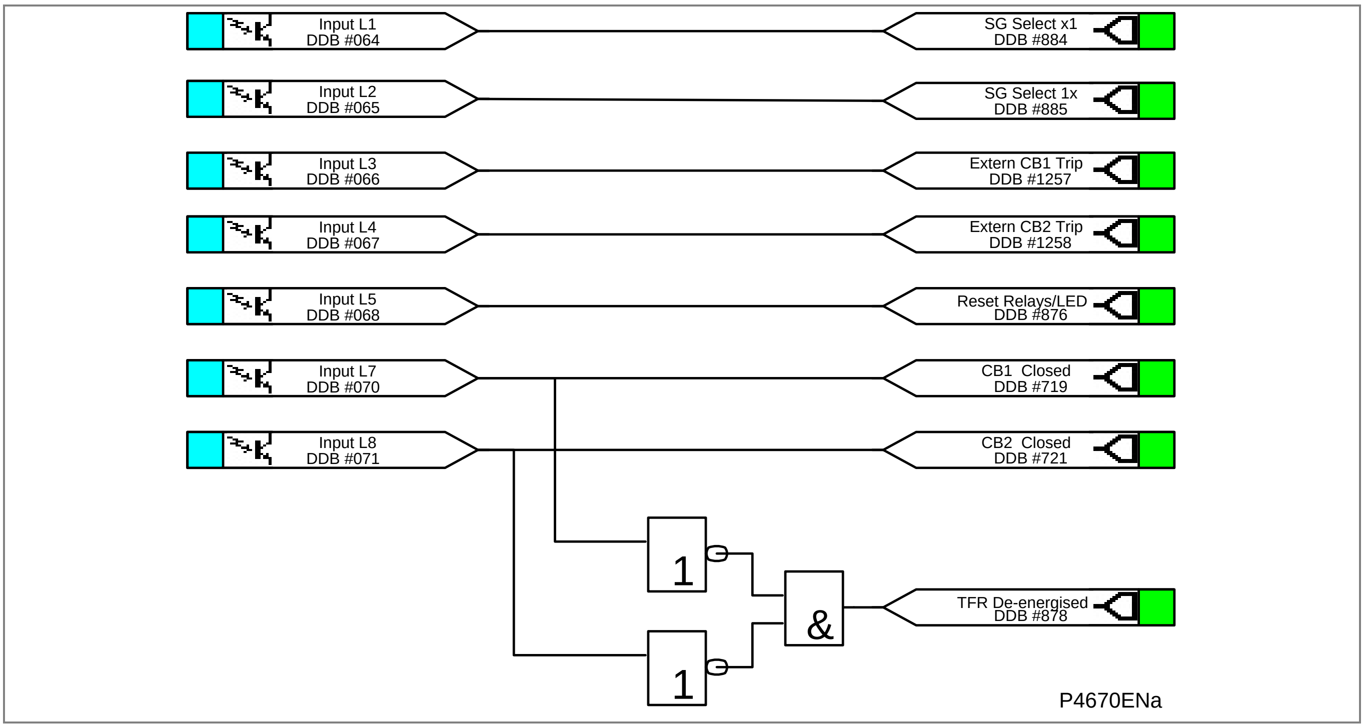

Input L1
DDB #064
SG Select x1
DDB #884
Input L2
DDB #065
SG Select 1x
DDB #885
Input L3
DDB #066
Extern CB1 Trip
DDB #1257
Input L4
DDB #067
Extern CB2 Trip
DDB #1258
Input L5
DDB #068
Reset Relays/LED
DDB #876
Input L7
DDB #070
CB1 Closed
DDB #719
Input L8
DDB #071
CB2 Closed
DDB #721
1
1
&
TFR De-energised
DDB #878
P4670ENa

Figure 14 - P642 - Opto isolator mappings

4.9 LED Mapping

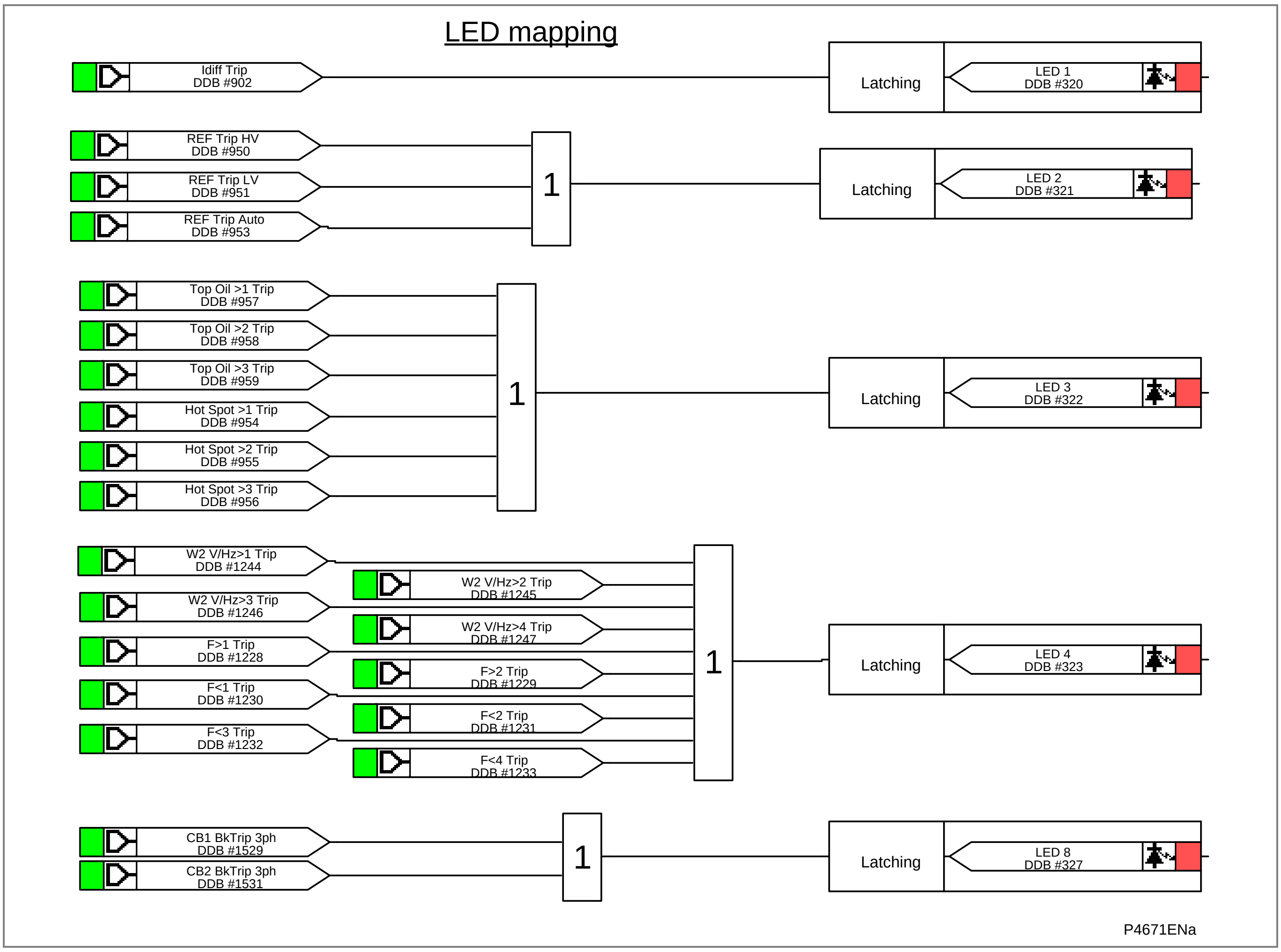

LED mapping
Idiff Trip DDB #902
Latching
LED 1 DDB #320
REF Trip HV DDB #950
REF Trip LV DDB #951
REF Trip Auto DDB #953
1
Latching
LED 2 DDB #321
Top Oil >1 Trip DDB #957
Top Oil >2 Trip DDB #958
Top Oil >3 Trip DDB #959
Hot Spot >1 Trip DDB #954
Hot Spot >2 Trip DDB #955
Hot Spot >3 Trip DDB #956
1
Latching
LED 3 DDB #322
W2 V/Hz>1 Trip DDB #1244
W2 V/Hz>2 Trip DDB #1245
W2 V/Hz>3 Trip DDB #1246
W2 V/Hz>4 Trip DDB #1247
F>1 Trip DDB #1228
F>2 Trip DDB #1229
F<1 Trip DDB #1230
F<2 Trip DDB #1231
F<3 Trip DDB #1232
F<4 Trip DDB #1233
1
Latching
LED 4 DDB #323
CB1 BkTrip 3ph DDB #1529
CB2 BkTrip 3ph DDB #1531
1
Latching
LED 8 DDB #327
P4671ENa

Figure 15 - P642 - LED mappings

5 MICOM P643 PSL DIAGRAMS

5.1 Any Trip Mapping

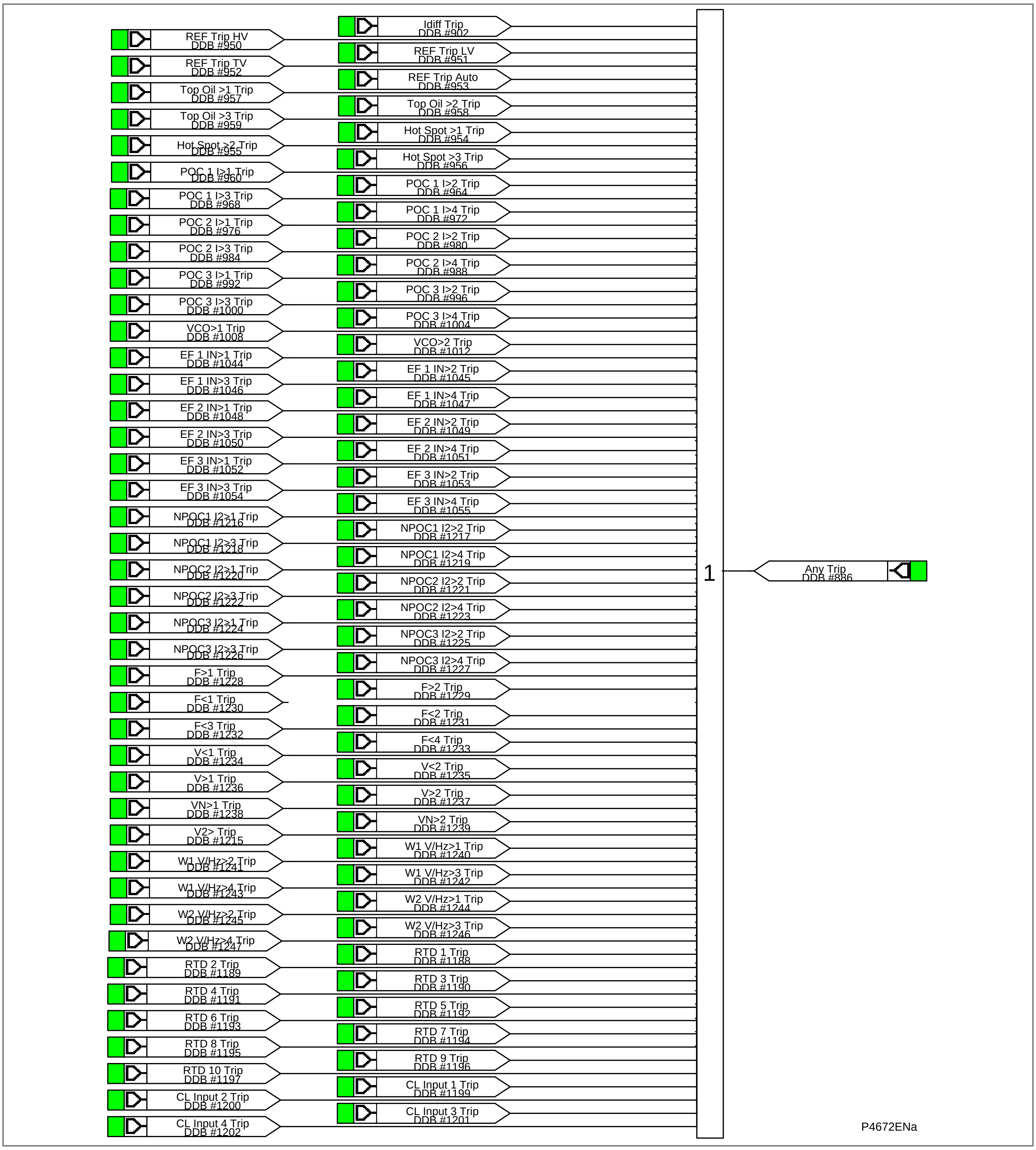

REF Trip HV DDB #950
REF Trip TV DDB #952
Top Oil >1 Trip DDB #957
Top Oil >3 Trip DDB #959
Hot Spot >2 Trip DDB #955
POC 1 I>1 Trip DDB #960
POC 1 I>3 Trip DDB #968
POC 2 I>1 Trip DDB #976
POC 2 I>3 Trip DDB #984
POC 3 I>1 Trip DDB #992
POC 3 I>3 Trip DDB #1000
VCO>1 Trip DDB #1008
EF 1 IN>1 Trip DDB #1044
EF 1 IN>3 Trip DDB #1046
EF 2 IN>1 Trip DDB #1048
EF 2 IN>3 Trip DDB #1050
EF 3 IN>1 Trip DDB #1052
EF 3 IN>3 Trip DDB #1054
NPOC1 I2>1 Trip DDB #1216
NPOC1 I2>3 Trip DDB #1218
NPOC2 I2>1 Trip DDB #1220
NPOC2 I2>3 Trip DDB #1222
NPOC3 I2>1 Trip DDB #1224
NPOC3 I2>3 Trip DDB #1226
F>1 Trip DDB #1228
F<1 Trip DDB #1230
F<3 Trip DDB #1232
V<1 Trip DDB #1234
V>1 Trip DDB #1236
VN>1 Trip DDB #1238
V2> Trip DDB #1215
W1 V/Hz>2 Trip DDB #1241
W1 V/Hz>4 Trip DDB #1243
W2 V/Hz>2 Trip DDB #1245
W2 V/Hz>4 Trip DDB #1247
RTD 2 Trip DDB #1189
RTD 4 Trip DDB #1191
RTD 6 Trip DDB #1193
RTD 8 Trip DDB #1195
RTD 10 Trip DDB #1197
CL Input 2 Trip DDB #1200
CL Input 4 Trip DDB #1202
Idiff Trip DDB #902
REF Trip LV DDB #951
REF Trip Auto DDB #953
Top Oil >2 Trip DDB #958
Hot Spot >1 Trip DDB #954
Hot Spot >3 Trip DDB #956
POC 1 I>2 Trip DDB #964
POC 1 I>4 Trip DDB #972
POC 2 I>2 Trip DDB #980
POC 2 I>4 Trip DDB #988
POC 3 I>2 Trip DDB #996
POC 3 I>4 Trip DDB #1004
VCO>2 Trip DDB #1012
EF 1 IN>2 Trip DDB #1045
EF 1 IN>4 Trip DDB #1047
EF 2 IN>2 Trip DDB #1049
EF 2 IN>4 Trip DDB #1051
EF 3 IN>2 Trip DDB #1053
EF 3 IN>4 Trip DDB #1055
NPOC1 I2>2 Trip DDB #1217
NPOC1 I2>4 Trip DDB #1219
NPOC2 I2>2 Trip DDB #1221
NPOC2 I2>4 Trip DDB #1223
NPOC3 I2>2 Trip DDB #1225
NPOC3 I2>4 Trip DDB #1227
F>2 Trip DDB #1229
F<2 Trip DDB #1231
F<4 Trip DDB #1233
V<2 Trip DDB #1235
V>2 Trip DDB #1237
VN>2 Trip DDB #1239
W1 V/Hz>1 Trip DDB #1240
W1 V/Hz>3 Trip DDB #1242
W2 V/Hz>1 Trip DDB #1244
W2 V/Hz>3 Trip DDB #1246
RTD 1 Trip DDB #1188
RTD 3 Trip DDB #1190
RTD 5 Trip DDB #1192
RTD 7 Trip DDB #1194
RTD 9 Trip DDB #1196
CL Input 1 Trip DDB #1199
CL Input 3 Trip DDB #1201
1
Any Trip DDB #886
P4672ENa

Figure 16 - P643 - Any trip mappings

5.2 Backup Trip Logic

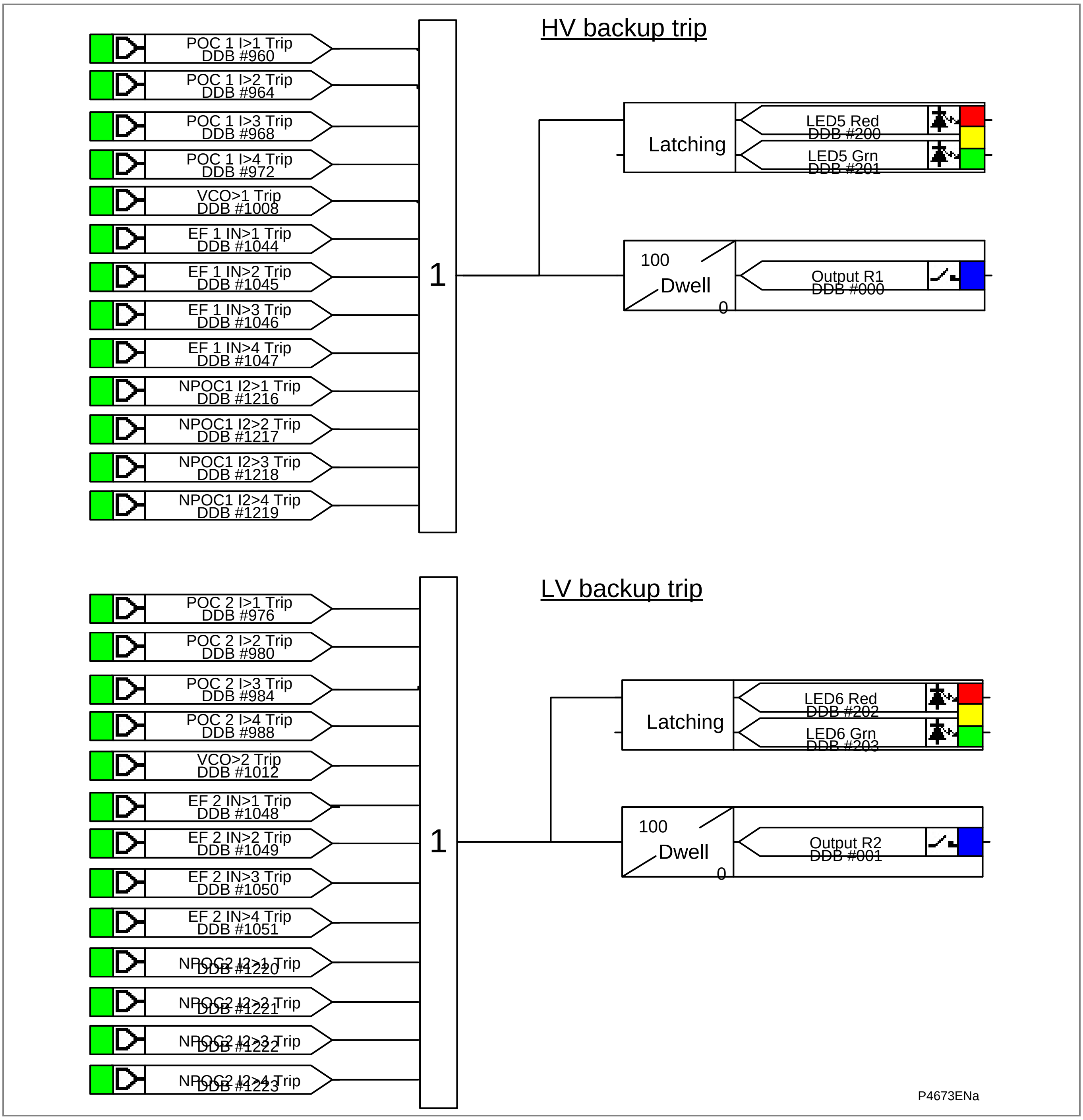

HV backup trip
POC 1 I>1 Trip DDB #960
POC 1 I>2 Trip DDB #964
POC 1 I>3 Trip DDB #968
POC 1 I>4 Trip DDB #972
VCO>1 Trip DDB #1008
EF 1 IN>1 Trip DDB #1044
EF 1 IN>2 Trip DDB #1045
EF 1 IN>3 Trip DDB #1046
EF 1 IN>4 Trip DDB #1047
NPOC1 I2>1 Trip DDB #1216
NPOC1 I2>2 Trip DDB #1217
NPOC1 I2>3 Trip DDB #1218
NPOC1 I2>4 Trip DDB #1219
1
Latching
LED5 Red DDB #200
LED5 Grn DDB #201
100
Dwell
0
Output R1 DDB #000
LV backup trip
POC 2 I>1 Trip DDB #976
POC 2 I>2 Trip DDB #980
POC 2 I>3 Trip DDB #984
POC 2 I>4 Trip DDB #988
VCO>2 Trip DDB #1012
EF 2 IN>1 Trip DDB #1048
EF 2 IN>2 Trip DDB #1049
EF 2 IN>3 Trip DDB #1050
EF 2 IN>4 Trip DDB #1051
NPOC2 I2>1 Trip DDB #1220
NPOC2 I2>2 Trip DDB #1221
NPOC2 I2>3 Trip DDB #1222
NPOC2 I2>4 Trip DDB #1223
1
Latching
LED6 Red DDB #202
LED6 Grn DDB #203
100
Dwell
0
Output R2 DDB #001
P4673ENa

Figure 17 - P643 - HV and LV Backup trip logic mappings

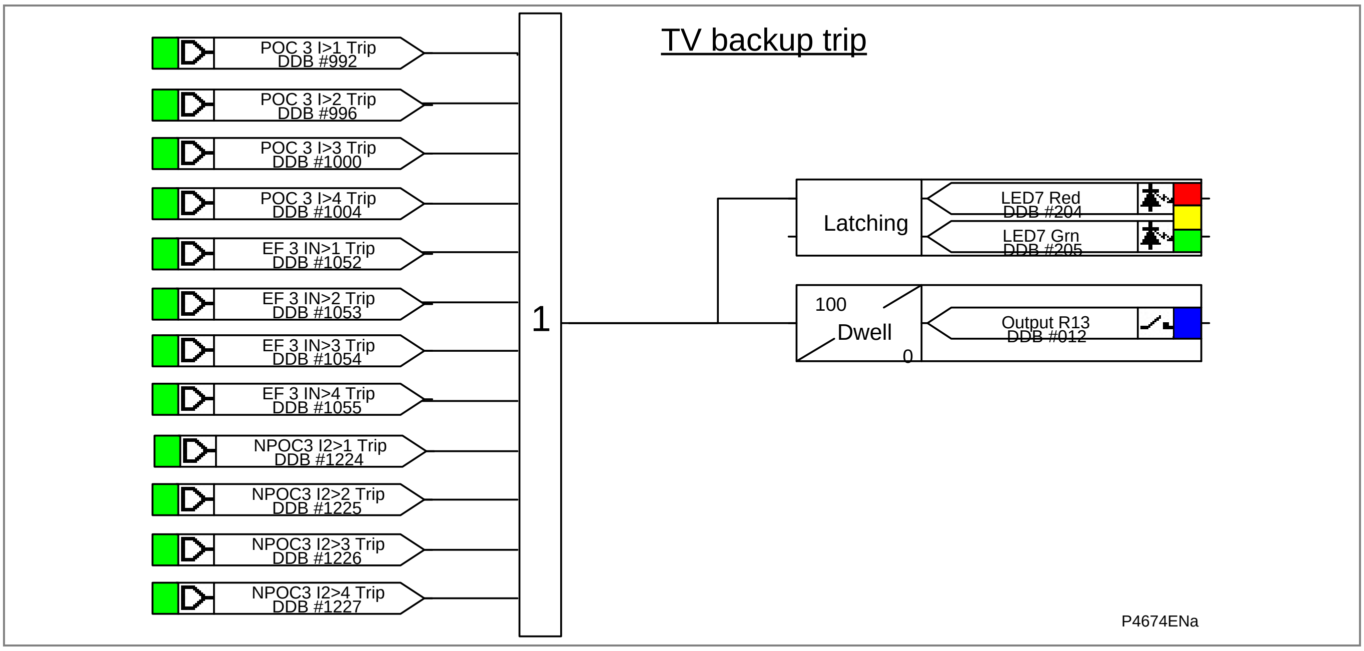

TV backup trip
POC 3 I>1 Trip DDB #992
POC 3 I>2 Trip DDB #996
POC 3 I>3 Trip DDB #1000
POC 3 I>4 Trip DDB #1004
EF 3 IN>1 Trip DDB #1052
EF 3 IN>2 Trip DDB #1053
EF 3 IN>3 Trip DDB #1054
EF 3 IN>4 Trip DDB #1055
NPOC3 I2>1 Trip DDB #1224
NPOC3 I2>2 Trip DDB #1225
NPOC3 I2>3 Trip DDB #1226
NPOC3 I2>4 Trip DDB #1227
1
Latching
LED7 Red DDB #204
LED7 Grn DDB #205
100
Dwell
0
Output R13 DDB #012
P4674ENa

Figure 18 - P643 - TV Backup trip logic mappings

5.3 General Alarm

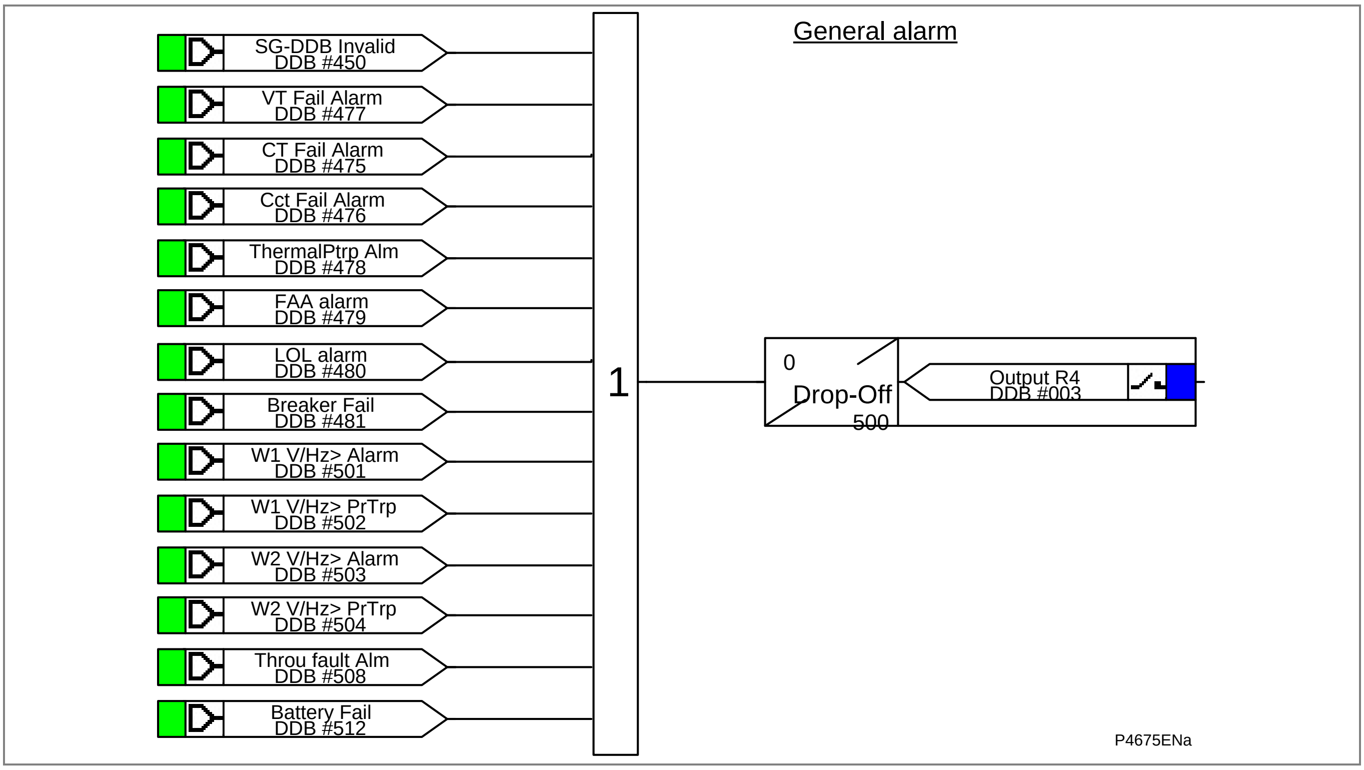

General alarm
SG-DDB Invalid DDB #450
VT Fail Alarm DDB #477
CT Fail Alarm DDB #475
Cct Fail Alarm DDB #476
ThermalPtrp Alm DDB #478
FAA alarm DDB #479
LOL alarm DDB #480
Breaker Fail DDB #481
W1 V/Hz> Alarm DDB #501
W1 V/Hz> PrTrp DDB #502
W2 V/Hz> Alarm DDB #503
W2 V/Hz> PrTrp DDB #504
Throu fault Alm DDB #508
Battery Fail DDB #512
1
0
Drop-Off
500
Output R4 DDB #003
P4675ENa

Figure 19 - P643 - General alarm mappings

5.4 Breaker Failure

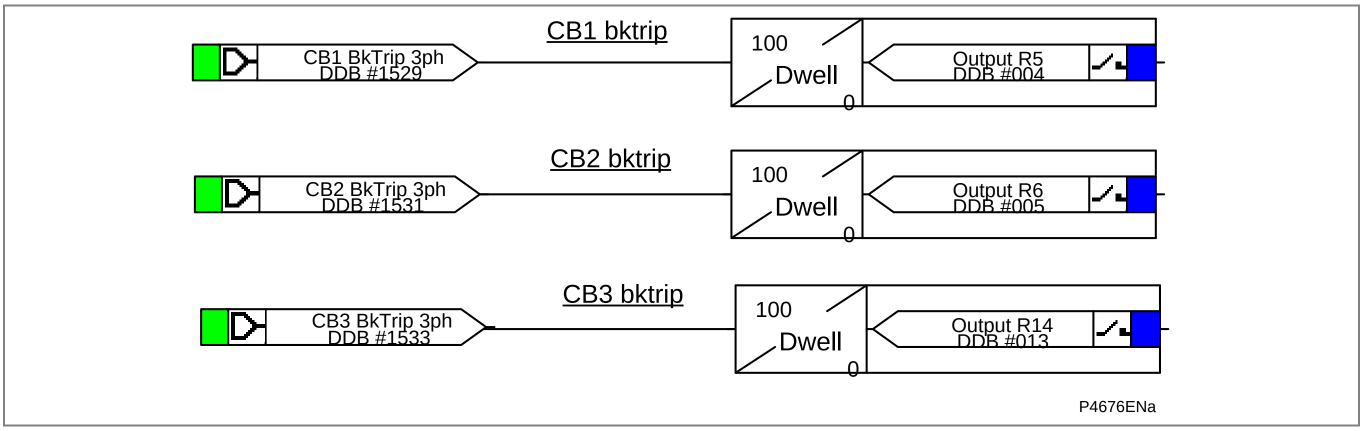

CB1 BkTrip 3ph
DDB #1529
CB1 bktrip
100
Dwell
0
Output R5
DDB #004
CB2 BkTrip 3ph
DDB #1531
CB2 bktrip
100
Dwell
0
Output R6
DDB #005
CB3 BkTrip 3ph
DDB #1533
CB3 bktrip
100
Dwell
0
Output R14
DDB #013
P4676ENa

Figure 20 - P643 - Breaker failure mappings

5.5 Any Differential Trip

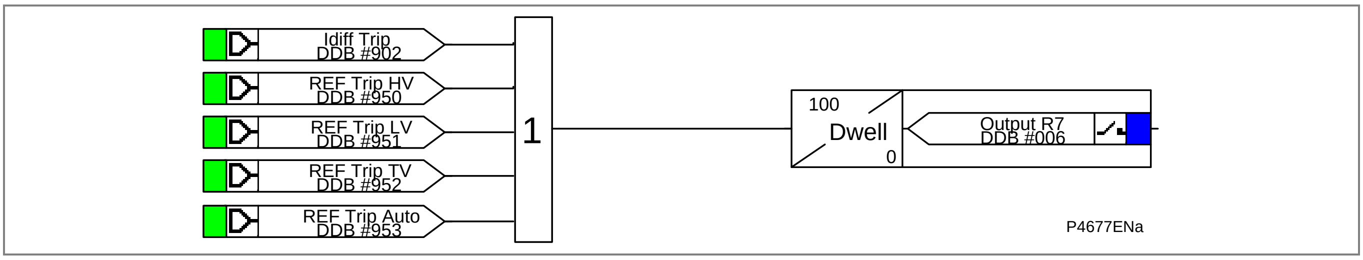

Idiff Trip
DDB #902
REF Trip HV
DDB #950
REF Trip LV
DDB #951
REF Trip TV
DDB #952
REF Trip Auto
DDB #953
1
100
Dwell
0
Output R7
DDB #006
P4677ENa

Figure 21 - P643 - Any differential trip mappings

5.6 Any Trip

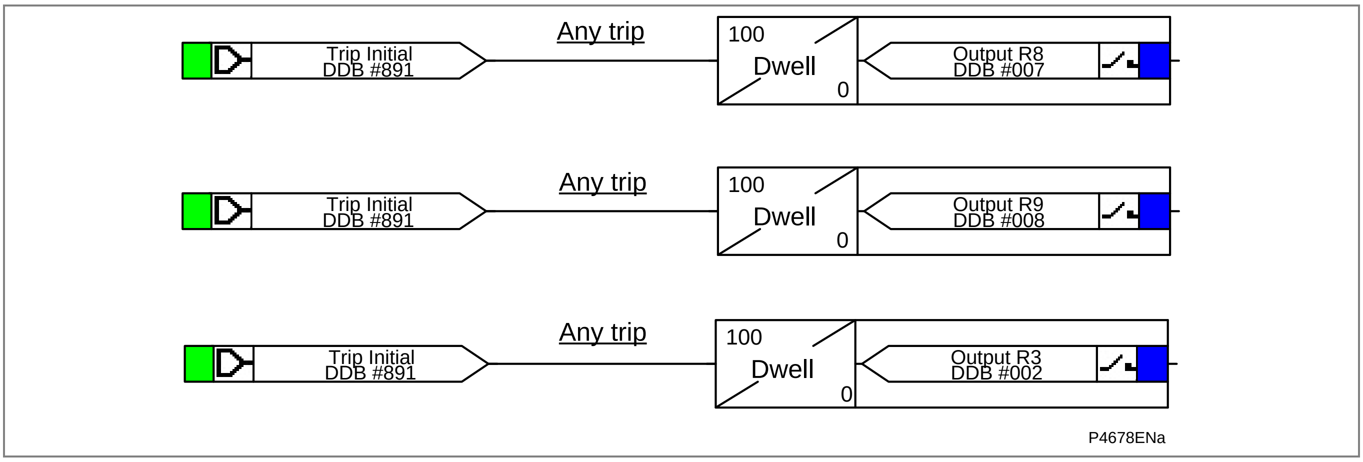

Trip Initial
DDB #891
Any trip
100
Dwell
0
Output R8
DDB #007
Trip Initial
DDB #891
Any trip
100
Dwell
0
Output R9
DDB #008
Trip Initial
DDB #891
Any trip
100
Dwell
0
Output R3
DDB #002
P4678ENa

Figure 22 - P643 - Any trip mappings

5.7 Pretrip Alarms

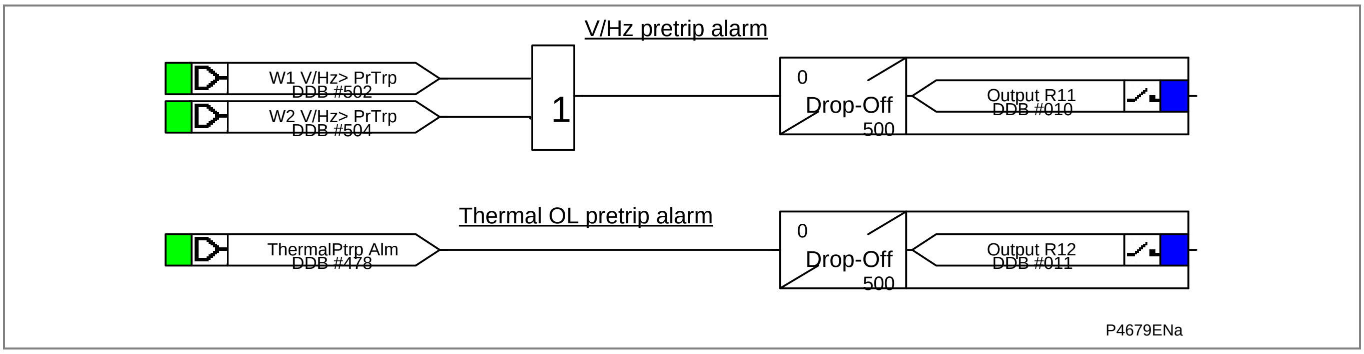

V/Hz pretrip alarm
W1 V/Hz> PrTrp
DDB #502
W2 V/Hz> PrTrp
DDB #504
1
0
Drop-Off
500
Output R11
DDB #010
Thermal OL pretrip alarm
ThermalPtrp Alm
DDB #478
0
Drop-Off
500
Output R12
DDB #011
P4679ENa

Figure 23 - P643 - Pretrip alarm mappings

5.8 Fault Recorder Trigger

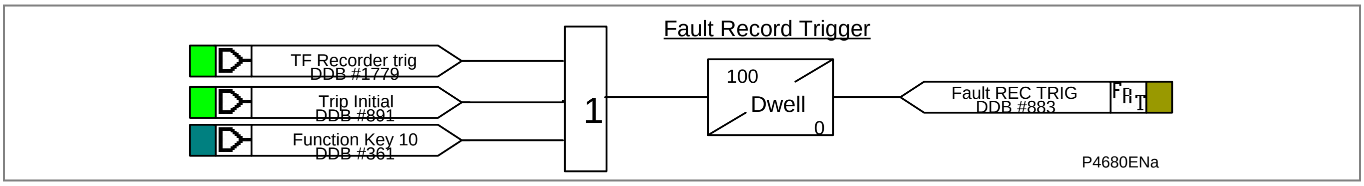

Fault Record Trigger
TF Recorder trig
DDB #1779
Trip Initial
DDB #891
Function Key 10
DDB #361
1
100
Dwell
0
Fault REC TRIG
DDB #883
P4680ENa

Figure 24 - P643 - Fault recorder trigger mappings

5.9 Opto Isolator Mappings

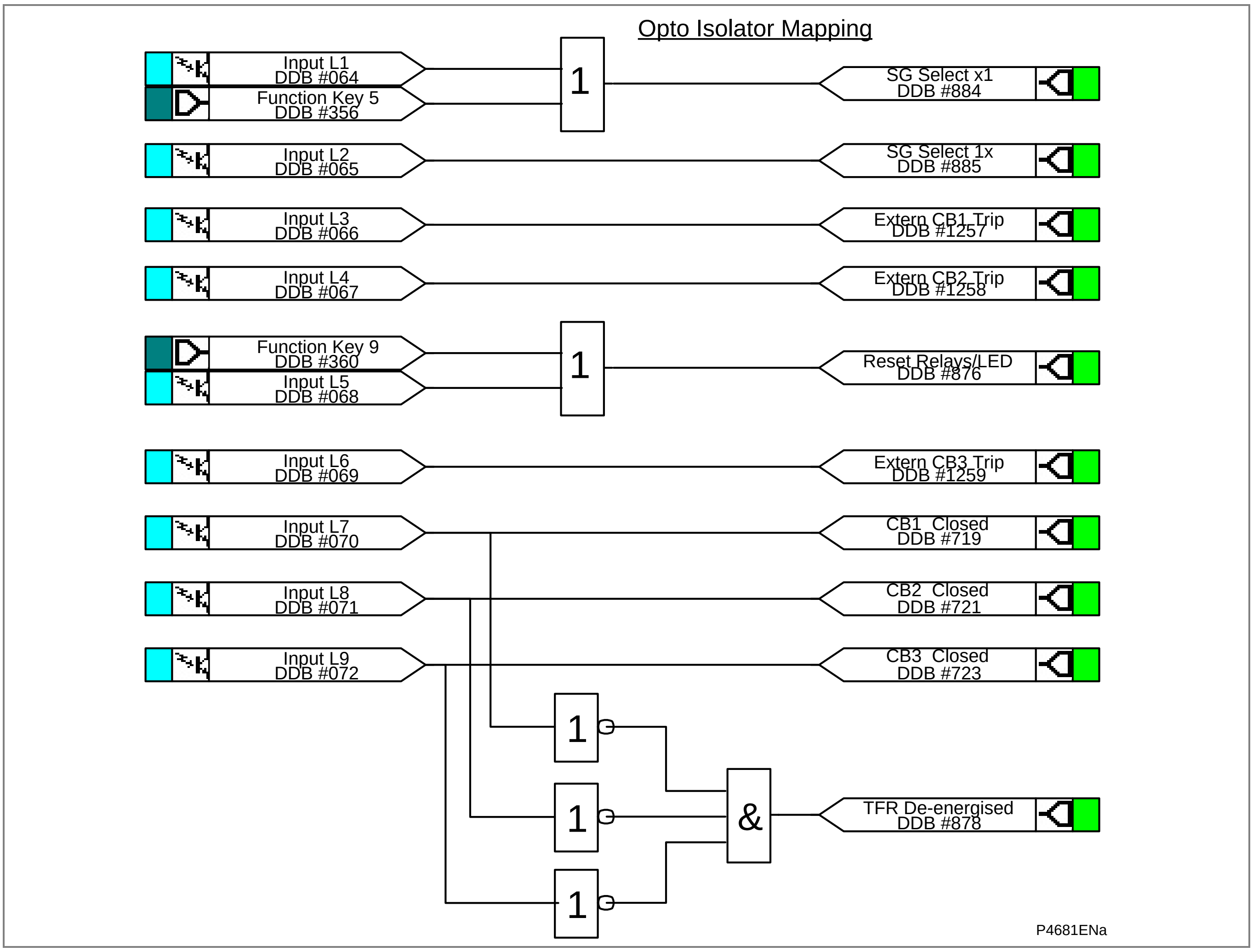

Opto Isolator Mapping
Input L1
DDB #064
Function Key 5
DDB #356
1
SG Select x1
DDB #884
Input L2
DDB #065
SG Select 1x
DDB #885
Input L3
DDB #066
Extern CB1 Trip
DDB #1257
Input L4
DDB #067
Extern CB2 Trip
DDB #1258
Function Key 9
DDB #360
Input L5
DDB #068
1
Reset Relays/LED
DDB #876
Input L6
DDB #069
Extern CB3 Trip
DDB #1259
Input L7
DDB #070
CB1 Closed
DDB #719
Input L8
DDB #071
CB2 Closed
DDB #721
Input L9
DDB #072
CB3 Closed
DDB #723
1
1
1
&
TFR De-energised
DDB #878
P4681ENa

Figure 25 - P643 - Opto isolator mappings

5.10 LED Mappings

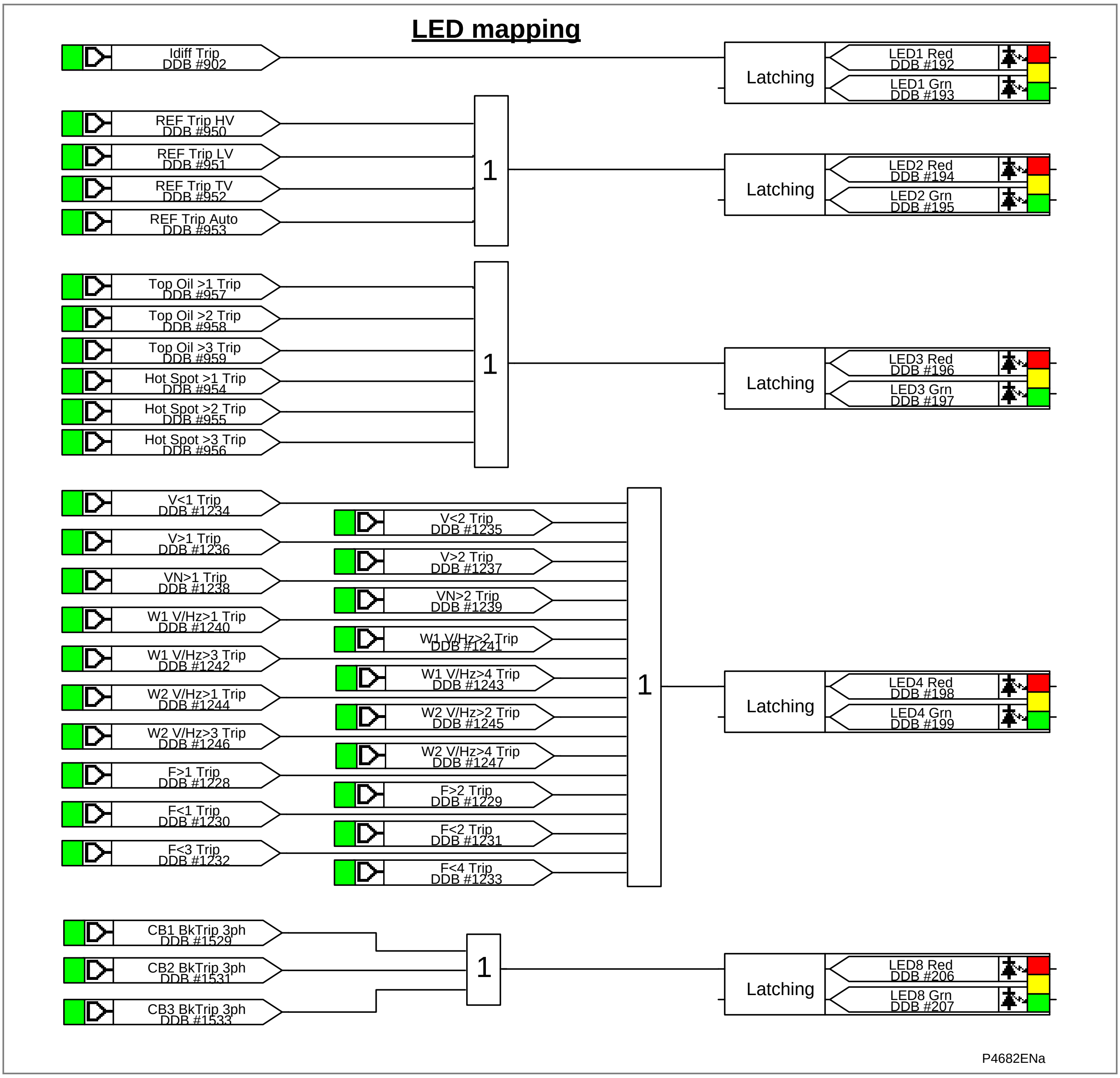

LED mapping
Idiff Trip DDB #902
REF Trip HV DDB #950
REF Trip LV DDB #951
REF Trip TV DDB #952
REF Trip Auto DDB #953
Top Oil >1 Trip DDB #957
Top Oil >2 Trip DDB #958
Top Oil >3 Trip DDB #959
Hot Spot >1 Trip DDB #954
Hot Spot >2 Trip DDB #955
Hot Spot >3 Trip DDB #956
V<1 Trip DDB #1234
V<2 Trip DDB #1235
V>1 Trip DDB #1236
V>2 Trip DDB #1237
VN>1 Trip DDB #1238
VN>2 Trip DDB #1239
W1 V/Hz>1 Trip DDB #1240
W1 V/Hz>2 Trip DDB #1241
W1 V/Hz>3 Trip DDB #1242
W1 V/Hz>4 Trip DDB #1243
W2 V/Hz>1 Trip DDB #1244
W2 V/Hz>2 Trip DDB #1245
W2 V/Hz>3 Trip DDB #1246
W2 V/Hz>4 Trip DDB #1247
F>1 Trip DDB #1228
F>2 Trip DDB #1229
F<1 Trip DDB #1230
F<2 Trip DDB #1231
F<3 Trip DDB #1232
F<4 Trip DDB #1233
CB1 BkTrip 3ph DDB #1529
CB2 BkTrip 3ph DDB #1531
CB3 BkTrip 3ph DDB #1533
1
1
1
1
Latching
Latching
Latching
Latching
Latching
LED1 Red DDB #192
LED1 Grn DDB #193
LED2 Red DDB #194
LED2 Grn DDB #195
LED3 Red DDB #196
LED3 Grn DDB #197
LED4 Red DDB #198
LED4 Grn DDB #199
LED8 Red DDB #206
LED8 Grn DDB #207
P4682ENa

Figure 26 - P643 - LED mappings

5.11 Function Key and Function LED Mapping

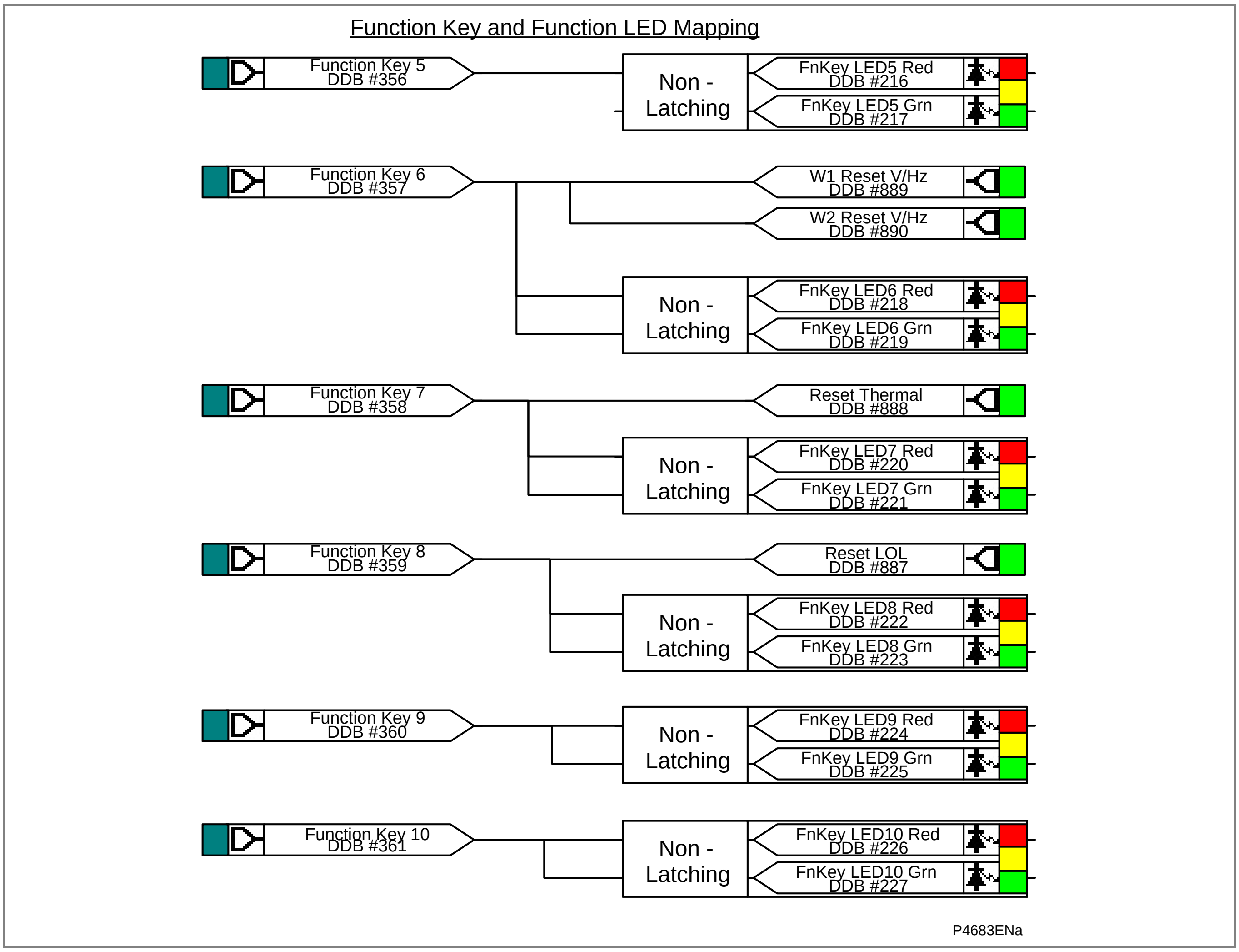

Function Key and Function LED Mapping
Function Key 5 DDB #356
Non - Latching
FnKey LED5 Red DDB #216
FnKey LED5 Grn DDB #217
Function Key 6 DDB #357
W1 Reset V/Hz DDB #889
W2 Reset V/Hz DDB #890
Non - Latching
FnKey LED6 Red DDB #218
FnKey LED6 Grn DDB #219
Function Key 7 DDB #358
Reset Thermal DDB #888
Non - Latching
FnKey LED7 Red DDB #220
FnKey LED7 Grn DDB #221
Function Key 8 DDB #359
Reset LOL DDB #887
Non - Latching
FnKey LED8 Red DDB #222
FnKey LED8 Grn DDB #223
Function Key 9 DDB #360
Non - Latching
FnKey LED9 Red DDB #224
FnKey LED9 Grn DDB #225
Function Key 10 DDB #361
Non - Latching
FnKey LED10 Red DDB #226
FnKey LED10 Grn DDB #227
P4683ENa

Figure 27 - P643 - Function key and function LED mappings

6 MICOM P645 PSL DIAGRAMS

6.1 Any Trip Mapping

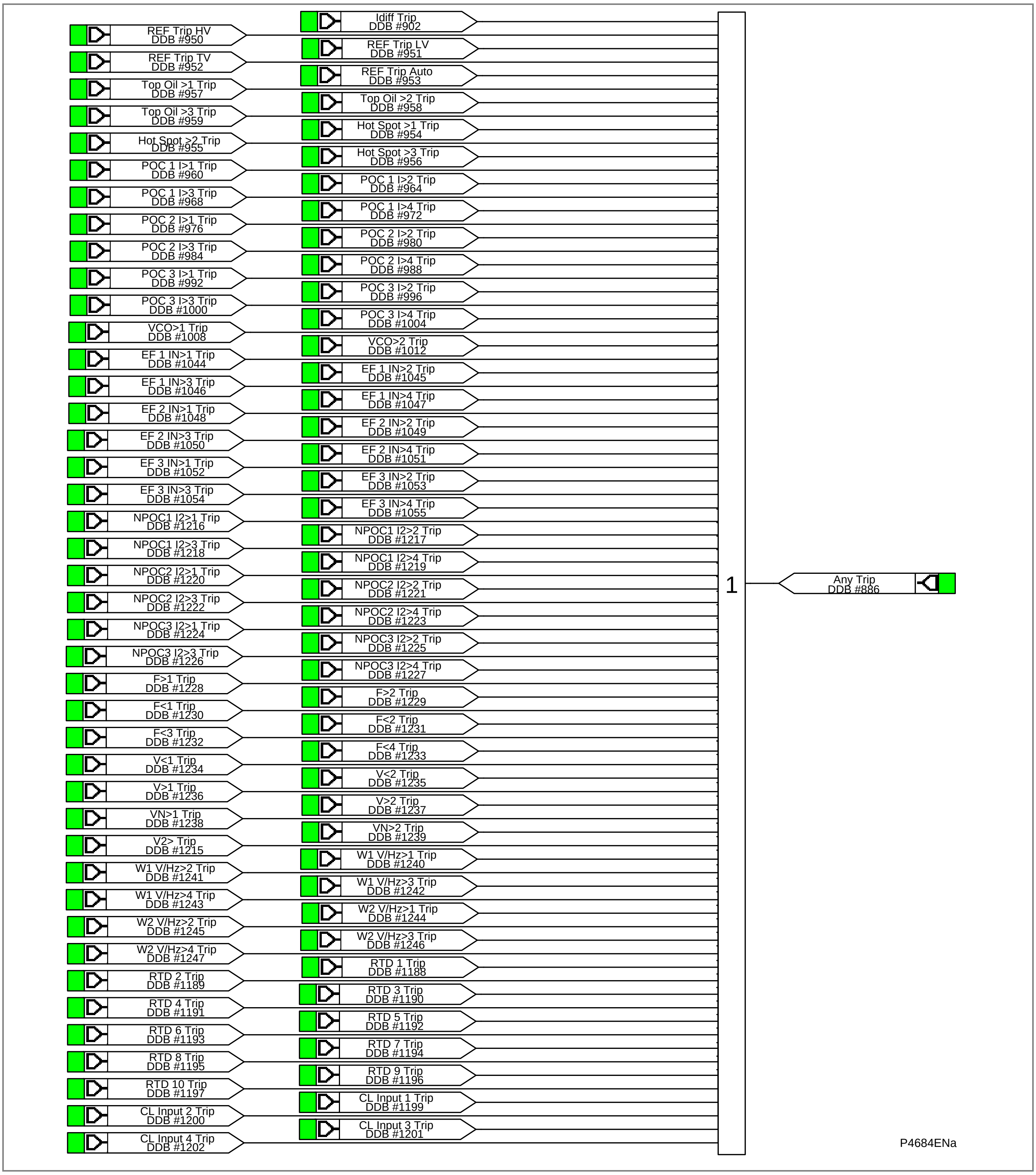

REF Trip HV DDB #950
REF Trip TV DDB #952
Top Oil >1 Trip DDB #957
Top Oil >3 Trip DDB #959
Hot Spot >2 Trip DDB #955
POC 1 I>1 Trip DDB #960
POC 1 I>3 Trip DDB #968
POC 2 I>1 Trip DDB #976
POC 2 I>3 Trip DDB #984
POC 3 I>1 Trip DDB #992
POC 3 I>3 Trip DDB #1000
VCO>1 Trip DDB #1008
EF 1 IN>1 Trip DDB #1044
EF 1 IN>3 Trip DDB #1046
EF 2 IN>1 Trip DDB #1048
EF 2 IN>3 Trip DDB #1050
EF 3 IN>1 Trip DDB #1052
EF 3 IN>3 Trip DDB #1054
NPOC1 I2>1 Trip DDB #1216
NPOC1 I2>3 Trip DDB #1218
NPOC2 I2>1 Trip DDB #1220
NPOC2 I2>3 Trip DDB #1222
NPOC3 I2>1 Trip DDB #1224
NPOC3 I2>3 Trip DDB #1226
F>1 Trip DDB #1228
F<1 Trip DDB #1230
F<3 Trip DDB #1232
V<1 Trip DDB #1234
V>1 Trip DDB #1236
VN>1 Trip DDB #1238
V2> Trip DDB #1215
W1 V/Hz>2 Trip DDB #1241
W1 V/Hz>4 Trip DDB #1243
W2 V/Hz>2 Trip DDB #1245
W2 V/Hz>4 Trip DDB #1247
RTD 2 Trip DDB #1189
RTD 4 Trip DDB #1191
RTD 6 Trip DDB #1193
RTD 8 Trip DDB #1195
RTD 10 Trip DDB #1197
CL Input 2 Trip DDB #1200
CL Input 4 Trip DDB #1202
Idiff Trip DDB #902
REF Trip LV DDB #951
REF Trip Auto DDB #953
Top Oil >2 Trip DDB #958
Hot Spot >1 Trip DDB #954
Hot Spot >3 Trip DDB #956
POC 1 I>2 Trip DDB #964
POC 1 I>4 Trip DDB #972
POC 2 I>2 Trip DDB #980
POC 2 I>4 Trip DDB #988
POC 3 I>2 Trip DDB #996
POC 3 I>4 Trip DDB #1004
VCO>2 Trip DDB #1012
EF 1 IN>2 Trip DDB #1045
EF 1 IN>4 Trip DDB #1047
EF 2 IN>2 Trip DDB #1049
EF 2 IN>4 Trip DDB #1051
EF 3 IN>2 Trip DDB #1053
EF 3 IN>4 Trip DDB #1055
NPOC1 I2>2 Trip DDB #1217
NPOC1 I2>4 Trip DDB #1219
NPOC2 I2>2 Trip DDB #1221
NPOC2 I2>4 Trip DDB #1223
NPOC3 I2>2 Trip DDB #1225
NPOC3 I2>4 Trip DDB #1227
F>2 Trip DDB #1229
F<2 Trip DDB #1231
F<4 Trip DDB #1233
V<2 Trip DDB #1235
V>2 Trip DDB #1237
VN>2 Trip DDB #1239
W1 V/Hz>1 Trip DDB #1240
W1 V/Hz>3 Trip DDB #1242
W2 V/Hz>1 Trip DDB #1244
W2 V/Hz>3 Trip DDB #1246
RTD 1 Trip DDB #1188
RTD 3 Trip DDB #1190
RTD 5 Trip DDB #1192
RTD 7 Trip DDB #1194
RTD 9 Trip DDB #1196
CL Input 1 Trip DDB #1199
CL Input 3 Trip DDB #1201
1
Any Trip DDB #886
P4684ENa

Figure 28 - P645 - Any trip mappings

6.2 Backup Trip Logic

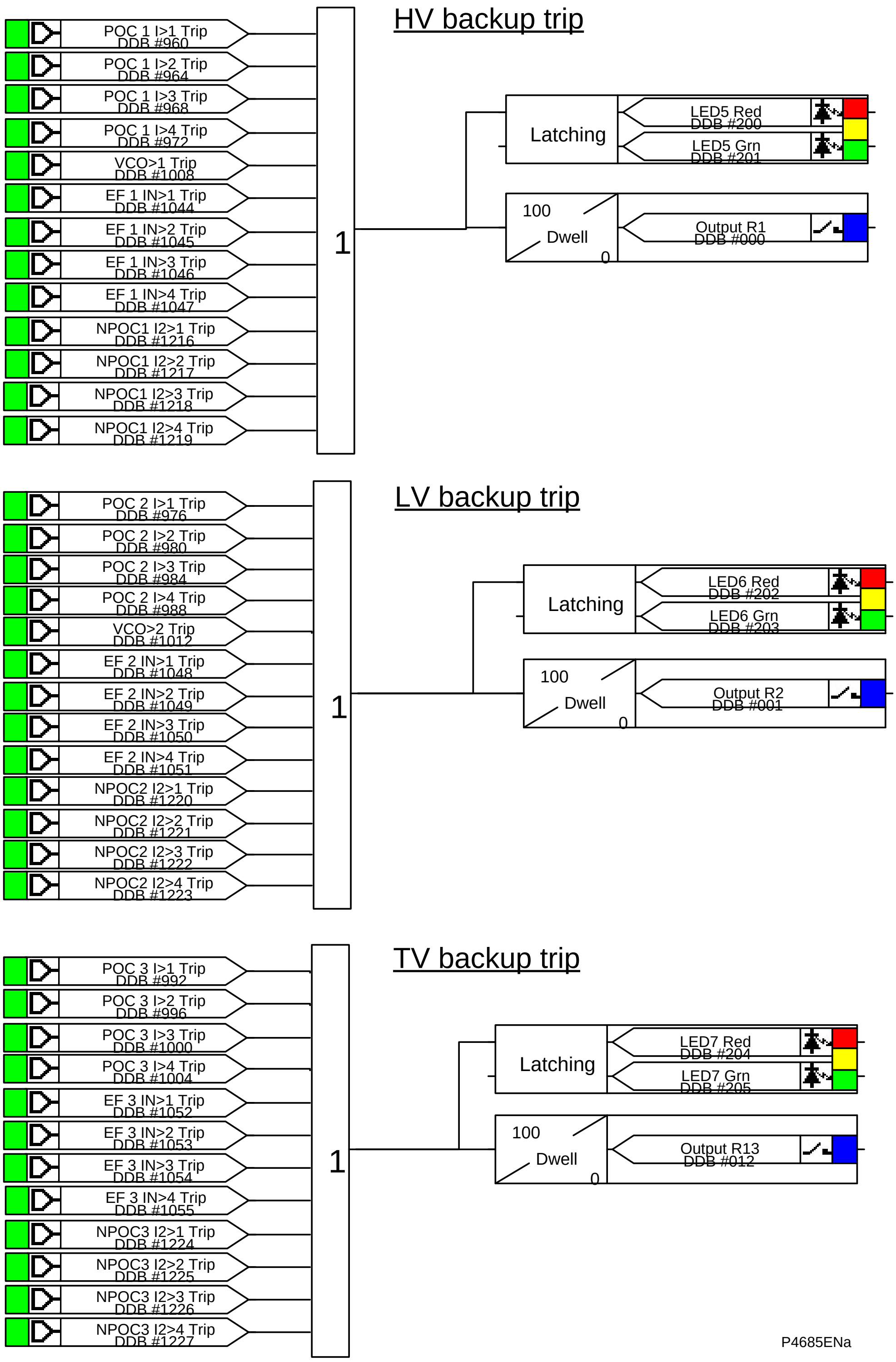

HV backup trip
POC 1 I>1 Trip DDB #960
POC 1 I>2 Trip DDB #964
POC 1 I>3 Trip DDB #968
POC 1 I>4 Trip DDB #972
VCO>1 Trip DDB #1008
EF 1 IN>1 Trip DDB #1044
EF 1 IN>2 Trip DDB #1045
EF 1 IN>3 Trip DDB #1046
EF 1 IN>4 Trip DDB #1047
NPOC1 I2>1 Trip DDB #1216
NPOC1 I2>2 Trip DDB #1217
NPOC1 I2>3 Trip DDB #1218
NPOC1 I2>4 Trip DDB #1219
1
Latching
LED5 Red DDB #200
LED5 Grn DDB #201
100
Dwell
0
Output R1 DDB #000
LV backup trip
POC 2 I>1 Trip DDB #976
POC 2 I>2 Trip DDB #980
POC 2 I>3 Trip DDB #984
POC 2 I>4 Trip DDB #988
VCO>2 Trip DDB #1012
EF 2 IN>1 Trip DDB #1048
EF 2 IN>2 Trip DDB #1049
EF 2 IN>3 Trip DDB #1050
EF 2 IN>4 Trip DDB #1051
NPOC2 I2>1 Trip DDB #1220
NPOC2 I2>2 Trip DDB #1221
NPOC2 I2>3 Trip DDB #1222
NPOC2 I2>4 Trip DDB #1223
1
Latching
LED6 Red DDB #202
LED6 Grn DDB #203
100
Dwell
0
Output R2 DDB #001
TV backup trip
POC 3 I>1 Trip DDB #992
POC 3 I>2 Trip DDB #996
POC 3 I>3 Trip DDB #1000
POC 3 I>4 Trip DDB #1004
EF 3 IN>1 Trip DDB #1052
EF 3 IN>2 Trip DDB #1053
EF 3 IN>3 Trip DDB #1054
EF 3 IN>4 Trip DDB #1055
NPOC3 I2>1 Trip DDB #1224
NPOC3 I2>2 Trip DDB #1225
NPOC3 I2>3 Trip DDB #1226
NPOC3 I2>4 Trip DDB #1227
1
Latching
LED7 Red DDB #204
LED7 Grn DDB #205
100
Dwell
0
Output R13 DDB #012
P4685ENa

Figure 29 - P645 - Backup trip logic mappings

6.3 General Alarm

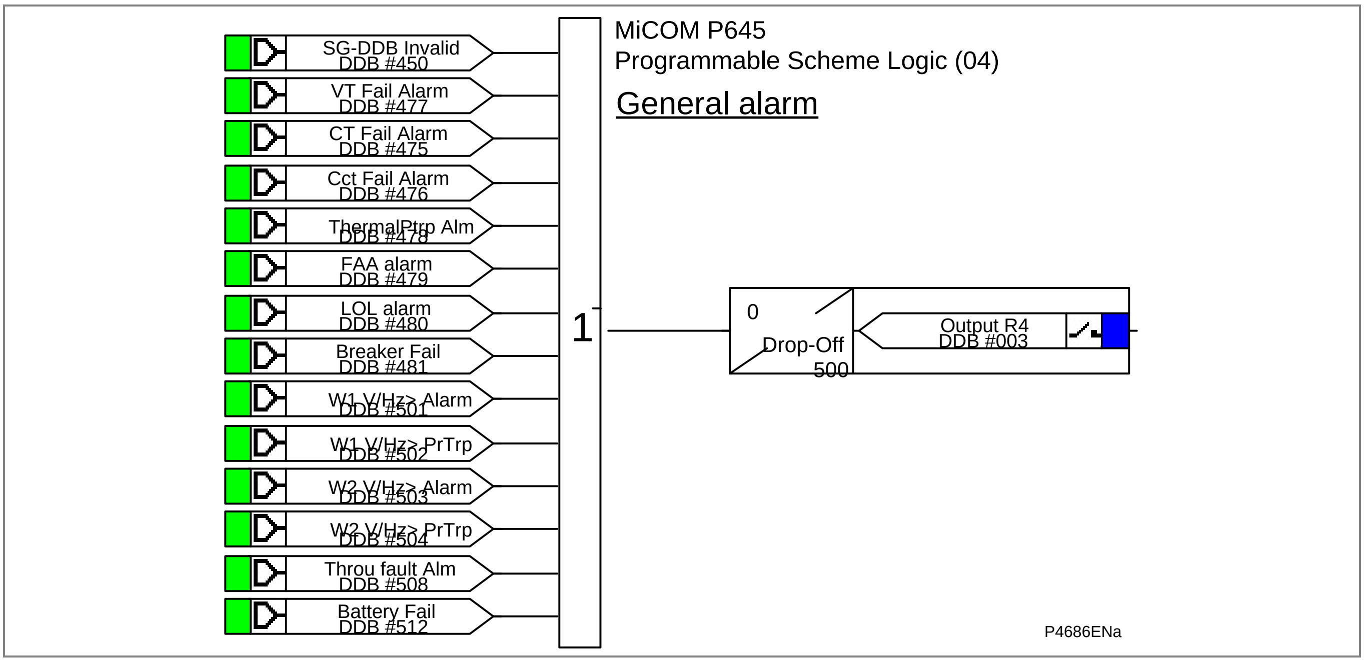

MiCOM P645
Programmable Scheme Logic (04)
General alarm
SG-DDB Invalid
DDB #450
VT Fail Alarm
DDB #477
CT Fail Alarm
DDB #475
Cct Fail Alarm
DDB #476
ThermalPtrp Alm
DDB #478
FAA alarm
DDB #479
LOL alarm
DDB #480
Breaker Fail
DDB #481
W1 V/Hz> Alarm
DDB #501
W1 V/Hz> PrTrp
DDB #502
W2 V/Hz> Alarm
DDB #503
W2 V/Hz> PrTrp
DDB #504
Throu fault Alm
DDB #508
Battery Fail
DDB #512
1
0
Drop-Off
500
Output R4
DDB #003
P4686ENa

Figure 30 - P645 - General alarm mappings

6.4 Breaker Failure

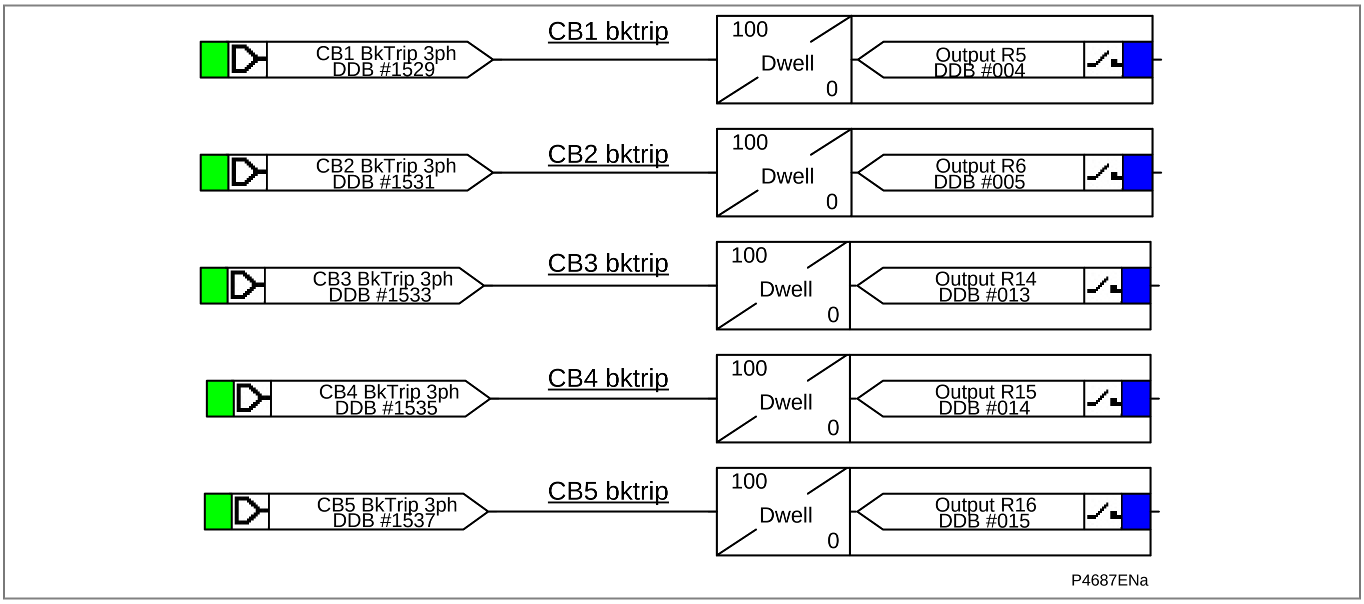

CB1 BkTrip 3ph
DDB #1529
CB1 bktrip
100
Dwell
0
Output R5
DDB #004
CB2 BkTrip 3ph
DDB #1531
CB2 bktrip
100
Dwell
0
Output R6
DDB #005
CB3 BkTrip 3ph
DDB #1533
CB3 bktrip
100
Dwell
0
Output R14
DDB #013
CB4 BkTrip 3ph
DDB #1535
CB4 bktrip
100
Dwell
0
Output R15
DDB #014
CB5 BkTrip 3ph
DDB #1537
CB5 bktrip
100
Dwell
0
Output R16
DDB #015
P4687ENa

Figure 31 - P645 - Breaker failure mappings

6.5 Any Differential Trip

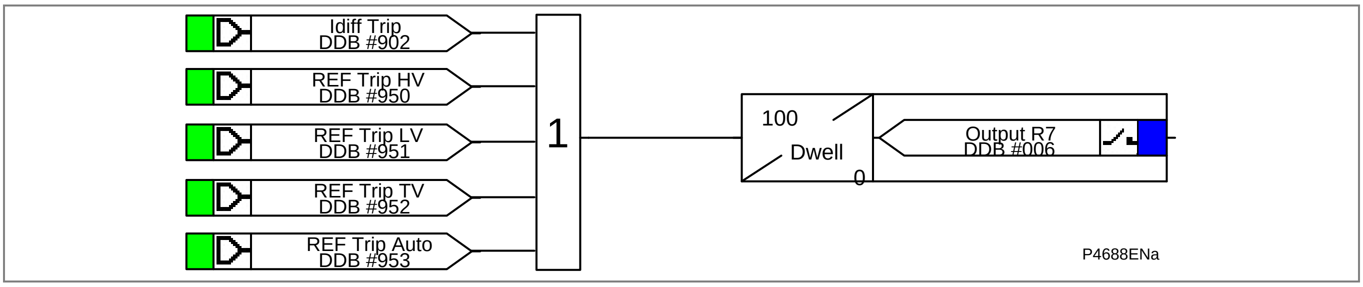

Idiff Trip
DDB #902
REF Trip HV
DDB #950
REF Trip LV
DDB #951
REF Trip TV
DDB #952
REF Trip Auto
DDB #953
1
100
Dwell
0
Output R7
DDB #006
P4688ENa

Figure 32 - P645 - Any differential trip mappings

6.6 Any Trip

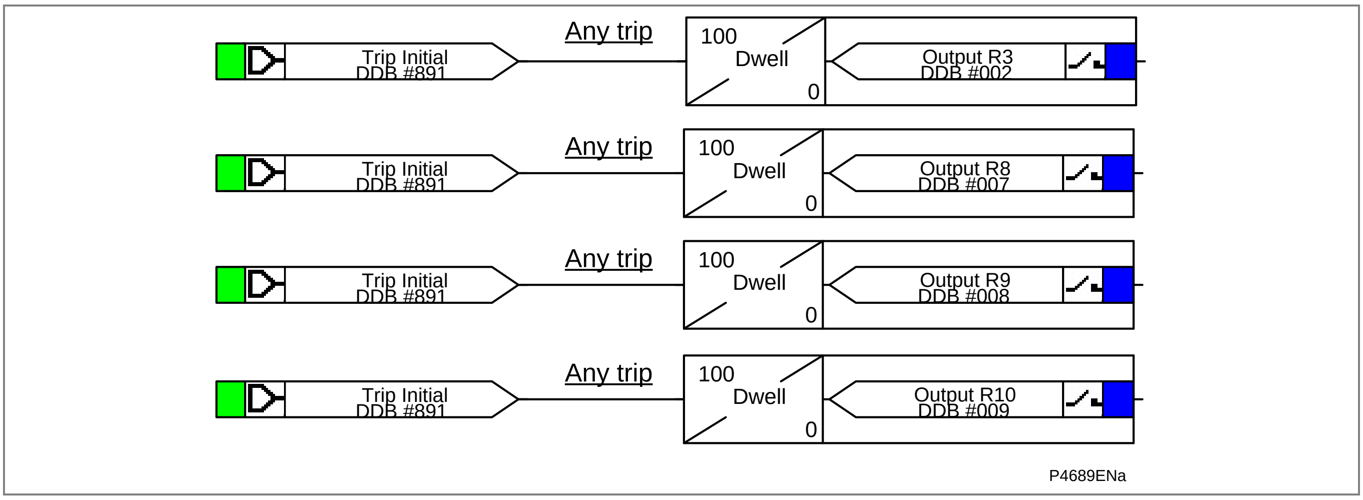

Trip Initial
DDB #891
Any trip
100
Dwell
0
Output R3
DDB #002
Trip Initial
DDB #891
Any trip
100
Dwell
0
Output R8
DDB #007
Trip Initial
DDB #891
Any trip
100
Dwell
0
Output R9
DDB #008
Trip Initial
DDB #891
Any trip
100
Dwell
0
Output R10
DDB #009
P4689ENa

Figure 33 - P645 - Any trip mappings

6.7 Pretrip Alarms

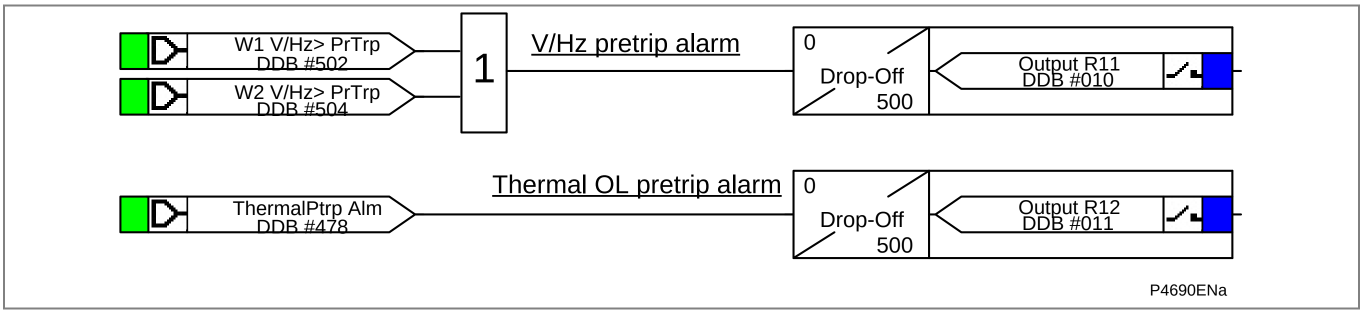

W1 V/Hz> PrTrp
DDB #502
W2 V/Hz> PrTrp
DDB #504
1
V/Hz pretrip alarm
0
Drop-Off
500
Output R11
DDB #010
ThermalPtrp Alm
DDB #478
Thermal OL pretrip alarm
0
Drop-Off
500
Output R12
DDB #011
P4690ENa

Figure 34 - P645 - Pretrip alarm mappings

6.8 Fault Record Trigger

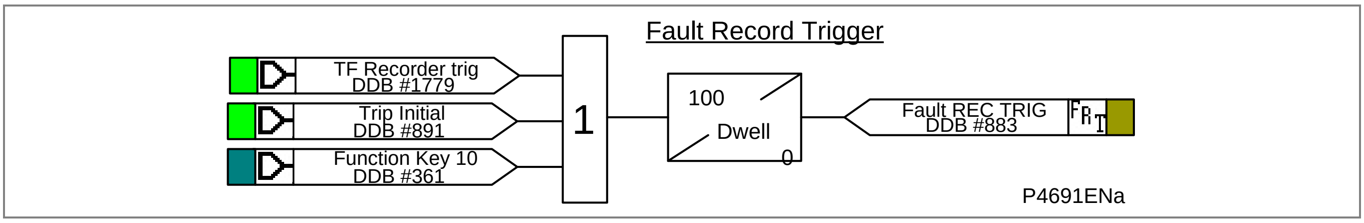

Fault Record Trigger
TF Recorder trig
DDB #1779
Trip Initial
DDB #891
Function Key 10
DDB #361
1
100
Dwell
0
Fault REC TRIG
DDB #883
P4691ENa

Figure 35 - P645 - Fault record trigger mappings

6.9 Opto Isolator Mappings

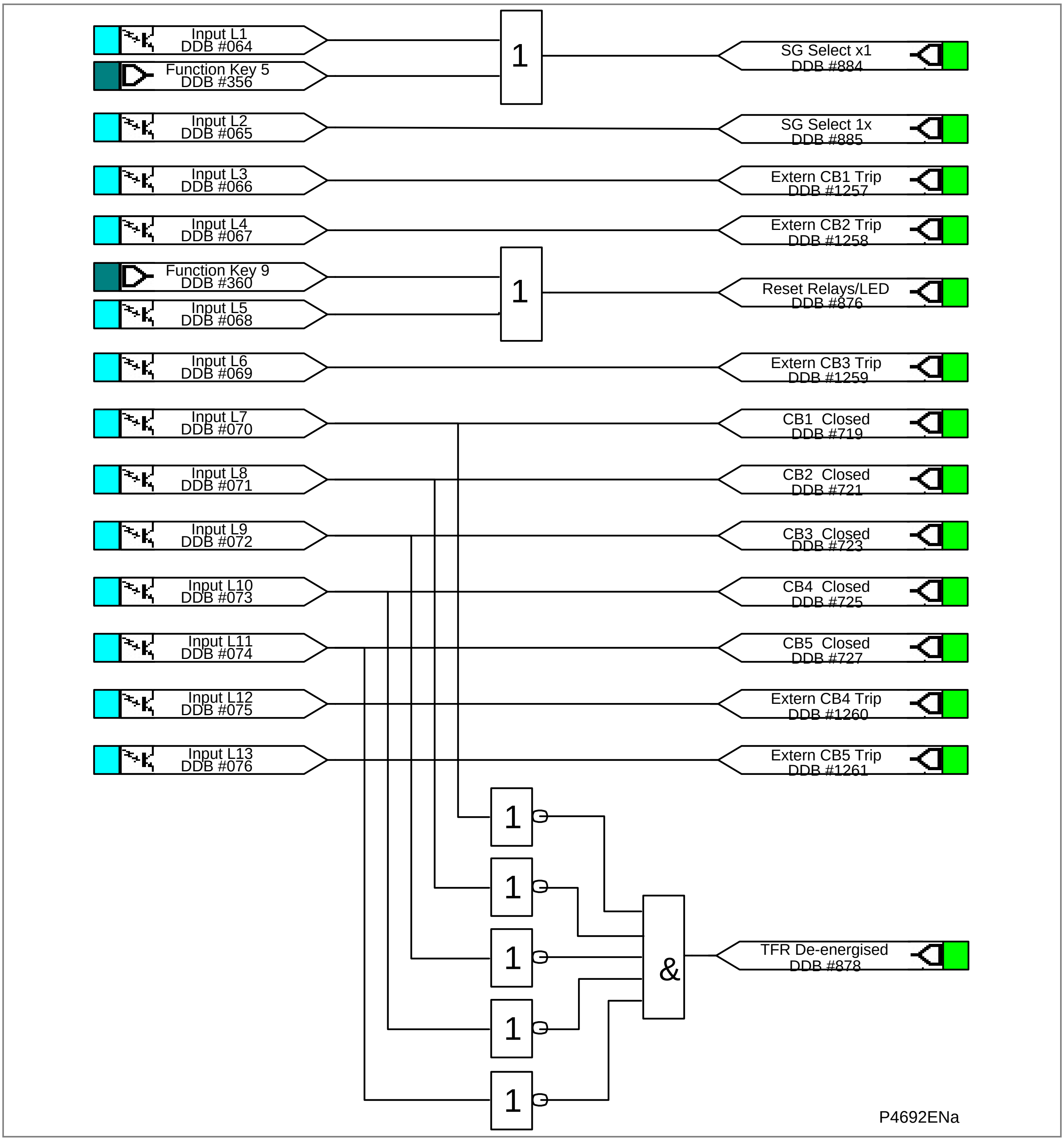

Input L1
DDB #064
Function Key 5
DDB #356
Input L2
DDB #065
Input L3
DDB #066
Input L4
DDB #067
Function Key 9
DDB #360
Input L5
DDB #068
Input L6
DDB #069
Input L7
DDB #070
Input L8
DDB #071
Input L9
DDB #072
Input L10
DDB #073
Input L11
DDB #074
Input L12
DDB #075
Input L13
DDB #076
1
1
1
1
1
1
1
&
SG Select x1
DDB #884
SG Select 1x
DDB #885
Extern CB1 Trip
DDB #1257
Extern CB2 Trip
DDB #1258
Reset Relays/LED
DDB #876
Extern CB3 Trip
DDB #1259
CB1 Closed
DDB #719
CB2 Closed
DDB #721
CB3 Closed
DDB #723
CB4 Closed
DDB #725
CB5 Closed
DDB #727
Extern CB4 Trip
DDB #1260
Extern CB5 Trip
DDB #1261
TFR De-energised
DDB #878
P4692ENa

Figure 36 - P645 - Opto isolator mappings

6.10 LED Mappings

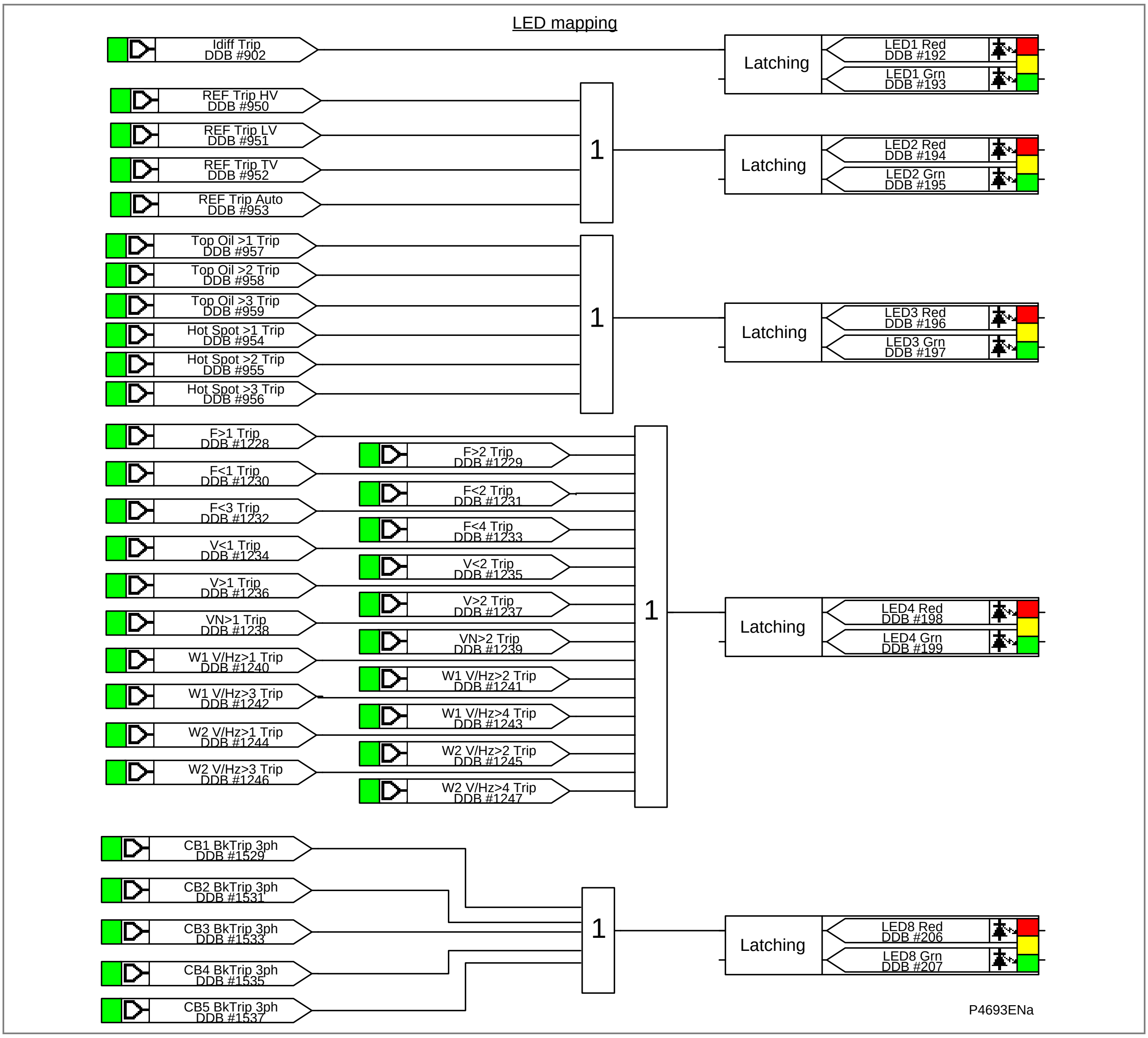

LED mapping
Idiff Trip DDB #902
REF Trip HV DDB #950
REF Trip LV DDB #951
REF Trip TV DDB #952
REF Trip Auto DDB #953
Top Oil >1 Trip DDB #957
Top Oil >2 Trip DDB #958
Top Oil >3 Trip DDB #959
Hot Spot >1 Trip DDB #954
Hot Spot >2 Trip DDB #955
Hot Spot >3 Trip DDB #956
F>1 Trip DDB #1228
F>2 Trip DDB #1229
F<1 Trip DDB #1230
F<2 Trip DDB #1231
F<3 Trip DDB #1232
F<4 Trip DDB #1233
V<1 Trip DDB #1234
V<2 Trip DDB #1235
V>1 Trip DDB #1236
V>2 Trip DDB #1237
VN>1 Trip DDB #1238
VN>2 Trip DDB #1239
W1 V/Hz>1 Trip DDB #1240
W1 V/Hz>2 Trip DDB #1241
W1 V/Hz>3 Trip DDB #1242
W1 V/Hz>4 Trip DDB #1243
W2 V/Hz>1 Trip DDB #1244
W2 V/Hz>2 Trip DDB #1245
W2 V/Hz>3 Trip DDB #1246
W2 V/Hz>4 Trip DDB #1247
CB1 BkTrip 3ph DDB #1529
CB2 BkTrip 3ph DDB #1531
CB3 BkTrip 3ph DDB #1533
CB4 BkTrip 3ph DDB #1535
CB5 BkTrip 3ph DDB #1537
1
1
1
1
Latching
LED1 Red DDB #192
LED1 Grn DDB #193
Latching
LED2 Red DDB #194
LED2 Grn DDB #195
Latching
LED3 Red DDB #196
LED3 Grn DDB #197
Latching
LED4 Red DDB #198
LED4 Grn DDB #199
Latching
LED8 Red DDB #206
LED8 Grn DDB #207
P4693ENa

Figure 37 - P645 - LED mappings

6.11 Function Key and Function LED Mapping

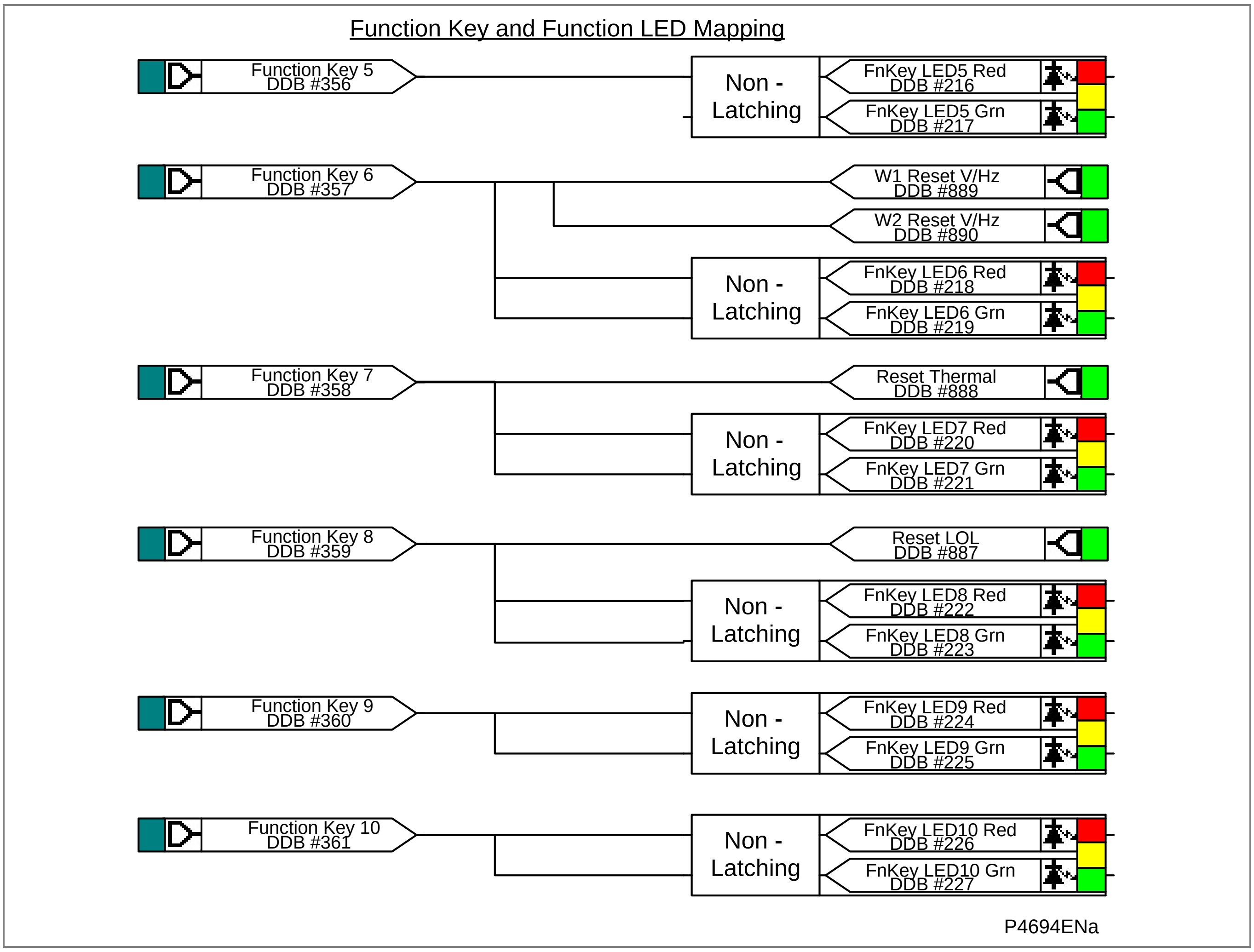

Function Key and Function LED Mapping
Function Key 5 DDB #356
Non - Latching
FnKey LED5 Red DDB #216
FnKey LED5 Grn DDB #217
Function Key 6 DDB #357
W1 Reset V/Hz DDB #889
W2 Reset V/Hz DDB #890
Non - Latching
FnKey LED6 Red DDB #218
FnKey LED6 Grn DDB #219
Function Key 7 DDB #358
Reset Thermal DDB #888
Non - Latching
FnKey LED7 Red DDB #220
FnKey LED7 Grn DDB #221
Function Key 8 DDB #359
Reset LOL DDB #887
Non - Latching
FnKey LED8 Red DDB #222
FnKey LED8 Grn DDB #223
Function Key 9 DDB #360
Non - Latching
FnKey LED9 Red DDB #224
FnKey LED9 Grn DDB #225
Function Key 10 DDB #361
Non - Latching
FnKey LED10 Red DDB #226
FnKey LED10 Grn DDB #227
P4694ENa

Figure 38 - P645 - Function key and function LED mappings

MEASUREMENTS AND RECORDING

CHAPTER NO 8

Date:	12/2013
Hardware Suffix:	J (P642) K (P643/P645)
Software Version:	04
Connection Diagrams:	10P642xx (xx = 1 to 10) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9)

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1 INTRODUCTION

The P64x is equipped with integral measurements, event, fault and disturbance recording facilities suitable for analysis of complex system disturbances.

The relay is flexible enough to allow for the programming of these facilities to specific user application requirements. These requirements are discussed in the sections which follow.

2 EVENT AND FAULT RECORDS

The relay records and time tags up to 512 events and stores them in non-volatile (battery-backed up) memory. This enables the system operator to establish the sequence of events that occurred in the relay following a particular power system condition or switching sequence. When the available space is used up, the oldest event is automatically overwritten by the new one.

The real-time clock in the relay provides the time tag to each event, to a resolution of 1 ms.

The event records can be viewed either from the frontplate LCD or remotely using the communications ports.

For local viewing on the LCD of event, fault and maintenance records, select the **VIEW RECORDS** menu column. See Table 1.

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
VIEW RECORDS				
Select Event	0	0	511	
Setting range from 0 to 511. This selects the required event record from the possible 512 that may be stored. A value of 0 corresponds to the latest event and so on.				
Menu Cell Ref	(From record)	Latched alarm active, Latched alarm inactive, Self reset alarm active, Self reset alarm inactive, Relay contact event, Opto-isolated input event, Protection event, General event, Fault record event, Maintenance record event		
Indicates the type of event.				
Time and Date	Data			
Time & Date Stamp for the event given by the internal Real Time Clock.				
Event text	Data.			
Up to 32 Character description of the Event. See the event sheet in the Relay Menu Database document, P64x/EN/MD.				
Event Value	Data.			
32-bit binary string indicating ON or OFF (1 or 0) status of relay contact, opto input, alarm or protection event, depending on event type. Unsigned integer is used for maintenance records. See the event sheet in the Relay Menu Database document, P64x/EN/MD for details.				
Select Fault	0	0	4	1
Setting range from 0 to 4. This selects the required fault record from the possible 5 that may be stored. A value of 0 corresponds to the latest fault and so on.				
Faulted Phase	00000000			
Displays the faulted phase as a binary string, bits 0 – 8 = Start A/B/C/N Trip A/B/C/N.				
Start elements 1	00000000000000000000000000000000			
32-bit binary string. Gives the status of the first 32 start signals. See Data Type G84 in the Relay Menu Database document, P64x/EN/MD for details.				
Start elements 2	00000000000000000000000000000000			
32-bit binary string. Gives the status of the second 32 start signals. See Data Type G107 in the Relay Menu Database document, P64x/EN/MD for details.				
Start elements 3	00000000000000000000000000000000			
32-bit binary string. Gives the status of the third 32 start signals. See Data Type G129 in the Relay Menu Database document, P64x/EN/MD for details.				
Trip elements 1	00000000000000000000000000000000			
32-bit binary string. Gives the status of the first 32 trip signals. See Data Type G85 in the Relay Menu Database document, P64x/EN/MD for details.				

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
VIEW RECORDS				
Trip elements 2	00000000000000000000000000000000			
32-bit binary string gives the status of the second 32 trip signals. See Data Type G86 in the Relay Menu Database document, P64x/EN/MD for details.				
Trip elements 3	00000000000000000000000000000000			
32-bit binary string Gives the status of the third 32 trip signals. See Data Type G130 in the Relay Menu Database document, P64x/EN/MD for details.				
Fault Alarms	0000001000000000			
32-bit binary string Gives the status of the fault alarm signals. See Data Type G87 in the Relay Menu Database document, P64x/EN/MD for details.				
Fault Time	Data.			
Fault time and date.				
Active Group	Data.			
Active setting group 1-4.				
System Frequency	Data			
System frequency.				
Fault Duration				
Fault duration. Time from the start or trip until the undercurrent elements indicate the CB is open.				
CB Operate Time	Data.			
CB operating time. Time from protection trip to undercurrent elements indicating the CB is open.				
Relay Trip Time	Data.			
Relay trip time. Time from protection start to protection trip.				
The following cells provide measurement information of the fault : IA-1, IB-1, IC-1, IA-2, IB-2, IC-2, IA-3, IB-3, IC-3, IA-4, IB-4, IC-4, IA-5, IB-5, IC-5, IA-HV, IB-HV, IC-HV, IA-LV, IB-LV, IC-LV, IA-TV, IB-TV, IC-TV, I2-HV, I2-LV, I2-TV, IN-HV Mea, IN-LV Mea, IN-TV Mea, VAN, VBN, VCN, Vx, V1, V2, VN derived, VAB, VBC, VCA, IA Differential, IB Differential, IC Differential, IA Biased, IB Biased, IC Biased, IREF HV LoZ Diff, IREF HV LoZ Bias, IREF LV LoZ Diff, IREF LV LoZ Bias, IREF TV LoZ Diff, IREF TV LoZ Bias, IREF Auto LoZ Diff, IREF Auto LoZ Bias, IREF HV HighZ Op, IREF HV HighZ Op, IREF HV HighZ Op, IREF LV HighZ Op, IREF TV HighZ Op, IREF Auto HighZ Op, IA Peak, IB Peak, IC Peak, I2t phase A, I2t phase B, I2t phase C, RTD 1-10, CLIO Input 1-4				
Reset Indication	No	No, Yes		N/A
Resets latched LEDs and latched relay contacts, provided the relevant protection element has reset.				

Table 1 - View Records

For extraction from a remote source using communications, see the *SCADA Communications* chapter *P64x/EN SC*.

For a full list of all the event types and the meaning of their values, see the Relay Menu Database document P64x/EN MD.

2.1 Types of Event

An event may be a change of state of a control input or output relay, an alarm condition, or a setting change. Sections 2.1.1 to 2.1.7 show the various items that constitute an event:

2.1.1 Change of State of Opto-Isolated Inputs

If one or more of the opto (logic) inputs has changed state since the last time the protection algorithm ran, the new status is logged as an event. When this event is selected to be viewed on the LCD, three cells appear, as in Table 2:

Time and Date of Event - Logic Inputs
Event Value 0101010101010101

Table 2 - Time and date of event - logic inputs

The Event Value is an 8, 12, 16, 24 or 32-bit word showing the status of the opto inputs, where the least significant bit (extreme right) corresponds to opto input 1. The same information is present if the event is extracted and viewed using a PC.

2.1.2 Change of State of one or more Output Relay Contacts

If one or more of the output relay contacts have changed state since the last time the protection algorithm ran, the new status is logged as an event. When this event is selected to be viewed on the LCD, three cells appear, as shown in Table 3:

Time and Date of Event - Output Contacts
Event Value 010101010101010101010

Table 3 - Time and date of event - output contacts

The Event Value is a 7, 11, 14, 15, 16, 22, 24 or 32-bit word showing the status of the output contacts, where the least significant bit (extreme right) corresponds to output contact 1. The same information is present if the event is extracted and viewed using a PC.

2.1.3 Relay Alarm Conditions

Any alarm conditions generated by the relays are logged as individual events. Table 4 shows examples of some of the alarm conditions and how they appear in the event list:

Alarm condition	Resulting event	
	Event text	**Event value**
Alarm Status 1 (Alarms 1 to 32) (32 bits)		
Not used		Bit positions 0 to 1 in 32-bit field
Setting Group Via Opto Invalid	SG-DDB Invalid	Bit position 2 in 32-bit field
This alarm is not operative because the CB Monitoring function is not available	CB Status Alarm	Bit position 3 in 32-bit field
RTD Thermal Alarm	RTD Thermal Alm	Bit position 4 in 32-bit field
RTD Open Circuit Failure	RTD Open Cct	Bit position 5 in 32-bit field
RTD Short Circuit Failure	RTD Short Cct	Bit position 6 in 32-bit field
RTD Data Inconsistency Error	RTD data error	Bit position 7 in 32-bit field
RTD Board Failure	RTD board fail	Bit position 8 in 32-bit field
Current Loop Input 1 Alarm	CL Input 1 Alarm	Bit position 9 in 32-bit field
Current Loop Input 2 Alarm	CL Input 2 Alarm	Bit position 10 in 32-bit field
Current Loop Input 3 Alarm	CL Input 3 Alarm	Bit position 11 in 32-bit field
Current Loop Input 4 Alarm	CL Input 4 Alarm	Bit position 12 in 32-bit field
Current Loop Input 1 Undercurrent Fail Alarm	CL1 I< Fail Alm	Bit position 13 in 32-bit field
Current Loop Input 2 Undercurrent Fail Alarm	CL2 I< Fail Alm	Bit position 14 in 32-bit field
Current Loop Input 3 Undercurrent Fail Alarm	CL3 I< Fail Alm	Bit position 15 in 32-bit field
Current Loop Input 4 Undercurrent Fail Alarm	CL4 I< Fail Alm	Bit position 16 in 32-bit field
Protection Disabled	Prot’n Disabled ON/OFF	Bit positions 17 in 32-bit field
Frequency Out of Range	Freq out of Range ON/OFF	Bit positions 18 in 32-bit field
Not used		Bit positions 19 to 21 in 32-bit field

Alarm condition	Resulting event	
	Event text	**Event value**
Current loop card input fail	CL Card I/P Fail	Bit positions 22 in 32-bit field
Current loop card output fail	CL Card O/P Fail	Bit positions 23 in 32-bit field
The current input configured in VCO>1 setting cell is not located at the same transformer terminal as the main VT.	VCO> 1 Config err	Bit positions 24 in 32-bit field
The current input configured in VCO>2 setting cell is not located at the same transformer terminal as the main VT.	VCO> 2 Config err	Bit positions 25 in 32-bit field
Not used		Bit positions 26 in 32-bit field
Current transformer supervision alarm	CT Fail Alarm	Bit position 27 in 32
Circuitry fail alarm	Cct Fail Alarm	Bit position 28 in 32
Voltage transformer supervision alarm	VT Fail Alarm	Bit position 29 in 32
Thermal pre-trip alarm	ThermalPretrp Alm	Bit position 30 in 32
Ageing acceleration factor alarm	FAA alarm	Bit position 31 in 32
Alarm Status 2 (Alarms 1 to 32) (32 bits)		
LOL alarm	LOL alarm	Bit position 0 in 32-bit field
CB Trip Fail Protection	Breaker Fail	Bit position 1 in 32-bit field
The ratio correction factor is out of range	Ct para mistmatch	Bit position 2 in 32-bit field
One current input is assigned to more than one terminal.	Ct Selection Alm	Bit position 3 in 32-bit field
Any of the single phase CTs is assigned at the same time to the high impedance REF and any other protection function such as earth fault current or circuit breaker failure.	SinglePha CT Alm	Bit position 4 in 32-bit field
Only one CT is left for the differential function.	Insuff No. of CT	Bit position 5 in 32-bit field
The CT stored status does not match the status after the power supply is re-established.	Disc CT invalid	Bit position 6 in 32-bit field
Scaling factor of HV low impedance REF is out of range	HV-LZREF sf OOR	Bit position 7 in 32-bit field
Scaling factor of LV low impedance REF is out of range	LV-LZREF sf OOR	Bit position 8 in 32-bit field
Scaling factor of TV low impedance REF is out of range	TV-LZREF sf OOR	Bit position 9 in 32-bit field
Scaling factor of autotransformer low impedance REF is out of range	AutoLZREF sf OOR	Bit position 10 in 32-bit field
Not used		Bit positions 11 to 20 in 32-bit field
W1 overfluxing element alarm	W1 V/Hz>1 Alarm	Bit position 21 in 32-bit field
W1 overfluxing element pretrip alarm	W1 V/Hz>2 PrTrp	Bit position 22 in 32-bit field
W2 overfluxing element alarm	W2 V/Hz>1 Alarm	Bit position 23 in 32-bit field
W2 overfluxing element pretrip alarm	W2 V/Hz>2 PrTrp	Bit position 24 in 32-bit field
Not used		Bit positions 25 to 26 in 32-bit field
Frequency Protection Alarm	Freq Prot Alm	Bit position 27 in 32-bit field
Through fault Alarm	Throu fault Alm	Bit position 28 in 32-bit field
unused		Bit positions 29 to 31 in 32-bit field
Alarm Status 3 (Alarms 1 to 32) (32 bits)		
Battery Fail	Battery Fail	Bit position 0 in 32-bit field

Alarm condition	Resulting event	
	Event text	Event value
Field Voltage Fail	Field Volt Fail	Bit position 1 in 32-bit field
unused		Bit position 2 in 32-bit field
Enrolled GOOSE IED absent alarm indication	Goose IED Absent	Bit position 3 in 32-bit field
Network Interface Card not fitted/failed alarm	NIC not fitted	Bit position 4 in 32-bit field
Network Interface Card not responding alarm	NIC no response	Bit position 5 in 32-bit field
Network Interface Card fatal error alarm indication	NIC fatal error	Bit position 6 in 32-bit field
Not used		Bit positions 7 to 9 in 32-bit field
Bad TCP/IP Configuration Alarm	Bad TCP/IP Cfg	Bit position 8 in 32-bit field
		Bit position 9 in 32-bit field
Network Interface Card link fail alarm indication	NIC link fail	Bit position 10 in 32-bit field
Main card/NIC software mismatch alarm indication	NIC software mismatch	Bit position 11 in 32-bit field
IP address conflict alarm indication	IP Addr Conflict	Bit position 12 in 32-bit field
Not used		Bit positions 13 to 16 in 32-bit field
Error when writing the settings from RAM to Flash memory	Back up Setting	Bit position 17 in 32-bit field
It is only available when DNP3 over Ethernet is in used.	Bad DNP Settings	Bit positions 18 to 31 in 32-bit field
Alarm Status 4 (Alarms 1 to 32) (32 bits)		
User alarm 1	User alarm 1	Bit position 0 in 32-bit field
User alarm 32	User alarm 32	Bit position 31 in 32-bit field

Table 4 - Relay alarm conditions

Table 4 shows the abbreviated description given to the various alarm conditions and a corresponding value between 0 and 31. This value is appended to each alarm event in a similar way to the input and output events described previously. It is used by the event extraction software, such as MiCOM S1 Studio, to identify the alarm and is therefore invisible if the event is viewed on the LCD. ON or OFF is shown after the description to signify whether the particular condition has become operated or has reset.

The User Alarms can be operated from an opto input or a control input using the PSL. They can be useful to give an alarm LED and message on the LCD and an alarm indication through the communications of an external condition, for example trip circuit supervision alarm or rotor earth fault alarm. Label the user alarm in the setting file in MiCOM S1 Studio to give a more meaningful description on the LCD.

2.1.4 Protection Element Starts and Trips

Any operation of protection elements, (either a start or a trip condition) is logged as an event record, consisting of a text string indicating the operated element and an event value. Again, this value is intended for use by the event extraction software, such as MiCOM S1 Studio, rather than for the user, and is therefore invisible when the event is viewed on the LCD.

2.1.5 General Events

Several events come under the heading of **General Events**. An example appears in Table 5.

Nature of event	Displayed text in event record	Displayed value
Level 1 password modified, either from user interface, front or rear port.	PW1 modified UI, F, R or R2	0 UI=6, F=11, R=16, R2=38

Table 5 - General events

A complete list of the General Events is given in the Relay Menu Database document, P64x/EN MD. This is a separate document, available for downloaded from our website.

2.1.6 Fault Records

Each time a fault record is generated, an event is also created. The event states that a fault record was generated, with a corresponding time stamp.

Further down the **VIEW RECORDS** column, select the **Select Fault** cell to view the actual fault record, which is selectable from up to 5 records. These records consist of, for example, fault flags, fault location, and fault measurements. The time stamp given in the fault record is more accurate than the corresponding stamp given in the event record as the event is logged some time after the actual fault record is generated.

The fault record is triggered from the **Fault REC. TRIG.** signal assigned in the default programmable scheme logic to relay 3, protection trip. The fault measurements in the fault record are given at the time of the protection start. The fault recorder does not stop recording until any start (DDB 832) or the any trip signals (DDB 626) resets to record all the protection flags during the fault.

The triggering signals are Trip Initial (DDB 891), Function Key 10 (DDB 361) and TF Recorder trig (DDB 1779). Never program a latching contact/signal to trigger the fault recorder as the fault record would not be generated until the contact/signal has reset.

2.1.7 Setting Changes

Changes to any setting in the relay are logged as an event. Two examples are shown in Table 6:

Type of setting change	Displayed text in event record	Displayed value
Control/Support Setting	C & S Changed	22
Group # Change	Group # Changed	#
Where # = 1 to 4		

Type of setting change	Displayed text in event record	Displayed value
Note *Control/Support settings are such as communications, measurement, CT/VT ratio settings, which are not duplicated in the four setting groups. When any of these settings are changed, the event record is created simultaneously. However, changes to protection or disturbance recorder settings only generate an event once the settings have been confirmed at the 'setting trap'.*		

Table 6 - Setting changes

2.2 Resetting of Event or Fault Records

To delete the event, fault or maintenance reports, use the **RECORD CONTROL** column.

2.3 Viewing Event Records using MiCOM S1 Studio Support Software

When the event records are extracted and viewed on a PC they look slightly different than when viewed on the LCD. The following shows an example of how various events appear when displayed using MiCOM S1 Studio:

Monday 08 January 2001 18:45:28.633 GMT V<1 Trip A/AB ON

Schneider Electric: MiCOM P643
Model Number: P643314B2A0020A
Address: 001 Column: 0F Row: 26
Event Type: Setting event
Event Value: 00000001000000000000000000000000

Monday 08 January 2001 18:45:28.634 GMT Output Contacts

Schneider Electric: MiCOM P643
Model Number: P643314B2A0020A
Address: 001 Column: 00 Row: 21
Event Type: Device output changed state
Event Value: 00000000001100

OFF 0	Output R1
OFF 1	Output R2
ON 2	R3 Any Trip
ON 3	R4 General Alarm
OFF 4	R5 CB Fail
OFF 5	R6 E/F Trip
OFF 6	R7 Volt Trip
OFF 7	R8 Freq Trip
OFF 8	R9 Diff Trip
OFF 9	Output R10
OFF 10	R11 NPS Trip
OFF 11	Output R12
OFF 12	Output R13
OFF 13	R14 V/Hz Trip

Monday 08 January 2001 18:45:28.633 GMT Voltage Prot Alm ON

Schneider Electric: MiCOM P643
Model Number: P643314B2A0020A
Address: 001 Column: 00 Row: 22

Event Type:	Alarm event
Event Value:	00001000000000000000000000000000

OFF 0	Battery Fail
OFF 1	Field Volt Fail
OFF 2	SG-opto Invalid
OFF 3	Prot'n Disabled
OFF 4	VT Fail Alarm
OFF 5	CT Fail Alarm
OFF 6	CB Fail Alarm
OFF 7	Not Used
OFF 8	Not Used
OFF 9	Not Used
OFF 10	Not Used
OFF 11	Not Used
OFF 12	Not Used
OFF 13	Fault Freq Lock
OFF 14	CB Status Alarm
OFF 15	Not Used
OFF 16	Not Used
OFF 17	Not Used
OFF 18	NPS Alarm
OFF 19	V/Hz Alarm
OFF 20	Field Fail Alarm
OFF 21	RTD Thermal Alm
OFF 22	RTD Open Cct
OFF 23	RTD short Cct
OFF 24	RTD Data Error
OFF 25	RTD Board Fail
OFF 26	Freq Prot Alm
ON 27	Voltage Prot Alm
OFF 28	User Alarm 1
OFF 29	User Alarm 2
OFF 30	User Alarm 3
OFF 31	User Alarm 4

As can be seen, the first line gives the description and time stamp for the event, while the additional information displayed below may be collapsed using the +/– symbol.

For further information regarding events and their specific meaning, refer to the *Relay Menu Database* document*, P64x/EN MD*. This is a standalone document not included in this manual.

2.4 Event Filtering

Event reporting can be disabled from all interfaces that support setting changes. The settings that control the various types of events are in the record control column. The effect of setting each to disabled is in Table 7:

Menu text	Default setting	Available settings
RECORD CONTROL		
Clear Events	No	No or Yes
Selecting Yes clears the existing event log and an event is generated indicating that the events have been erased.		
Clear Faults	No	No or Yes
Selecting Yes causes the existing fault records to be erased from the relay.		
Clear Maint.	No	No or Yes
Selecting Yes causes the existing maintenance records to be erased from the relay.		
Alarm Event	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for all alarms.		
Relay O/P Event	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any change in relay output contact state.		
Opto Input Event	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any change in logic input state.		
General Event	Enabled	Enabled or Disabled
Disabling this setting means that no General Events is generated. See event record sheet in the Relay Menu Database document, P64x/EN MD for list of general events.		
Fault Rec Event	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any fault that produces a fault record.		
Maint. Rec Event	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any maintenance records.		
Protection Event	Enabled	Enabled or Disabled
Disabling this setting means that no event is generated for any operation of the protection elements.		
Clear Disturbance Records	No	No or Yes
Selecting Yes causes the existing disturbance record to be erased from the memory.		
DDB 31 - 0	11111111111111111111111111111111	
32 bit setting to enable or disable the event recording for DDBs 0-31. For each bit 1 = event recording Enabled, 0 = event recording Disabled.		
DDB 2407 to 2016	11111111111111111111111111111111	
32 bit setting to enable or disable the event recording for DDBs 2407 to 2016. For each bit 1 = event recording Enabled, 0 = event recording Disabled. There are similar cells showing 32 bit binary strings for all DDBs from 0 to 2407. The first and last 32 bit binary strings only are shown here.		
Note *Some occurrences result in more than one type of event, for example a battery failure produces an alarm event and a maintenance record event.*		

Table 7 - Record control

If the Protection Event setting is Enabled, a further set of settings is revealed which allow the event generation by individual DDB signals to be enabled or disabled.

For further information on events and their specific meaning, see the *Relay Menu Database* document *P64x/EN MD*.

3 DISTURBANCE RECORDER

The integral disturbance recorder has an area of memory specifically set aside for record storage. The number of records that may be stored by the relay is dependent on the duration of the selected recording. The relay can typically store a minimum of 50 records, each of 1.5 seconds duration (8 analogue channels and 32 digital channels). However, VDEW relays have the same total record length but the VDEW protocol dictates that only 8 records can be extracted through the rear port. Disturbance records continue to be recorded until the available memory is exhausted, at which time the oldest records are overwritten to make space for the newest ones.

The recorder stores actual samples that are taken at a rate of 24 samples per cycle.

Each disturbance record consists of a maximum of 19/26/30 analog data channels for P642/P643/P645 with software versions 04. Also, 32 digital data channels are available. The relevant CT and VT ratios for the analog channels are also extracted to enable scaling to primary quantities. If a CT ratio is set to less than unity, the relay chooses a scaling factor of zero for the appropriate channel.

Table 8 shows the **DISTURBANCE RECORDER** menu column.

Menu text	**Default setting**	**Setting range**		**Step size**
		Min.	**Max.**	
DISTURB RECORDER				
Duration	1.5 s	0.1 s	10.5 s	0.01 s
Overall recording time setting.				
Trigger Position	33.3%	0	100%	0.1%
Trigger point setting as a percentage of the duration. For example, the default settings show that the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1 s post-fault recording times.				
Trigger Mode	Single	Single or Extended		
If set to Single and if a further trigger occurs while a recording is taking place, the recorder ignores the trigger. However, if this is set to Extended, the post-trigger timer is reset to zero, extending the recording time.				

P642	P643	P645	Default Setting
			VA
			VB
			VC
Analog. Channel 1	Analog. Channel 1	Analog. Channel 1	IA1
Analog. Channel 2	Analog. Channel 2	Analog. Channel 2	IB1
Analog. Channel 3	Analog. Channel 3	Analog. Channel 3	IC1
Analog. Channel 4	Analog. Channel 4	Analog. Channel 4	IN1
Analog. Channel 5	Analog. Channel 5	Analog. Channel 5	IA2
Analog. Channel 6	Analog. Channel 6	Analog. Channel 6	IB2
Analog. Channel 7	Analog. Channel 7	Analog. Channel 7	IC2
Analog. Channel 8	Analog. Channel 8	Analog. Channel 8	IN2
	Analog. Channel 9	Analog. Channel 9	IA3
	Analog. Channel 10	Analog. Channel 10	IB3
	Analog. Channel 11	Analog. Channel 11	IC3
	Analog. Channel 12	Analog. Channel 12	IN3
		Analog. Channel 13	IA4
		Analog. Channel 14	IB4
		Analog. Channel 15	IC4

Menu text	Default setting	Setting range		Step size
		Min.	Max.	
DISTURB RECORDER				
		Analog. Channel 16	IA5	
		Analog. Channel 17	IB5	
		Analog. Channel 18	IC5	
Analog. Channel 9	Analog. Channel 13	Analog. Channel 19	IA DIFF	
Analog. Channel 10	Analog. Channel 14	Analog. Channel 20	IB DIFF	
Analog. Channel 11	Analog. Channel 15	Analog. Channel 21	IC DIFF	
Analog. Channel 12	Analog. Channel 16	Analog. Channel 22	IA Bias	
Analog. Channel 13	Analog. Channel 17	Analog. Channel 23	IB Bias	
Analog. Channel 14	Analog. Channel 18	Analog. Channel 24	IC Bias	
Analog. Channel 15	Analog. Channel 19	Analog. Channel 25	LoZ REF HV Diff	
Analog. Channel 16	Analog. Channel 20	Analog. Channel 26	LoZ REF HV Bias	
Analog. Channel 17	Analog. Channel 21	Analog. Channel 27	LoZ REF LV Diff	
Analog. Channel 18	Analog. Channel 22	Analog. Channel 28	LoZ REF LV Bias	
	Analog. Channel 23	Analog. Channel 29	LoZ REF TV Diff	
	Analog. Channel 24	Analog. Channel 30	LoZ REF TV Bias	
			LoZ REF Auto Diff	
			LoZ REF Auto Bias	
			HighZ REF HV Op	
			HighZ REF LV Op	
			HighZ REF TV Op	
			HighZ REF Auto Op	
	Analog. Channel 25		VX	
Analog. Channel 19	Analog. Channel 26		Frequency	
			VAB	
			VBC	
Selects any available analog input to be assigned to this channel. The options are: VA, VB, VC, VX, IA1, IB1, IC1, IN1, IA2, IB2, IC2, IN2, IA3, IB3, IC3, IN3, IA4, IB4, IC4, IA5, IB5, IC5, IA Diff, IB Diff, IC Diff, IA Bias, IB bias, IC bias, LoZ REF HV Diff, LoZ REF HV Bias, LoZ REF LV Diff, LoZ REF LV Bias, LoZ REF TV Diff, LoZ REF TV Bias, LoZ REF Auto Diff, LoZ REF Auto Bias, HighZ REF HV Op, HighZ REF LV Op, HighZ REF TV Op, HighZ REF Auto Op, Frequency VAB and VBC depending on the model. ***Note*** *VAB and VBC are only available in P642.*				
Digital Inputs 1 to 32	Relays 1 to 12 and Optos 1 to 12	Any of 12 O/P Contacts or Any of 12 Opto Inputs or Internal Digital Signals		
The digital channels may be mapped to any of the opto isolated inputs or output contacts, in addition to several internal relay digital signals, such as protection starts and LEDs.				
Inputs 1 to 32 Trigger	No Trigger except Dedicated Trip Relay O/Ps which are set to Trigger L/H	No Trigger, Trigger L/H, Trigger H/L		
Any of the digital channels may be selected to trigger the disturbance recorder on either a Low-to-High (L/H) or a High-to-Low (H/L) transition.				

Table 8 - Disturbance recorder

The pre and post fault recording times are set by a combination of the **Duration** and **Trigger Position** cells. **Duration** sets the overall recording time and the **Trigger Position** sets the trigger point as a percentage of the duration. For example, the default settings show that the overall recording time is set to 1.5 s with the trigger point being at 33.3% of this, giving 0.5 s pre-fault and 1 s post-fault recording times.

If a further trigger occurs while a recording is taking place, the recorder ignores the trigger if the **Trigger Mode** is set to **Single**. However, if this is set to **Extended**, the post-trigger timer is reset to zero, extending the recording time.

As can be seen from the menu, each of the analog channels is selectable from the available analog inputs to the relay. The digital channels may be mapped to any of the opto isolated inputs or output contacts, in addition to several internal relay digital signals, such as protection starts and LEDs. The complete list of these signals may be found by viewing the available settings in the relay menu or using a setting file in MiCOM S1 Studio. Any of the digital channels may be selected to trigger the disturbance recorder on either a low-to-high or a high-to-low transition, using the **Input Trigger** cell. The default trigger settings are that any dedicated trip output contacts, such as relay 3, trigger the recorder.

It is not possible to view the disturbance records locally using the LCD; they must be extracted using suitable software such as MiCOM S1 Studio. This process is fully explained in the *SCADA Communications* chapter, *P64x/EN SC*.

4 MEASUREMENTS

The relay produces a variety of both directly measured and calculated power system quantities. These measurement values are updated every second and can be viewed in the **Measurements** columns (up to three) of the relay or using the MiCOM S1 Studio Measurement viewer. The P64x relay can measure and display these quantities:

- Phase Voltages and Currents
- Phase to Phase Voltage and Currents
- Sequence Voltages and Currents
- Power and Energy Quantities
- Rms. Voltages and Currents
- Peak, Fixed and Rolling Demand Values

There are also measured values from the protection functions, which are also displayed under the measurement columns of the menu; these are described in the section on the relevant protection function.

4.1 Measured Voltages and Currents

The relay produces both phase-to-ground and phase-to-phase voltage and current values. They are produced directly from the Discrete Fourier Transform (DFT) used by the relay protection functions and present both magnitude and phase angle measurement.

4.2 Sequence Voltages and Currents

Sequence quantities are produced by the relay from the measured Fourier values; these are displayed as magnitude and phase angle values.

4.3 Power and Energy Quantities

Using the measured voltages and currents the relay calculates the apparent, real and reactive power quantities. These are produced phase by phase. Three-phase values are based on the sum of the three individual phase values. The signing of the real and reactive power measurements can be controlled using the measurement mode setting. The four options are defined in Table 9.

Measurement mode	Parameter	Signing
0 (Default)	Export Power Import Power Lagging Vars Leading VArs	+ – + –
1	Export Power Import Power Lagging Vars Leading VArs	– + + –
2	Export Power Import Power Lagging Vars Leading VArs	+ – – +

Measurement mode	Parameter	Signing
3	Export Power Import Power Lagging Vars Leading VArs	– + – +

Table 9 - Measurement mode, parameters and signing

In addition to the measured power quantities, the relay calculates the power factor phase-by-phase, in addition to a three-phase power factor.

These power values are also used to increment the total real and reactive energy measurements. Separate energy measurements are maintained for the total exported and imported energy. The energy measurements are incremented up to maximum values of 1000 GWhr or 1000 GVARhr, at which point they reset to zero. It is also possible to reset these values using the menu or remote interfaces using the **Reset Demand** cell.

4.4 RMS Voltages and Currents

RMS phase voltage and current values are calculated by the relay using the sum of the samples squared over a cycle of sampled data.

4.5 Demand Values

The relay produces fixed, rolling and peak demand values. Using the reset demand menu cell it is possible to reset these quantities from the user interface or the remote communications.

4.5.1 Fixed Demand Values

The fixed demand value is the average value of a quantity over the specified interval; values are produced for each phase current and for three-phase real and reactive power. The fixed demand values displayed by the relay are those for the previous interval. The values are updated at the end of the fixed demand period.

4.5.2 Rolling Demand Values

The rolling demand values are similar to the fixed demand values, the difference being that a sliding window is used. The rolling demand window consists of several smaller sub-periods. The resolution of the sliding window is the sub-period length, with the displayed values updated at the end of each of the sub-periods.

4.5.3 Peak Demand Values

Peak demand values are produced for each phase current and the real and reactive power quantities. These display the maximum value of the measured quantity since the last reset of the demand values.

4.6 Settings

The settings shown in Table 10 (under the heading **MEASURE’T SETUP**) can be used to configure the relay measurement function.

Menu text	Default settings	Available settings
MEASURE’T SETUP		
Default Display	Description	Description/Plant Reference/ Frequency/Access Level/3Ph + N

Menu text	Default settings	Available settings
MEASURE’T SETUP		
		Current/3Ph + N Voltage /Power/ Date and Time
This setting can be used to select the default display from a range of options. It is also possible to view the other default displays while at the default level using the ☐☐and ☐keys. However, once the 15 minute timeout elapses the default display reverts to that selected by this setting.		
Local Values	Primary	Primary/Secondary
This setting controls whether measured values from the front panel user interface and the front courier port are displayed as primary or secondary quantities.		
Remote Values	Primary	Primary/Secondary
This setting controls whether measured values from the rear communication port are displayed as primary or secondary quantities.		
Measurement Ref.	VX (P642) VA (P643,5)	VA/VB/VC/IA/IB/IC
Using this setting the phase reference for all angular measurements by the relay can be selected.		
Measurement Mode	0	0 to 3 step 1
This setting is used to control the signing of the real and reactive power quantities. The signing convention used is defined in section *4.3 Power and Energy Quantities*.		

Table 10 - Measure’t setup

In the firmware, the fix demand period has been fixed to 15min, the rolling demand to 1min and the number of rolling demand sub-periods 15.

4.7 Measurement Display Quantities

The relay has three Measurement columns for viewing of measurement quantities. These can also be viewed with MiCOM S1 Studio and are shown in these tables.

Measurements 1	Table 11
Measurements 2 - P643 and P645	Table 12
Measurements 2 - P642	Table 13
Measurements 3	Table 14

4.7.1 Measurements 1

MEASUREMENTS 1			
	P642	P643	P645
IA-1 Magnitude	*	*	*
IA-1 Phase Angle	*	*	*
IB-1 Magnitude	*	*	*
IB-1 Phase Angle	*	*	*
IC-1 Magnitude	*	*	*
IC-1 Phase Angle	*	*	*
IA-2 Magnitude	*	*	*
IA-2 Phase Angle	*	*	*
IB-2 Magnitude	*	*	*
IB-2 Phase Angle	*	*	*
IC-2 Magnitude	*	*	*
IC-2 Phase Angle	*	*	*
IA-3 Magnitude		*	*

MEASUREMENTS 1			
	P642	**P643**	**P645**
IA-3 Phase Angle		*	*
IB-3 Magnitude		*	*
IB-3 Phase Angle		*	*
IC-3 Magnitude		*	*
IC-3 Phase Angle		*	*
IA-4 Magnitude			*
IA-4 Phase Angle			*
IB-4 Magnitude			*
IB-4 Phase Angle			*
IC-4 Magnitude			*
IC-4 Phase Angle			*
IA-5 Magnitude			*
IA-5 Phase Angle			*
IB-5 Magnitude			*
IB-5 Phase Angle			*
IC-5 Magnitude			*
IC-5 Phase Angle			*
IA-HV Magnitude	*	*	*
IA-HV Phase Ang	*	*	*
IB-HV Magnitude	*	*	*
IB-HV Phase Ang	*	*	*
IC-HV Magnitude	*	*	*
IC-HV Phase Ang	*	*	*
IA-LV Magnitude	*	*	*
IA-LV Phase Ang	*	*	*
IB-LV Magnitude	*	*	*
IB-LV Phase Ang	*	*	*
IC-LV Magnitude	*	*	*
IC-LV Phase Ang	*	*	*
IA-TV Magnitude		*	*
IA-TV Phase Ang		*	*
IB-TV Magnitude		*	*
IB-TV Phase Ang		*	*
IC-TV Magnitude		*	*
IC-TV Phase Ang		*	*
I0-1 Magnitude	*	*	*
I1-1 Magnitude	*	*	*
I2-1 Magnitude	*	*	*
IN-HV Mea Mag	*	*	*
IN-HV Mea Ang	*	*	*
IN-HV Deriv Mag	*	*	*
IN-HV Deriv Ang	*	*	*
I0-2 Magnitude	*	*	*

MEASUREMENTS 1			
	P642	**P643**	**P645**
I1-2 Magnitude	*	*	*
I2-2 Magnitude	*	*	*
IN-LV Mea Mag	*	*	*
IN-LV Mea Ang	*	*	*
IN-LV Deriv Mag	*	*	*
IN-LV Deriv Ang	*	*	*
I0-3 Magnitude		*	*
I1-3 Magnitude		*	*
I2-3 Magnitude		*	*
IN-TV Mea Mag		*	*
IN-TV Mea Ang		*	*
IN-TV Deriv Mag		*	*
IN-TV Deriv Ang		*	*
I0-4 Magnitude			*
I1-4 Magnitude			*
I2-4 Magnitude			*
I0-5 Magnitude			*
I1-5 Magnitude			*
I2-5 Magnitude			*
IA-HV RMS	*	*	*
IB-HV RMS	*	*	*
IC-HV RMS	*	*	*
IA-LV RMS	*	*	*
IB-LV RMS	*	*	*
IC-LV RMS	*	*	*
IA-TV RMS		*	*
IB-TV RMS		*	*
IC-TV RMS		*	*
VAN Magnitude		*	*
VAN Phase Angle		*	*
VBN Magnitude		*	*
VBN Phase Angle		*	*
VCN Magnitude		*	*
VCN Phase Angle		*	*
Vx Magnitude	*	*	*
Vx Phase Angle	*	*	*
V1 Magnitude	*	*	*
V2 Magnitude	*	*	*
V0 Magnitude		*	*
VN Derived Mag		*	*
VN Derived Angle		*	*
VAB Magnitude	*	*	*
VAB Phase Angle	*	*	*

MEASUREMENTS 1			
	P642	**P643**	**P645**
VBC Magnitude	*	*	*
VBC Phase Angle	*	*	*
VCA Magnitude	*	*	*
VCA Phase Angle	*	*	*
VAN RMS		*	*
VBN RMS		*	*
VCN RMS		*	*
Frequency	*	*	*

Table 11 - Measurements 1

4.7.2 Measurements 2 - P643 and P645

MEASUREMENTS 2		
	P643	**P645**
A Phase Watts	*	*
A Phase Watts	*	*
A Phase Watts	*	*
B Phase Watts	*	*
B Phase Watts	*	*
B Phase Watts	*	*
C Phase Watts	*	*
C Phase Watts	*	*
C Phase Watts	*	*
A Phase VArs	*	*
A Phase VArs	*	*
A Phase VArs	*	*
B Phase VArs	*	*
B Phase VArs	*	*
B Phase VArs	*	*
C Phase VArs	*	*
C Phase VArs	*	*
C Phase VArs	*	*
A Phase VA	*	*
A Phase VA	*	*
A Phase VA	*	*
B Phase VA	*	*
B Phase VA	*	*
B Phase VA	*	*
C Phase VA	*	*
C Phase VA	*	*
C Phase VA	*	*
3 Phase Watts	*	*
3 Phase Watts	*	*
3 Phase Watts	*	*

MEASUREMENTS 2		
	P643	**P645**
3 Phase VArs	*	*
3 Phase VArs	*	*
3 Phase VArs	*	*
3 Phase VA	*	*
3 Phase VA	*	*
3 Phase VA	*	*
3Ph Power Factor	*	*
APh Power Factor	*	*
BPh Power Factor	*	*
CPh Power Factor	*	*
3Ph WHours Fwd	*	*
3Ph WHours Rev	*	*
3Ph VArHours Fwd	*	*
3Ph VArHours Rev	*	*
3Ph W Fix Demand	*	*
3Ph VArs Fix Dem	*	*
3 Ph W Roll Dem	*	*
3Ph VArs RollDem	*	*
3Ph W Peak Dem	*	*
3Ph VAr Peak Dem	*	*
Reset Demand	No, Yes	No, Yes

Table 12 - Measurements 2 - P643 and P645

4.7.3 Measurements 2 - P642

MEASUREMENTS 2	
	P642
IA Differential	*
IB Differential	*
IC Differential	*
IA Bias	*
IB Bias	*
IC Bias	*
IA Diff 2H	*
IB Diff 2H	*
IC Diff 2H	*
IA Diff 5H	*
IB Diff 5H	*
IC Diff 5H	*
IREF HV LoZ Diff	*
IREF HV LoZ Bias	*
IREF LV LoZ Diff	*
IREF LV LoZ Bias	*
IREF Auto LoZ Diff	*

MEASUREMENTS 2	
	P642
IREF Auto LoZ Bias	*
IREF HV HighZ Op	*
IREF LV HighZ Op	*
IREF Auto HighZ Op	*
Thermal Overload	*
Hot Spot T	*
Top Oil T	*
Reset Thermal	*
Ambient T	*
TOL Pretrip left	*
LOL status	*
Reset LOL	*
Rate of LOL	*
LOL Aging Factor	*
Lres at designed	*
FAA,m	*
Lres at FAA,m	*
Volts/Hz	*
Volts/Hz W2	*
V/Hz W2 tPretrip	*
V/Hz W2 Thermal	*
Reset V/Hz W2	*
RTD 1 label	*
RTD 2 label	*
RTD 3 label	*
RTD 4 label	*
RTD 5 label	*
RTD 6 label	*
RTD 7 label	*
RTD 8 label	*
RTD 9 label	*
RTD 10 label	*
RTD Open Cct	*
RTD Short Cct	*
RTD Data Error	*
Reset RTD Flags	*
CLIO Input 1	*
CLIO Input 2	*
CLIO Input 3	*
CLIO Input 4	*

Table 13 - Measurements 2 - P642

4.7.4 Measurements 3

MEASUREMENTS 3		
	P643	**P645**
IA Differential	*	*
IB Differential	*	*
IC Differential	*	*
IA Bias	*	*
IB Bias	*	*
IC Bias	*	*
IA Diff 2H	*	*
IB Diff 2H	*	*
IC Diff 2H	*	*
IA Diff 5H	*	*
IB Diff 5H	*	*
IC Diff 5H	*	*
IREF HV LoZ Diff	*	*
IREF HV LoZ Bias	*	*
IREF LV LoZ Diff	*	*
IREF LV LoZ Bias	*	*
IREF TV LoZ Diff	*	*
IREF TV LoZ Bias	*	*
IREF Auto LoZ Diff	*	*
IREF Auto LoZ Bias	*	*
IREF HV HighZ Op	*	*
IREF LV HighZ Op	*	*
IREF TV HighZ Op	*	*
IREF Auto HighZ Op	*	*
Thermal Overload	*	*
Hot Spot T	*	*
Top Oil T	*	*
Reset Thermal	*	*
Ambient T	*	*
TOL Pretrip left	*	*
LOL status	*	*
Reset LOL	*	*
Rate of LOL	*	*
LOL Aging Factor	*	*
Lres at designed	*	*
FAA,m	*	*
Lres at FAA,m	*	*
Volts/Hz	*	*
Volts/Hz W1	*	*
V/Hz W1 tPretrip	*	*
V/Hz W1 Thermal	*	*
Reset V/Hz W1	*	*

MEASUREMENTS 3		
	P643	**P645**
Volts/Hz W2	*	*
V/Hz W2 tPretrip	*	*
V/Hz W2 Thermal	*	*
Reset V/Hz W2	*	*
RTD 1 label	*	*
RTD 2 label	*	*
RTD 3 label	*	*
RTD 4 label	*	*
RTD 5 label	*	*
RTD 6 label	*	*
RTD 7 label	*	*
RTD 8 label	*	*
RTD 9 label	*	*
RTD 10 label	*	*
RTD Open Cct	*	*
RTD Short Cct	*	*
RTD Data Error	*	*
Reset RTD Flags	*	*
CLIO Input 1	*	*
CLIO Input 2	*	*
CLIO Input 3	*	*
CLIO Input 4	*	*

Table 14 - Measurements 3

FIRMWARE DESIGN

CHAPTER NO 9

Date:	12/2013
Hardware Suffix:	J (P642) K (P643/P645)
Software Version:	04
Connection Diagrams:	10P642xx (xx = 1 to 10) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9)

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1 RELAY SYSTEM OVERVIEW

1.1 Hardware Overview

The relay hardware is made up of several modules from a standard range. Some modules are essential while others are optional depending on the user's requirements.

All modules are connected by a parallel data and address bus which allows the processor board to send and receive information to and from the other modules as required.

There is also a separate serial data bus for transferring sample data from the input module to the processor. See Figure 1.

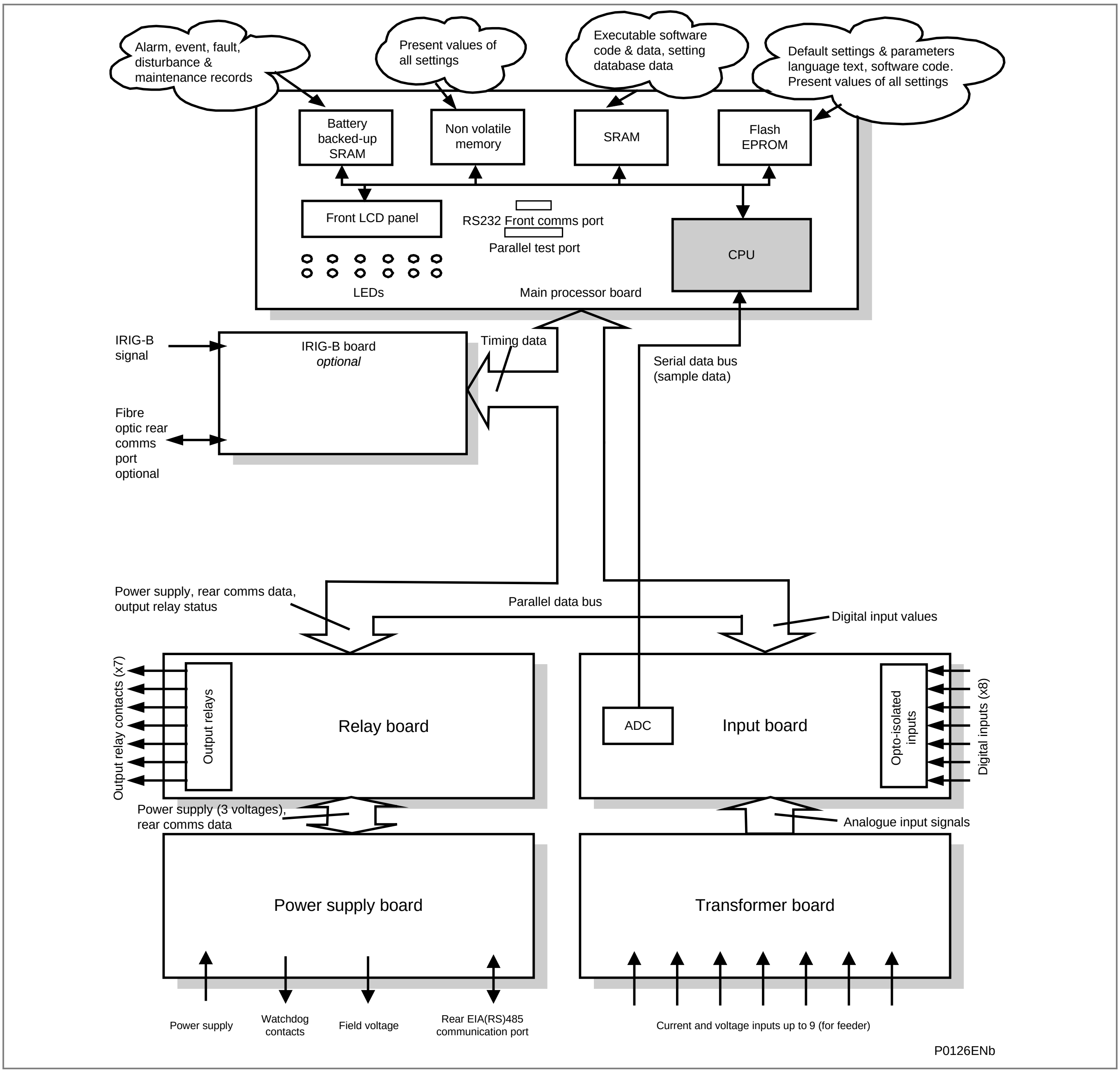

Alarm, event, fault, disturbance & maintenance records
Present values of all settings
Executable software code & data, setting database data
Default settings & parameters language text, software code. Present values of all settings
Battery backed-up SRAM
Non volatile memory
SRAM
Flash EPROM
Front LCD panel
RS232 Front comms port
Parallel test port
CPU
LEDs
Main processor board
IRIG-B signal
IRIG-B board
optional
Timing data
Serial data bus (sample data)
Fibre optic rear comms port optional
Power supply, rear comms data, output relay status
Parallel data bus
Digital input values
Output relay contacts (x7)
Output relays
Relay board
ADC
Input board
Opto-isolated inputs
Digital inputs (x8)
Power supply (3 voltages), rear comms data
Analogue input signals
Power supply board
Transformer board
Power supply
Watchdog contacts
Field voltage
Rear EIA(RS)485 communication port
Current and voltage inputs up to 9 (for feeder)
P0126ENb

Figure 1 - Relay modules

1.1.1 Processor Board

The processor board performs all calculations for the relay and controls the operation of all other modules in the relay. The processor board also contains and controls the user interfaces (LCD, LEDs, keypad and communication interfaces).

1.1.2 Input Module

The input module converts the data in the analog and digital input signals into a format suitable for processing by the processor board. The standard input module consists of two boards: a transformer board to provide electrical isolation and a main input board which provides analog to digital conversion and the isolated digital inputs.

1.1.3 Power Supply Module

The power supply module provides power to all of the other modules in the relay, at three different voltage levels. It also provides the EIA(RS)485 electrical connection for the rear communication port. The second board of the power supply module contains the relays that provide the output contacts.

1.1.4 Resistance Temperature Detectors (RTD) Board

This optional board can be used to process the signals from up to 10 Resistance Temperature Detectors (RTDs) to measure the winding and ambient temperatures.

1.1.5 IRIG-B Modulated or Un-modulated Board (Optional)

This board, which is optional, can be used where an IRIG-B signal is available to provide an accurate time reference for the relay. There is also an option on this board to specify a fiber optic or Ethernet rear communication port.

1.1.6 Second Rear Comms. Board

The optional second rear port is designed typically for dial-up modem access by protection engineers and operators, when the main port is reserved for SCADA traffic. Communication is through one of three physical links: K-BUS, EIA(RS)485 or EIA(RS)232. The port supports full local or remote protection and control access by MiCOM S1 Studio software. The second rear port is also available with an on board IRIG-B input.

1.1.7 Standard Ethernet Board

This optional board is required for IEC 61850 or DNP3 over Ethernet comms. It provides network connectivity through either copper or fiber media at rates of 10 Mb/s (copper only) or 100 Mb/s. There is also an option on this board to specify IRIG-B port (modulated or un-modulated). This board, the IRIG-B board described in section 1.1.5 and second rear comms. board described in section 1.1.6 are mutually exclusive as they all use slot A in the relay case.

1.2 Software Overview

The software for the relay can be split into four elements: the real-time operating system, the system services software, the platform software, and the protection and control software. These four elements are not distinguishable to the user, and are all processed by the same processor board.

1.2.1 Real-Time Operating System

The real-time operating system provides a framework for the different parts of the relay's software to operate in. The software is split into tasks. The real-time operating system schedules the processing of these tasks so they are carried out at the correct time and in the correct priority. The operating system also exchanges information between tasks in the form of messages.

1.2.2 System Services Software

The system services software provides the low-level control of the relay hardware. For example, the system services software controls the boot of the relay's software from the non-volatile flash memory at power-on, and provides driver software for the user interface through the LCD and keypad, and through the serial communication ports. The system services software provides an interface layer between the control of the relay's hardware and the rest of the relay software.

1.2.3 Platform Software

The platform software deals with the management of the relay settings, the user interfaces and logging of event, alarm, fault and maintenance records. All of the relay settings are stored in a database in the relay. This database is directly compatibility with Courier communications. For all other interfaces (such as the front panel keypad and LCD interface, MODBUS, IEC60870-5-103 and DNP3.0) the platform software converts the information from the database into the format required. The platform software notifies the protection and control software of all settings changes and logs data as specified by the protection and control software.

1.2.4 Protection and Control Software

The protection and control software performs the calculations for all of the protection algorithms of the relay. This includes digital signal processing such as Fourier filtering and ancillary tasks such as the disturbance recorder. The protection and control software interfaces with the platform software for settings changes and logging of records, and with the system services software for acquisition of sample data and access to output relays and digital opto-isolated inputs.

1.2.5 Disturbance Recorder

The analog values and logic signals are routed from the protection and control software to the disturbance recorder software. The platform software interfaces with the disturbance recorder to allow the stored records to be extracted.

2 HARDWARE MODULES

The relay is based on a modular hardware design where each module performs a separate function. This section describes the functional operation of the various hardware modules.

2.1 Processor Board

The relay is based around a TMS320VC33-150MHz (peak speed), floating-point, 32-bit Digital Signal Processor (DSP) operating at a clock frequency of half this speed. This processor performs all of the calculations for the relay, including the protection functions, control of the data communication and user interfaces including the operation of the LCD, keypad and LEDs.

There are two models of processor board, one with function keys for the P643 and P645, and one without function keys for the P642. The processor board is directly behind the relay’s front panel. This allows the LCD and LEDs and front panel communication ports to be mounted on the processor board. These ports are:

- The 9-pin D-connector for EIA(RS)232 serial communications used for MiCOM S1 Studio and Courier communications.
- The 25-pin D-connector relay test port for parallel communication.

All serial communication is handled using a Field Programmable Gate Array (FPGA).

The main processor board has:

- 2 MB SRAM for the working area. This is fast access (zero wait state) volatile memory used to temporarily store and execute the processor software.
- 2 MB flash ROM to store the software code, text, configuration data, default settings, and present settings.
- 4 MB battery-backed SRAM to store disturbance, event, fault and maintenance records.

2.2 Internal Communication Buses

The relay has two internal buses for the communication of data between different modules. The main bus is a parallel link that is part of a 64-way ribbon cable. The ribbon cable carries the data and address bus signals in addition to control signals and all power supply lines. Operation of the bus is driven by the main processor board that operates as a master while all other modules in the relay are slaves.

The second bus is a serial link that is used exclusively for communicating the digital sample values from the input module to the main processor board. The DSP has a built-in serial port that is used to read the sample data from the serial bus. The serial bus is also carried on the 64-way ribbon cable.

2.3 Input Module

The input module provides the interface between the relay processor board(s) and the analog and digital signals coming into the relay. The input module consists of the main input board and the transformer board.

2.3.1 Transformer Board

As shown in Figure 2, the transformer board holds up to two Voltage Transformers (VTs) and up to nine Current Transformers (CTs). The auxiliary transformer board adds up to four more CTs. The current inputs accept either 1 A or 5 A nominal current (menu and wiring options) and the voltage inputs can be specified for either 110 V nominal voltage (order option). The transformers are used both to step down the currents and voltages to levels appropriate to the relay’s electronic circuitry and to provide effective isolation between the relay and the power system. The connection arrangements of both the current and voltage transformer secondaries provide differential input signals to the main input board to reduce noise.

P642	1 VT, 8 CTs or 2 VTs, 8CTs
P643	2 VTs, 3 CTs or 2 VTs, 9 CTs
P645	2 VTs, 9 CTs

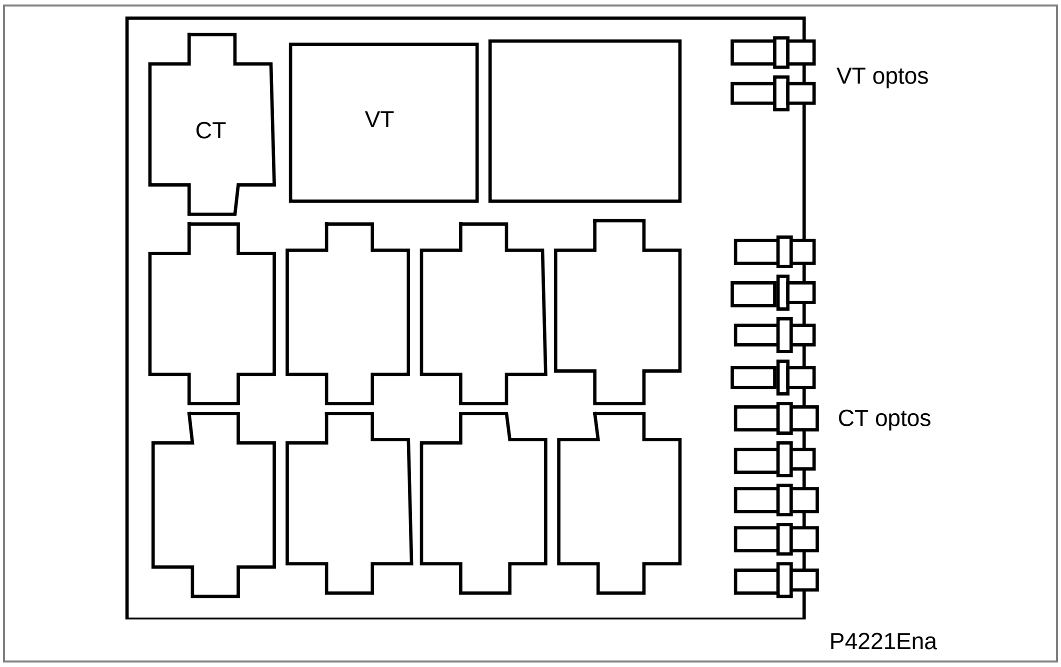


Figure 2 - Transformer board

2.3.2 Input Board

The main input board is shown as a block diagram in Figure 3. It provides the circuitry for the digital input signals and the analog-to-digital (A-D) conversion for the analog signals. It takes the differential analog signals from the CTs and VTs on the transformer board(s), converts these to digital samples and transmits the samples to the main processor board through the serial data bus. On the input board, the analog signals pass through an anti-alias filter then are multiplexed into a single A-D converter. The A-D converter provides 16-bit resolution and a serial data stream output. The digital input signals are opto isolated on this board to prevent excessive voltages on these inputs causing damage to the relay's internal circuitry.

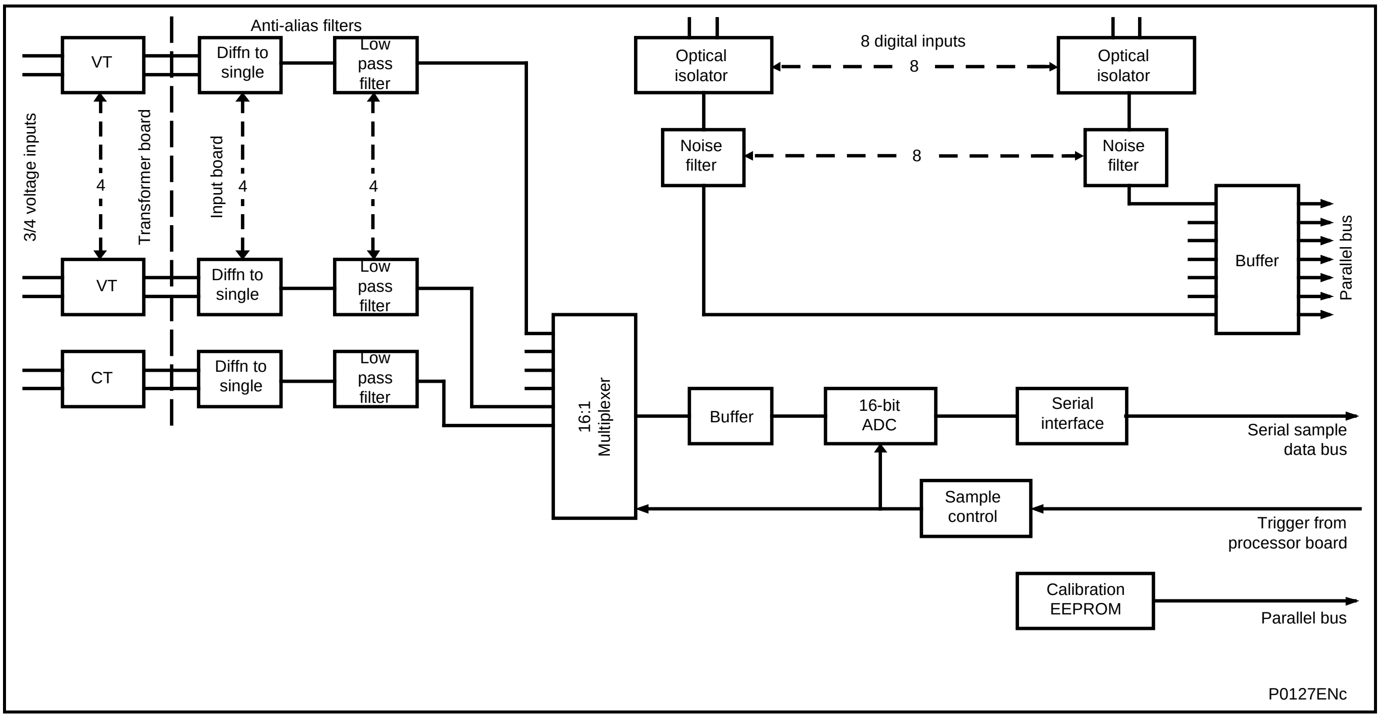

Anti-alias filters
VT
VT
CT
3/4 voltage inputs
Transformer board
Input board
Diffn to single
Diffn to single
Diffn to single
Low pass filter
Low pass filter
Low pass filter
4
4
4
16:1 Multiplexer
Optical isolator
Optical isolator
8 digital inputs
8
Noise filter
Noise filter
8
Buffer
Parallel bus
Buffer
16-bit ADC
Serial interface
Serial sample data bus
Sample control
Trigger from processor board
Calibration EEPROM
Parallel bus
P0127ENc

Figure 3 - Main input board

The signal multiplexing allows 16 analog channels to be sampled with up to nine current inputs and two voltage inputs. The three spare channels are used to sample three different reference voltages for continually checking the multiplexer operation and the A-D converter accuracy. The sample rate is kept at 24 samples per cycle of the power waveform by a logic control circuit driven by the frequency tracking function on the main processor board. The calibration non-volatile memory holds the calibration coefficients that are used by the processor board to correct for any amplitude or phase error introduced by the transformers and analog circuitry.

The other function of the input board is to read the signals on the digital inputs and send them through the parallel data bus to the processor board. The input board holds 8 optical isolators for connecting up to eight digital input signals. Opto-isolators are used with digital signals for the same reason as transformers are used with analog signals: to isolate the relay’s electronics from the power system environment. A 48 V ‘field voltage’ supply at the back of the relay is used to drive the digital opto-inputs. The input board has hardware filters to remove noise from the digital signals. The digital signals are then buffered so they can be read on the parallel data bus. Depending on the relay model, more than eight digital input signals can be accepted by the relay. This is done using an additional opto-board that contains the same provision for eight isolated digital inputs as the main input board, but does not contain any of the circuits for analog signals which are provided on the main input board.

2.3.3 Universal Opto Isolated Logic Inputs

The P64x series relays have universal opto-isolated logic inputs that can be programmed for the nominal battery voltage of the circuit of which they are a part. This allows different voltages for different circuits such as signaling and tripping. They can also be programmed as Standard 60% - 80% or 50% - 70% to satisfy different operating constraints.

Threshold levels are shown in Table 1:

Nominal battery voltage (Vdc)	Standard 60% - 80%		50% - 70%	
	No operation (Logic 0) Vdc	Operation (Logic 1) Vdc	No operation (Logic 0) Vdc	Operation (Logic 1) Vdc
24/27	<16.2	>19.2	<12.0	>16.8
30/34	<20.4	>24.0	<15.0	>21.0
48/54	<32.4	>38.4	<24.0	>33.6
110/125	<75.0	>88.0	<55.0	>77.0
220/250	<150.0	>176.0	<110	>154

Table 1 - Threshold Levels

This lower value eliminates fleeting pick-ups that may occur during a battery earth fault, when stray capacitance may present up to 50% of battery voltage across an input.

Each input also has selectable filtering. This allows a pre-set ½ cycle filter to be used to prevent induced noise on the wiring. However, although the ½ cycle filter is secure it can be slow, particularly for intertripping. If the ½ cycle filter is switched off to improve speed, double pole switching or screened twisted cable may be needed on the input to reduce ac noise.

2.4 Power Supply Module (including Output Relays)

The power supply module contains two boards, one for the power supply unit and the other for the output relays. The power supply board also contains the input and output hardware for the rear communication port which provides an EIA(RS)485 communication interface.

2.4.1 Power Supply Board (including EIA(RS)485 Communication Interface)

One of three different configurations of the power supply board can be fitted to the relay. This will be specified at the time of order and depends on the nature of the supply voltage that will be connected to the relay. The options are shown in Table 2.

Nominal dc range	Nominal ac range
24 to 48 V	DC only
48 to 110 V	40 to 100 Vrms
110 to 250 V	100 to 240 Vrms

Table 2 - Power supply options

The output from all versions of the power supply module are used to provide isolated power supply rails to all of the other modules in the relay. Three voltage levels are used in the relay: 5.1 V for all of the digital circuits, ±16 V for the analog electronics such as on the input board, and 22 V for driving the output relay coils and the RTD board if fitted. All power supply voltages including the 0 V earth line are distributed around the relay through the 64-way ribbon cable. The power supply board also provides the 48 V field voltage. This is brought out to terminals on the back of the relay so that it can be used to drive the optically-isolated digital inputs.

The two other functions provided by the power supply board are the EIA(RS)485 communications interface and the watchdog contacts for the relay. The EIA(RS)485 interface is used with the relay’s rear communication port to provide communication using one of either Courier, MODBUS, IEC60870-5-103, or DNP3.0 protocols. The EIA(RS)485 hardware supports half-duplex communication and provides optical isolation of the serial data that is transmitted and received. All internal communication of data from the power supply board is through the output relay board connected to the parallel bus.

The watchdog facility has two output relay contacts, one normally open and one normally closed. These are driven by the main processor board and indicate that the relay is in a healthy state.

The power supply board incorporates inrush current limiting. This limits the peak inrush current, during energization, to approximately 10 A.

2.4.2 Output Relay Board

The output relay board has eight relays, six normally open contacts and two changeover contacts.

The relays are driven from the 22 V power supply line. The relays' state is written to or read from using the parallel data bus. Depending on the relay model, more output contacts can be provided by using up to three extra relay boards. Each additional relay board provides a further four or eight output relays.

2.4.3 High Break Relay Board

The 'high break' output relay board has four normally open output contacts. It is optional in the P642, 3 and 5. The P642 can have a maximum of one board and the P643 and P645 can have up to two boards.

This board uses a hybrid of MOSFET Solid State Devices (SSD) in parallel with high capacity relay output contacts. The MOSFET has a varistor across it to provide protection which is required when switching off inductive loads because the stored energy in the inductor causes a reverse high voltage which could damage the MOSFET.

When there is a control input command to operate an output contact, the miniature relay is operated at the same time as the SSD. The miniature relay contact closes in nominally 3.5 ms and is used to carry the continuous load current; the SSD operates in <0.2 ms and is switched off after 7.5 ms. When the control input resets to open the contacts, the SSD is again turned on for 7.5 ms. The miniature relay resets in nominally 3.5 ms before the SSD so the SSD is used to break the load. The SSD absorbs the energy when breaking inductive loads and so limits the resulting voltage surge. This contact arrangement is for switching dc circuits only. As the SSD comes on very fast (<0.2 ms) these high break output contacts have the added advantage of being very fast operating. See Figure 4:

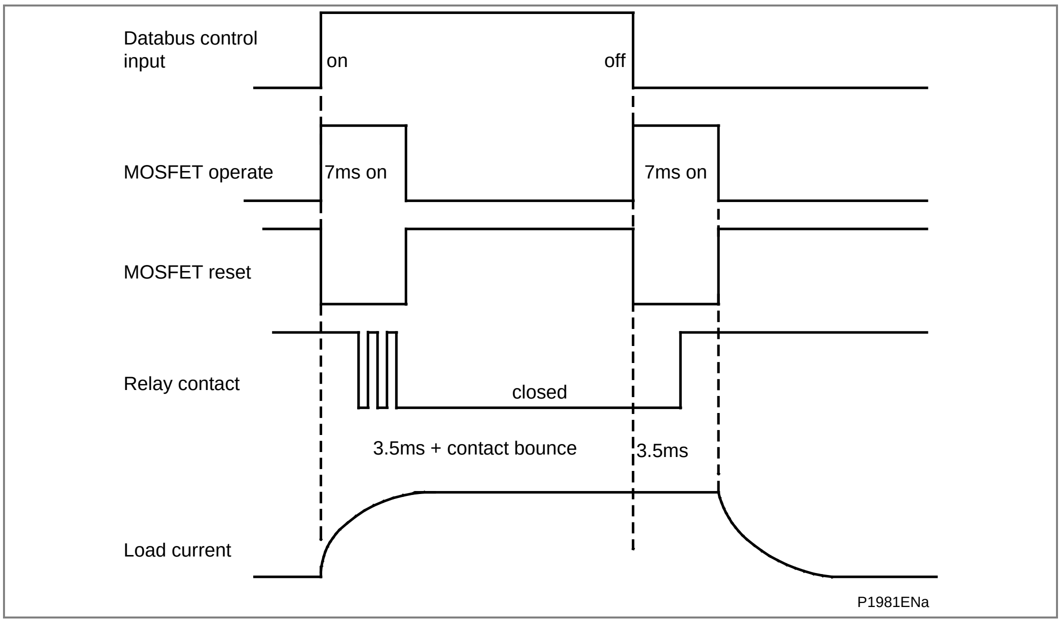


Figure 4 - High break contact operation

2.4.3.1 High Break Contact Applications

1. Efficient Scheme Engineering

   In traditional hardwired scheme designs, high break capability could only be achieved using external electromechanical trip relays. External MVAJ tripping relays can be used or the new high break contacts inside MiCOM relays can be used, reducing panel space.

2. Accessibility of CB Auxiliary Contacts

   Common practice is to use circuit breaker 52a (CB Closed) auxiliary contacts to break the trip coil current on breaker opening, easing the duty on the protection contacts. In cases such as operation of disconnectors, or retrofitting, 52a contacts may be unavailable or unreliable. High break contacts can be used to break the trip coil current in these applications.

3. Breaker Fail

   The technique to use 52a contacts in trip circuits was described above. However, in the event of failure of the local circuit breaker (stuck breaker), or defective auxiliary contacts (stuck contacts), the 52a contact action is incorrect. The interrupting duty at the local breaker then falls on the relay output contacts which may not be rated to perform this duty. MiCOM high break contacts will avoid the risk of burnt relay contacts.

4. Initiation of Teleprotection

   The MiCOM high break contacts also offer fast making, which can provide faster tripping. Also fast keying of teleprotection is a benefit. Fast keying bypasses the usual contact operation time so that permissive, blocking and intertrip commands can be routed faster.

2.4.4 Input/Output (4 + 4) Relay Board

The input/output relay board has four isolated digital inputs and four output relays. Two of the relays have normally open contacts and two have changeover contacts. The output relays are driven from the 22 V power supply line. The relays’ state is written to or read from using the parallel data bus.

This board is an option on the P642, giving 12 opto inputs and 12 output relay contacts.

2.5 Resistance Temperature Detector (RTD) Board

The RTD (Resistance Temperature Detector) board is an order option. It is used to monitor the temperature readings from up to ten PT100 RTDs that are each connected using a 3-wire connection. The board is powered from the 22 V power rail that is used to drive the output relays. The RTD board includes two redundant channels that are connected to high stability resistors to provide reference readings. These are used to check the operation of the RTD board. The temperature data is read by the processor through the parallel data bus, and is used to provide thermal protection of the transformer windings.

2.6 IRIG-B Board Modulated or Un-modulated Board (Optional)

The IRIG-B board is an order option that can be fitted to provide an accurate timing reference for the relay. This can be used wherever an IRIG-B signal is available. The IRIG-B signal is connected to the board with a BNC connector on the back of the relay. The timing information is used to synchronize the relay’s internal real-time clock to an accuracy of 1 ms. The internal clock is then used for the time tagging of the event, fault maintenance and disturbance records. The IRIG-B board can also be specified with a fiber optic or Ethernet rear communication port.

2.7 Second Rear Communications Board

For relays with Courier, MODBUS, IEC60870-5-103 or DNP3.0 protocol on the first rear communications port there is the hardware option of a second rear communications port, which runs the Courier language. This can be used over one of three physical links: twisted pair K-BUS (non-polarity sensitive), twisted pair EIA(RS)485 (connection polarity sensitive) or EIA(RS)232.

The second rear comms. board, Ethernet and IRIG-B boards are mutually exclusive since they use the same hardware slot. For this reason two versions of second rear comms. and Ethernet boards are available; one with an IRIG-B input and one without. The second rear comms. board is shown in Figure 5.

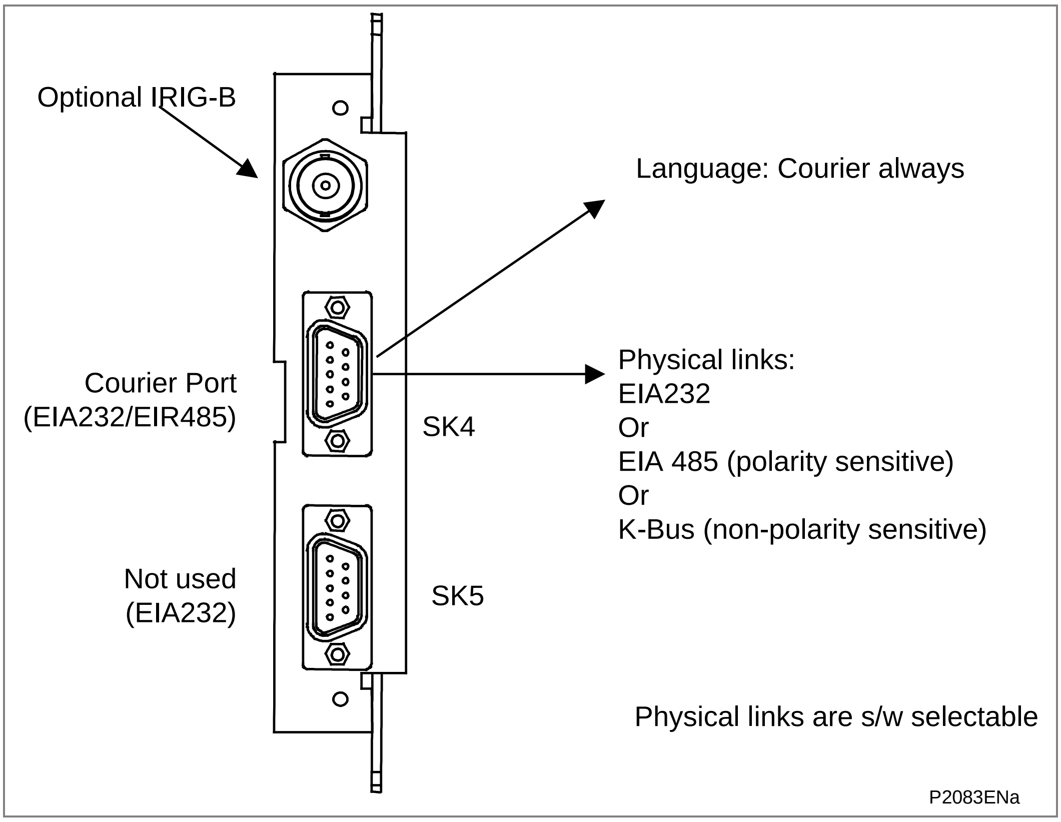

Optional IRIG-B
Language: Courier always
Courier Port
(EIA232/EIR485)
SK4
Physical links:
EIA232
Or
EIA 485 (polarity sensitive)
Or
K-Bus (non-polarity sensitive)
Not used
(EIA232)
SK5
Physical links are s/w selectable
P2083ENa

Figure 5 - Second rear comms. Port

2.8 Standard Ethernet Board (Optional)

The optional Ethernet board (ZN0049) is required for IEC 61850 or DNP3 over Ethernet comms. These variants support IEC 61850:

- 100 Mbits/s Fiber Optic + 10/100 Mbits/s Copper
- 100 Mbits/s Fiber Optic + 10/100 Mbits/s Copper + modulated IRIG-B
- 100 Mbits/s Fiber Optic + 10/100 Mbits/s Copper + un-modulated IRIG-B

This board is fitted into Slot A of the relay, which is the optional communications slot. Each Ethernet board has a unique MAC address used for Ethernet communications. The MAC address is printed on the rear of the board, next to the Ethernet sockets.

The 100 Mbits/s Fiber Optic ports use ST® type connectors and are suitable for 1300 nm multi-mode fiber type.

Copper ports use RJ45 type connectors. When using copper Ethernet, it is important to use Shielded Twisted Pair (STP) or Foil Twisted Pair (FTP) cables, to shield the IEC 61850 communications against electromagnetic interference. The RJ45 connector at each end of the cable must be shielded, and the cable shield must be connected to this RJ45 connector shield, so that the shield is grounded to the relay case. Both the cable and the RJ45 connector at each end of the cable must be Category 5 minimum, as specified by the IEC 61850 standard. It is recommended that each copper Ethernet cable is limited to a maximum length of 3 m and confined to one bay or cubicle.

When using IEC 61850 communications through the Ethernet board, the rear EIA(RS)485 and front EIA(RS)232 ports are also available for simultaneous use, both using the Courier protocol. The Ethernet board is shown in Figure 6.

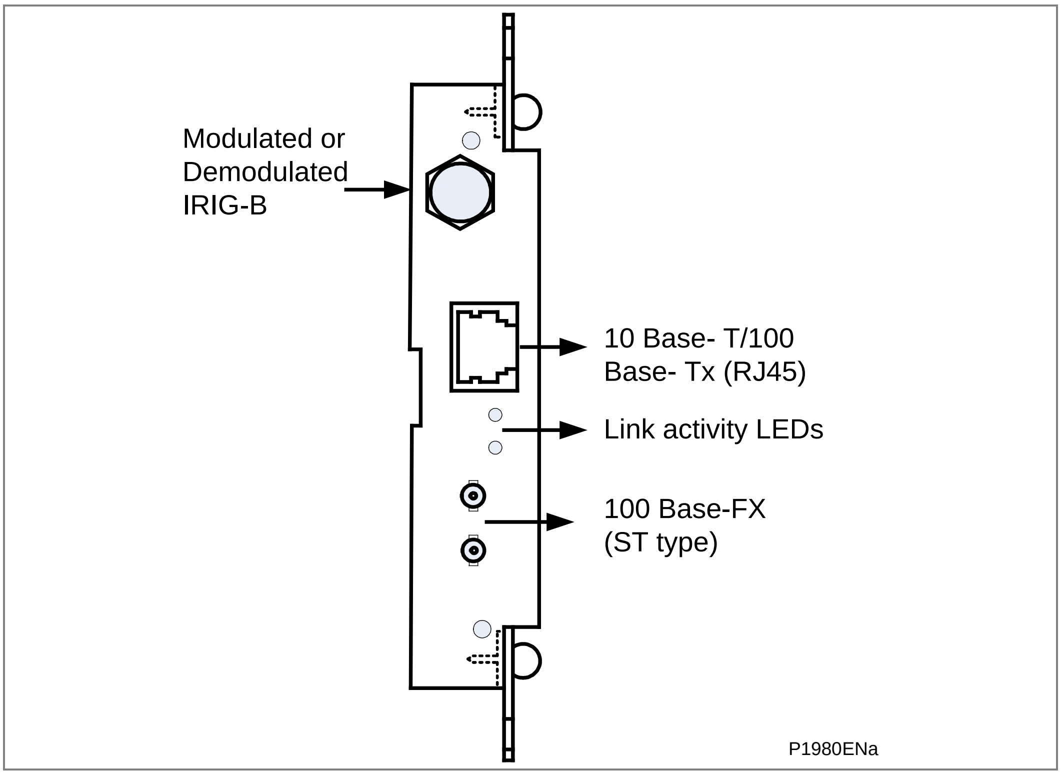


Figure 6 - Ethernet board (optional)

2.9 Current Loop Input Output (CLIO) Board

The Current Loop Input Output (CLIO) board is an order option. The CLIO board is powered from the 22 V power rail that is used to drive the output relays.

Four analog (or current loop) inputs are provided for transducers with ranges of 0 to 1 mA, 0 to 10 mA, 0 to 20 mA or 4 to 20 mA. The input current data is read by the processor through the parallel data bus, and is used to provide measurements from various transducers such as vibration monitors, tachometers and pressure transducers.

For each of the four current loop inputs there are two separate input circuits, 0 to 1 mA and 0 to 20 mA. The latter is also used for 0 to 10 mA and 4 to 20 mA transducer inputs. The anti-alias filters have a nominal cut-off frequency (3 dB point) of 23 Hz to reduce power system interference from the incoming signals. Four analog current outputs are provided with ranges of 0 to 1 mA, 0 to 10 mA, 0 to 20 mA or 4 to 20 mA which can alleviate the need for separate transducers. These may be used to feed standard moving coil ammeters for analog indication of certain measured quantities or into a SCADA using an existing analog RTU.

Each of the four current loop outputs provides one 0 to 1 mA output, one 0 to 20 mA output and one common return. Suitable software scaling of the value written to the board allows the 0 to 20 mA output to also provide 0 to 10 mA and 4 to 20 mA. Screened leads are recommended for use on the current loop output circuits.

The refresh interval for the outputs is nominally 50 ms. Any measurements that do not fit this timing are updated once every second.

All external connections to the current loop I/O board are made using the same 15-way light duty I/O connector SL3.5/15/90F used on the RTD board. Two such connectors are used, one for the current loop outputs and one for the current loop inputs.

The I/O connectors accommodate wire sizes in the range 1/0.85 mm (0.57 mm^2) to 1/1.38 mm (1.5 mm^2) and their multiple conductor equivalents. The use of screened cable is recommended. The screen terminations should be connected to the case earth of the relay.

Basic Insulation (300 V) is provided between analog inputs or outputs and earth, and between analog inputs and outputs. However, there is no insulation between one input and another or one output and another.

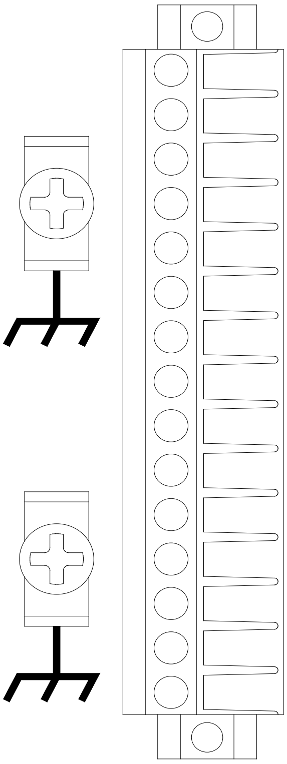
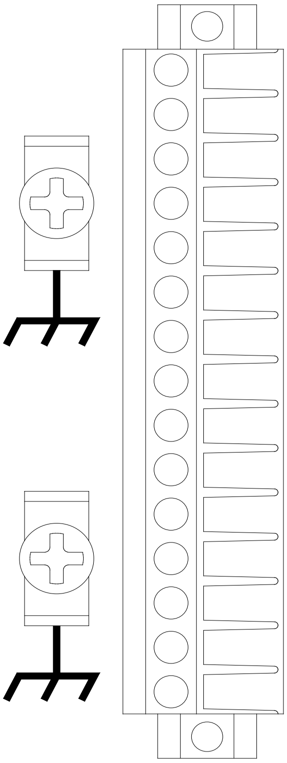
Connection	IO blocks	Connection
Outputs Screen channel 1 Screen channel 2 Screen channel 3 Screen channel 4		0 - 10/0 - 20/4 – 20 mA channel 1 0 – 1 mA channel 1 Common return channel 1 0 - 10/0 - 20/4 – 20 mA channel 2 0 – 1 mA channel 2 Common return channel 2 0 - 10/0 - 20/4 – 20 mA channel 3 0 – 1 mA channel 3 Common return channel 3 0 - 10/0 - 20/4 – 20 mA channel 4 0 – 1 mA channel 4 Common return channel 4
Inputs Screen channel 1 Screen channel 2 Screen channel 3 Screen channel 4		0 - 10/0 - 20/4 – 20 mA channel 1 0 – 1 mA channel 1 Common channel 1 0 - 10/0 - 20/4 – 20 mA channel 2 0 – 1 mA channel 2 Common channel 2 0 - 10/0 - 20/4 – 20 mA channel 3 0 – 1 mA channel 3 Common channel 3 0 - 10/0 - 20/4 – 20 mA channel 4 0 – 1 mA channel 4 Common channel 4

Table 3 - Current Loop Input Output (CLIO) board

2.10 Mechanical Layout

The relay case is pre-finished steel with a conductive covering of aluminum and zinc. This provides good earthing at all joints with a low impedance path to earth that is essential for shielding from external noise. The boards and modules use multi-point grounding (earthing) to improve immunity to external noise and minimize the effect of circuit noise. Ground planes are used on boards to reduce impedance paths and spring clips are used to ground the module metalwork.

Heavy duty terminal blocks are used at the rear of the relay for the current and voltage signal connections. Medium duty terminal blocks are used for the digital logic input signals, output relay contacts, power supply and rear communication port. A BNC connector is used for the optional IRIG-B signal. 9-pin and 25-pin female D-connectors are used at the front of the relay for data communication.

Inside the relay the boards plug into the connector blocks at the rear, and can be removed from the front of the relay only. The connector blocks to the relay’s CT inputs have internal shorting links inside the relay. These automatically short the current transformer circuits before they are broken when the board is removed.

The front panel consists of a membrane keypad with tactile dome keys, an LCD and 12 LEDs mounted on an aluminum backing plate.

3 RELAY SOFTWARE

The relay software was introduced in the overview of the relay at the start of this chapter. The software can be considered to be made up of these sections:

- The real-time operating system
- The system services software
- The platform software
- The protection and control software

This section describes in detail the ***platform software*** and the ***protection and control software***, which between them control the functional behavior of the relay. Figure 7 shows the structure of the relay software.

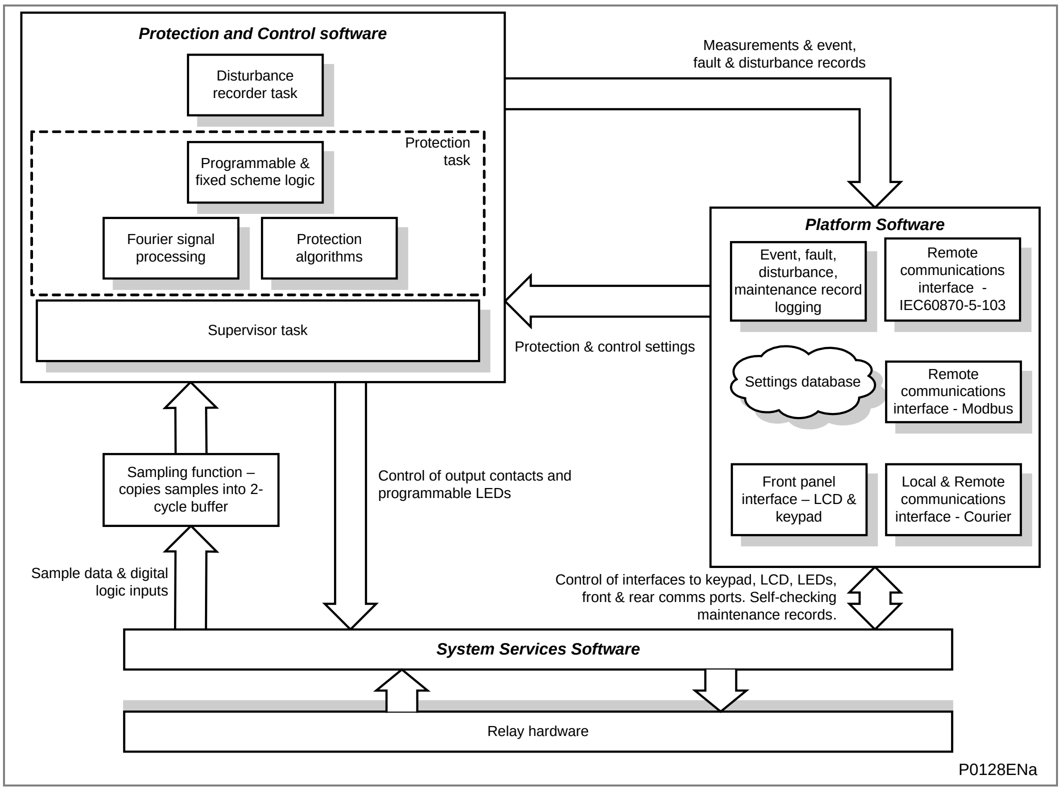

Protection and Control software
Disturbance recorder task
Protection task
Programmable & fixed scheme logic
Fourier signal processing
Protection algorithms
Supervisor task
Measurements & event, fault & disturbance records
Platform Software
Event, fault, disturbance, maintenance record logging
Remote communications interface - IEC60870-5-103
Protection & control settings
Settings database
Remote communications interface - Modbus
Front panel interface – LCD & keypad
Local & Remote communications interface - Courier
Sampling function – copies samples into 2-cycle buffer
Control of output contacts and programmable LEDs
Sample data & digital logic inputs
Control of interfaces to keypad, LCD, LEDs, front & rear comms ports. Self-checking maintenance records.
System Services Software
Relay hardware
P0128ENa

Figure 7 - Relay software structure

3.1 Real-Time Operating System

The software is split into tasks; the real-time operating system is used to schedule the processing of the tasks to ensure that they are processed in the time available and in the desired order of priority. The operating system is also responsible in part for controlling the communication between the software tasks through the use of operating system messages.

3.2 System Services Software

As shown in Figure 7, the system services software provides the interface between the relay's hardware and the higher-level functionality of the platform software and the protection and control software. For example, the system services software provides drivers for items such as the LCD display, the keypad and the remote communication ports, and controls the boot of the processor and downloading of the processor code into SRAM from non-volatile flash EPROM at power up.

3.3 Platform Software

The platform software has these main functions:

- To control the logging of all records that are generated by the protection software, including alarms and event, fault, disturbance and maintenance records.
- To store and maintain a database of all of the relay's settings in non-volatile memory.
- To provide the internal interface between the settings database and each of the relay's user interfaces. These interfaces are the front panel interface and the front and rear communication ports, using whichever communication protocol has been specified (Courier, MODBUS, IEC60870-5-103 and DNP3.0).

3.3.1 Record Logging

The logging function is provided to store all alarms, events, faults and maintenance records. The records for all of these incidents are logged in battery backed-up SRAM to provide a non-volatile log of what has happened. The relay maintains four logs: one each for up to 32 alarms, 512 event records, 5 fault records and 5 maintenance records. The logs are maintained so that the oldest record is overwritten with the newest record. The logging function can be initiated from the protection software or the platform software.

The logging function can be initiated from the protection software or the platform software is responsible for logging of a maintenance record in the event of a relay failure. This includes errors that have been detected by the platform software itself or error that are detected by either the system services or the protection software functions. See also the section on Self-Testing and Diagnostics later in this section.

3.3.2 Settings Database

The settings database contains all of the settings and data for the relay, including the protection, disturbance recorder and control and support settings. The settings are maintained in non-volatile memory. The platform software's management of the settings database includes the responsibility of ensuring that only one user interface modifies the settings of the database at any one time. This feature is employed to avoid confusion between different parts of the software during a setting change. For changes to protection settings and disturbance recorder settings, the platform software operates a 'scratchpad' in SRAM memory. This allows a number of setting changes to be made in any order but applied to the protection elements, disturbance recorder and saved in the database in non-volatile memory, at the same time. If a setting change affects the protection and control task, the database advises it of the new values.

3.3.3 Database Interface

The other function of the platform software is to implement the relay's internal interface between the database and each of the relay's user interfaces. The database of settings and measurements must be accessible from all of the relay's user interfaces to allow read and modify operations. The platform software presents the data in the appropriate format for each user interface.

3.4 Protection and Control Software

The protection and control software task processes all of the protection elements and measurement functions of the relay. It has to communicate with both the system services software and the platform software, and organize its own operations. The protection software has the highest priority of any of the software tasks in the relay, to provide the fastest possible protection response. The protection and control software has a supervisor task that controls the start-up of the task and deals with the exchange of messages between the task and the platform software.

3.4.1 Overview - Protection and Control Scheduling

After initialization at start-up, the protection and control task waits until there are enough samples to process. The sampling function is called by the system services software and takes each set of new samples from the input module and stores them in a two-cycle buffer. The protection and control software resumes execution when the number of unprocessed samples in the buffer reaches a certain number. Samples are taken 24 times every power cycle. Every 6 samples the protection task is executed (4 times per cycle). The protection elements are split into groups so that different elements are processed each time, and every element is processed at least once per cycle. The protection and control software is suspended again when all of its processing on a set of samples is complete. This allows operations by other software tasks to take place.

3.4.2 Signal Processing

The sampling function filters the digital input signals from the opto-isolators and tracks the frequency of the analog signals. The digital inputs are checked against their previous value over a period of half a cycle. Therefore a change in the state of one of the inputs must be maintained over at least half a cycle before it is registered with the protection and control software.

The frequency tracking of the analog input signals is achieved by a recursive Fourier algorithm which is applied to one of the input signals, and works by detecting a change in the measured signal’s phase angle. The calculated value of the frequency is used to modify the sample rate being used by the input module to achieve a constant sample rate of 24 samples per cycle of the power waveform. The value of the frequency is also stored for use by the protection and control task.

When the protection and control task is re-started by the sampling function, it calculates the Fourier components for the analog signals. The Fourier components are calculated using a one-cycle, 24-sample Discrete Fourier Transform (DFT). The DFT is always calculated using the last cycle of samples from the 2-cycle buffer, which is the most recent data. Used in this way, the DFT extracts the power frequency fundamental component from the signal and produces the magnitude and phase angle of the fundamental in rectangular component format. The DFT provides an accurate measurement of the fundamental frequency component, and effective filtering of harmonic frequencies and noise. This performance is achieved with the relay input module which provides hardware anti-alias filtering to attenuate frequencies above the half sample rate, and frequency tracking to maintain a sample rate of 24 samples per cycle. The Fourier components of the input current and voltage signals are stored in memory so they can be accessed by all of the protection elements’ algorithms. The samples from the input module are also used in an unprocessed form by the disturbance recorder for waveform recording and to calculate true RMS values of current, voltage and power for metering purposes.

3.4.3 Frequency Response

With the exception of the RMS measurements, all other measurements and protection functions are based on the Fourier-derived fundamental component. The fundamental component is extracted by using a 24-sample DFT. This gives good harmonic rejection for frequencies up to the 23rd harmonic. The 23rd is the first predominant harmonic that is not attenuated by the Fourier filter and this is known as an ‘Alias’. However, the Alias is attenuated by approximately 85% by an additional, analog, ‘anti-aliasing’ filter (low pass filter). The combined affect of the anti-aliasing and Fourier filters is shown in Figure 8.

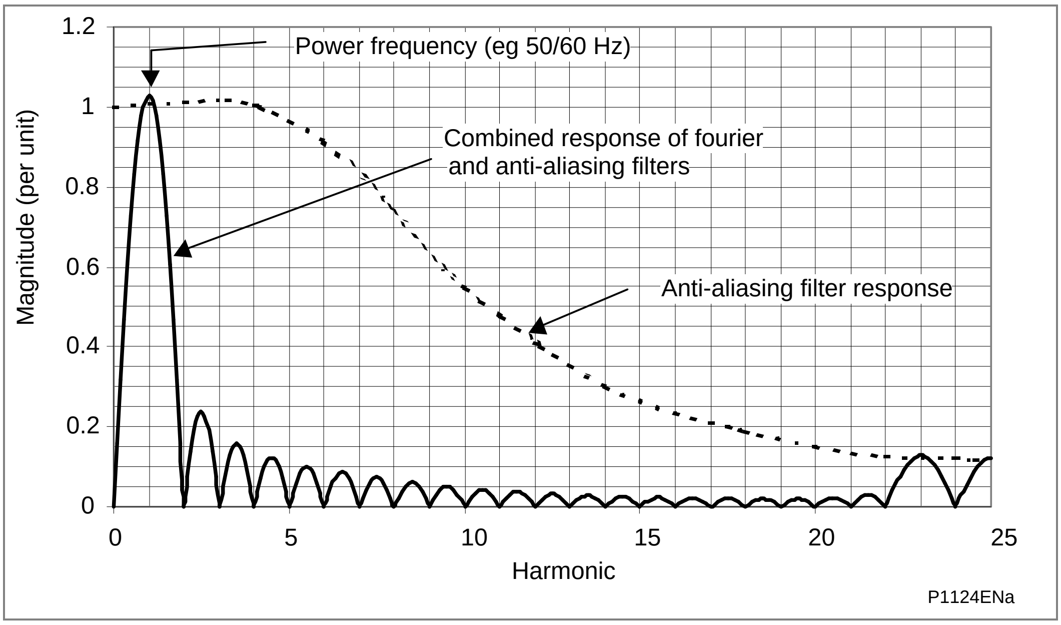


Figure 8 - Frequency response

For power frequencies that are not equal to the selected rated frequency, the harmonics are attenuated to zero amplitude. For small deviations of ±1Hz, this is not a problem but to allow for larger deviations, frequency tracking is used.

Frequency tracking automatically adjusts the sampling rate of the analog to digital conversion to match the applied signal. In the absence of a suitable signal to amplitude track, the sample rate defaults to the selected rated frequency (Fn). If the a signal is in the tracking range of 45 to 66 Hz, the relay locks onto the signal and the measured frequency coincides with the power frequency as shown in Figure 8. The outputs for harmonics up to the 23rd are zero. The relay frequency tracks off any voltage or current in the order VA/VB/VC/IA/IB/IC down to 10% Vn for voltage and 5%In for current.

3.4.4 Programmable Scheme Logic (PSL)

The Programmable Scheme Logic (PSL) allows the relay user to configure an individual protection scheme to suit their own particular application. This is done with programmable logic gates and delay timers.

The input to the PSL is any combination of the status of the digital input signals from the opto-isolators on the input board, the outputs of the protection elements such as protection starts and trips, and the outputs of the fixed PSL. The fixed PSL provides the relay’s standard protection schemes. The PSL consists of software logic gates and timers. The logic gates can be programmed to perform a range of different logic functions and can accept any number of inputs. The timers are used either to create a programmable delay or to condition the logic outputs, such as to create a pulse of fixed duration on the output, regardless of the length of the pulse on the input. The outputs of the PSL are the LEDs on the front panel of the relay and the output contacts at the rear.

The execution of the PSL logic is event driven: the logic is processed whenever any of its inputs change, for example as a result of a change in one of the digital input signals or a trip output from a protection element. Also, only the part of the PSL logic that is affected by the particular input change that has occurred is processed. This reduces the amount of processing time that is used by the PSL. The protection and control software updates the logic delay timers and checks for a change in the PSL input signals every time it runs.

This system provides flexibility for the user to create their own scheme logic design. However, it also means that the PSL can be configured into a very complex system, and because of this setting of the PSL is implemented through the PC support package MiCOM S1 Studio.

3.4.5 Function Key Interface (P643 and P645 only)

The ten function keys interface directly into the PSL as digital input signals and are processed based on the PSLs event-driven execution. However, a change of state is only recognized when a key press is executed, on average for longer than 200 ms. The time to register a change of state depends on whether the function key press is executed at the start or the end of a protection task cycle, with the additional hardware and software scan time included. A function key press can provide a latched (toggled mode) or output on key press only (normal mode) depending on how it is programmed and can be configured to individual protection scheme requirements. The latched state signal for each function key is written to non-volatile memory and read from non-volatile memory during relay power up, allowing the function key state to be reinstated after power-up if the relay power is lost.

3.4.5.1 PSL Data

In the PSL editor in MiCOM S1 Studio, when a PSL file is downloaded to the relay the user can specify the group to download the file and a 32 character PSL reference description. This PSL reference is shown in the **Grp. 1/2/3/4 PSL Ref.** cell in the **PSL DATA** menu in the relay. The download date and time and file checksum for each group’s PSL file is also shown in the **PSL DATA** menu in cells **Date/Time** and **Grp. 1/2/3/4 PSL ID**. The PSL data can be used to show if a PSL has been changed and can be useful in providing information for version control of PSL files.

The default PSL Reference description is **Default PSL** followed by the model number, for example, Default PSL **P64x**??????**0yy0**? where x refers to the model such as 1, 2, 3 and yy refers to the software version such as 05. This is the same for all protection setting groups (since the default PSL is the same for all groups). Since the LCD display (bottom line) only has space for 16 characters, the display must be scrolled to see all 32 characters of the PSL Reference description.

The default date and time is the date and time when the defaults were loaded.

Note	*The PSL DATA column information is only supported by Courier and MODBUS, but not DNP3.0 or IEC60870-5-103.*

3.4.6 Event, Fault and Maintenance Recording

A change in any digital input signal or protection element output signal is used to indicate that an event has taken place. When this happens, the protection and control task sends a message to the supervisor task to show that an event is available to be processed. The protection and control task writes the event data to a fast buffer in SRAM that is controlled by the supervisor task. When the supervisor task receives either an event or fault record message, it instructs the platform software to create the appropriate log in battery backed-up SRAM. The supervisor's buffer is faster than battery backed-up SRAM, therefore the protection software is not delayed waiting for the records to be logged by the platform software. However, if a large number of records to be logged are created in a short time, some may be lost if the supervisor's buffer is full before the platform software is able to create a new log in battery backed-up SRAM. If this occurs, an event is logged to indicate this loss of information.

Maintenance records are created in a similar manner with the supervisor task instructing the platform software to log a record when it receives a maintenance record message. However, it is possible that a maintenance record may be triggered by a fatal error in the relay, in which case it may not be possible to successfully store a maintenance record, depending on the nature of the problem. *See section 4.2 Self-Testing and Diagnostics.*

Fault records are stored in the sequence of events. They can be viewed locally or remotely and include:

- Faulty phase(s)
- Protection Tripped
- Protection Started
- Fault duration
- Fault type (internal or external fault)
- Operating time
- Primary or Secondary RMS values of prefault phase and neutral currents or angle of each winding
- Primary or Secondary RMS values of fault phase and neutral currents or angle of each winding
- Primary or Secondary RMS values of differential and biased current of each phase

3.4.7 Disturbance Recorder

The disturbance recording is started from any relay start or trip, or any specific opto-isolator input or internal information. The recording time is user selectable up to a maximum of 10 seconds. The disturbance recorder operates as a separate task to the protection and control task. It can record the waveforms for up to 22 analog channels and the values of up to 32 digital signals. The disturbance recorder is supplied with data once per cycle by the protection and control task. The disturbance recorder collates the data that it receives into the required length disturbance record. The disturbance records that can also store the data in COMTRADE format can be extracted using MiCOM S1 Studio, allowing the use of other packages to view the recorded data.

4 SELF-TESTING AND DIAGNOSTICS

The relay includes several self-monitoring functions to check the operation of its hardware and software when it is in service. These are included so that if an error or fault occurs in the relay's hardware or software, the relay is able to detect and report the problem and attempt to resolve it by performing a reboot. The relay must therefore be out of service for a short time, during which the **Healthy** LED on the front of the relay is OFF and, the watchdog contact at the rear is ON. If the reboot fails to resolve the problem, the relay takes itself permanently out of service; the **Healthy** LED stays OFF and watchdog contact stays ON.

If a problem is detected by the self-monitoring functions, the relay stores a maintenance record in battery backed-up SRAM.

The self-monitoring is implemented in two stages:

- firstly a thorough diagnostic check that is performed when the relay is booted-up and
- secondly a continuous self-checking operation that checks the operation of the relay's critical functions while it is in service.

4.1 Start-Up Self-Testing

The self-testing that is carried out when the relay is started takes a few seconds to complete, during which time the relay's protection is unavailable. This is shown by the **Healthy** LED on the front of the relay which is ON when the relay has passed all tests and entered operation. If the tests detect a problem, the relay remains out of service until it is manually restored to working order.

The operations that are performed at start-up are:

- System Boot
- Initialization Software
- Platform Software Initialization and Monitoring

4.1.1 System Boot

The integrity of the flash memory is verified using a checksum before the program code and data are copied into SRAM and executed by the processor. When the copy is complete the data then held in SRAM is checked against that in flash memory to ensure they are the same and that no errors have occurred in the transfer of data from flash memory to SRAM. The entry point of the software code in SRAM is then called which is the relay initialization code.

4.1.2 Initialization Software

The initialization process includes the operations of initializing the processor registers and interrupts, starting the watchdog timers (used by the hardware to determine whether the software is still running), starting the real-time operating system and creating and starting the supervisor task. In the initialization process the relay checks the following.

- The status of the battery
- The integrity of the battery backed-up SRAM that stores event, fault and disturbance records
- The voltage level of the field voltage supply that drives the opto-isolated inputs
- The operation of the LCD controller

- The watchdog operation

When the initialization software routine is complete, the supervisor task starts the platform software.

4.1.3 Platform Software Initialization and Monitoring

In starting the platform software, the relay checks the integrity of the data held in non-volatile memory with a checksum, the operation of the real-time clock, and the IRIG-B, RTD and CLIO board if fitted. The final test that is made concerns the input and output of data; the presence and healthy condition of the input board is checked and the analog data acquisition system is checked through sampling the reference voltage.

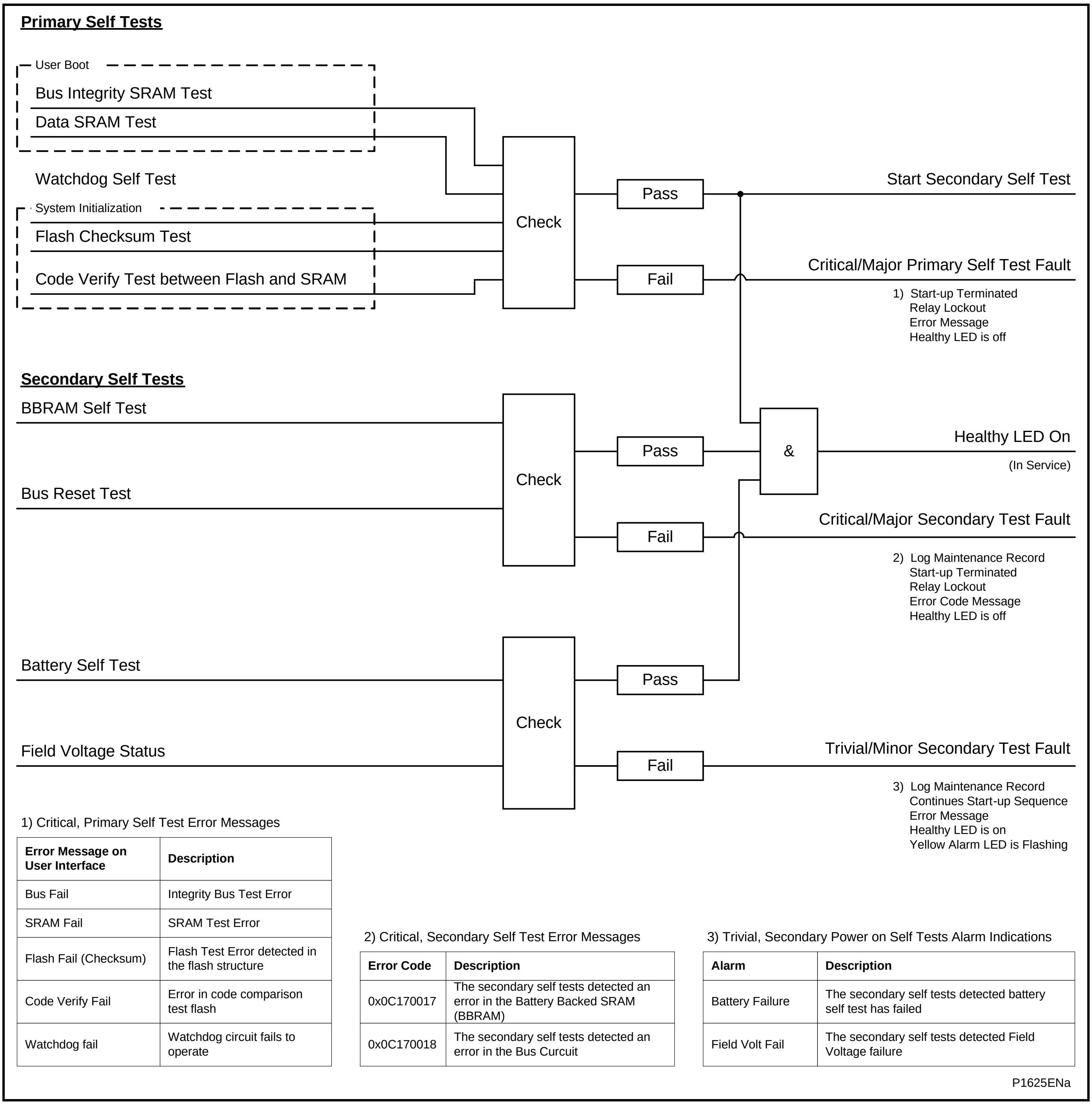
At the successful conclusion of all of these tests the relay is entered into service and the protection started-up.

4.2 Continuous Self-Testing

When the relay is in service, it continually checks the operation of the critical parts of its hardware and software. The checking is carried out by the system services software (see section on relay software earlier in this section) and the results reported to the platform software. The functions that are checked are as follows:

- The flash EPROM containing all program code and language text is verified by a checksum
- The code and constant data held in SRAM is checked against the corresponding data in flash EPROM to check for data corruption
- The SRAM containing all data other than the code and constant data is verified with a checksum
- The non-volatile memory containing setting values is verified by a checksum, whenever its data is accessed
- The battery status
- The level of the field voltage
- The integrity of the digital signal I/O data from the opto-isolated inputs and the relay contacts, is checked by the data acquisition function every time it is executed. The operation of the analog data acquisition system is checked by the acquisition function every time it is executed. This is done by sampling the reference voltage on a spare multiplexed channel
- The operation of the RTD board is checked by reading the temperature indicated by the reference resistors on the two spare RTD channels
- The operation of the IRIG-B board is checked, where it is fitted, by the software that reads the time and date from the board
- The correct operation of the CLIO board is checked, where it is fitted
- If the Ethernet board is fitted, it is checked by the software on the main processor board. If the Ethernet board fails to respond, an alarm is raised and the board is reset in an attempt to resolve the problem

In the unlikely event that one of the checks detects an error in the relay’s subsystems, the platform software is notified and it will attempt to log a maintenance record in battery backed-up SRAM. If the problem is with the battery status, the RTD board, CLIO board or the IRIG-B board, the relay continues in operation. However, for problems detected in any other area the relay shuts down and reboots. This result in a period of up to 5 seconds when protection is unavailable, but the complete restart of the relay including all initializations should clear most problems that could occur. An integral part of the start-up procedure is a thorough diagnostic self-check. If this detects the same problem that caused the relay to restart, the restart has not cleared the problem and the relay takes itself permanently out of service. This is indicated by the **Healthy** LED on the front of the relay which goes OFF, and the watchdog contact that goes ON.


Primary Self Tests
User Boot
Bus Integrity SRAM Test
Data SRAM Test
Watchdog Self Test
System Initialization
Flash Checksum Test
Code Verify Test between Flash and SRAM
Check
Pass
Fail
Start Secondary Self Test
Critical/Major Primary Self Test Fault
1) Start-up Terminated
Relay Lockout
Error Message
Healthy LED is off
Secondary Self Tests
BBRAM Self Test
Bus Reset Test
Check
Pass
Fail
&
Healthy LED On
(In Service)
Critical/Major Secondary Test Fault
2) Log Maintenance Record
Start-up Terminated
Relay Lockout
Error Code Message
Healthy LED is off
Battery Self Test
Field Voltage Status
Check
Pass
Fail
Trivial/Minor Secondary Test Fault
3) Log Maintenance Record
Continues Start-up Sequence
Error Message
Healthy LED is on
Yellow Alarm LED is Flashing
P1625ENa

1) Critical, Primary Self Test Error Messages

Error Message on User Interface	Description
Bus Fail	Integrity Bus Test Error
SRAM Fail	SRAM Test Error
Flash Fail (Checksum)	Flash Test Error detected in the flash structure
Code Verify Fail	Error in code comparison test flash
Watchdog fail	Watchdog circuit fails to operate

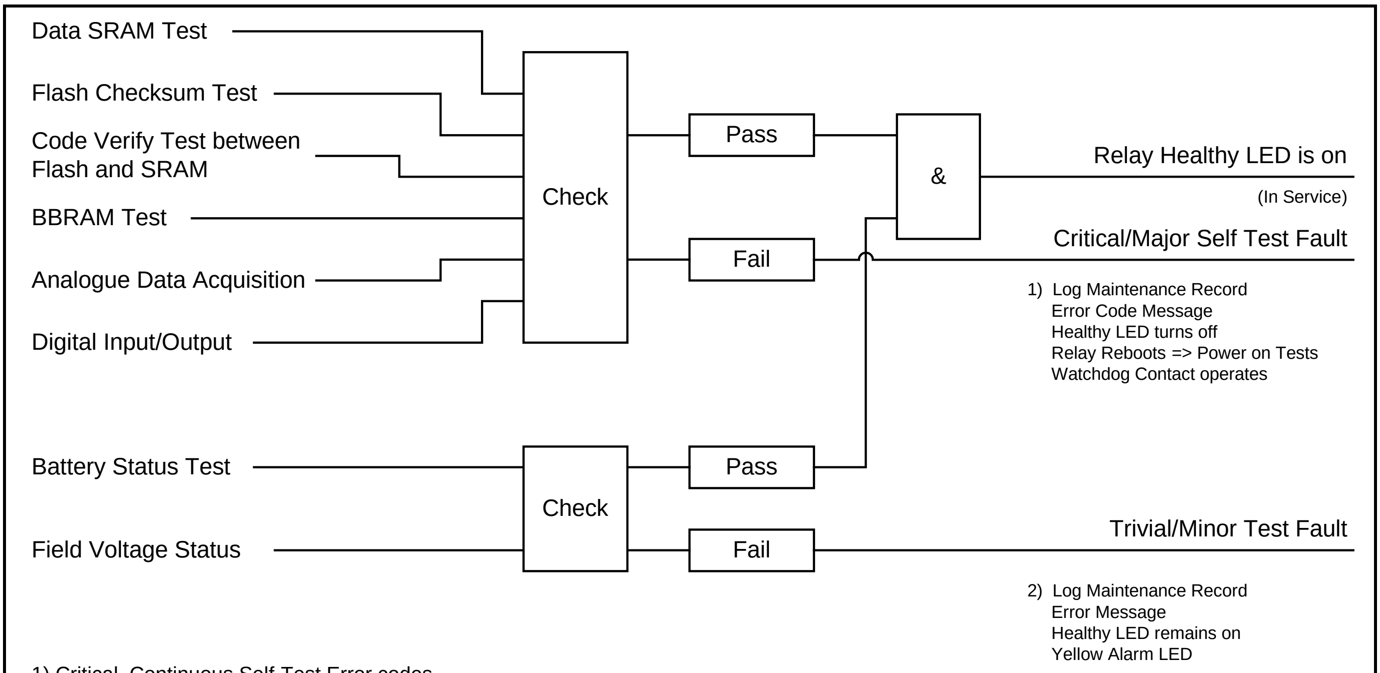
2) Critical, Secondary Self Test Error Messages

Error Code	Description
0x0C170017	The secondary self tests detected an error in the Battery Backed SRAM (BBRAM)
0x0C170018	The secondary self tests detected an error in the Bus Curcuit

3) Trivial, Secondary Power on Self Tests Alarm Indications

Alarm	Description
Battery Failure	The secondary self tests detected battery self test has failed
Field Volt Fail	The secondary self tests detected Field Voltage failure

Figure 9 - Start-up self-testing logic


Data SRAM Test
Flash Checksum Test
Code Verify Test between Flash and SRAM
BBRAM Test
Analogue Data Acquisition
Digital Input/Output
Check
Pass
Fail
&
Relay Healthy LED is on
(In Service)
Critical/Major Self Test Fault
Battery Status Test
Field Voltage Status
Check
Pass
Fail
Trivial/Minor Test Fault

1) Log Maintenance Record
Error Code Message
Healthy LED turns off
Relay Reboots => Power on Tests
Watchdog Contact operates

2) Log Maintenance Record
Error Message
Healthy LED remains on
Yellow Alarm LED

1) Critical, Continuous Self-Test Error codes

Error Code	Description
0x0C160011	The continuous self tests detected an error in SRAM
0x0C160012	The continuous self tests detected an error in the Flash memory checksum
0x0C160013	The continuous self tests detected an error in the code comparison
0x0C160014	The continuous self tests detected an error in the Battery Backed RAM
0x0C1600A0	The continuous self tests detected an error in the acquisition card
0x0C1600Bn	The continuous self tests detected an error in relay card n (number from 0)
0x0C1600Cn	The continuous self tests detected an error in opto card n (number from 0)

2) Trivial, Continuous Self-Test alarm indications

Error Code	Description
Battery Failure	The secondary self tests detected battery self test has failed
Field Volt Fail	The secondary self tests detected Field Voltage failure

P1626ENa

Figure 10 - Continuous self-testing logic

COMMISSIONING

CHAPTER NO 10

Date:	12/2013
Hardware Suffix:	J (P642) K (P643/P645)
Software Version:	04
Connection Diagrams:	10P642xx (xx = 1 to 10) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9)

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Notes:

1 INTRODUCTION

The P64x transformer protection relays are fully numerical in their design, implementing all protection and non-protection functions in software. The relays use a high degree of self-checking and give an alarm in the unlikely event of a failure. Therefore, the commissioning tests do not need to be as extensive as with non-numeric electronic or electro-mechanical relays.

To commission numeric relays, it is only necessary to verify that the hardware is functioning correctly and the application-specific software settings have been applied to the relay. It is considered unnecessary to test every function of the relay if the settings have been verified by one of the following methods:

- Extracting the settings applied to the relay using appropriate setting software (preferred method)
- Using the operator interface

To confirm that the product is operating correctly once the application-specific settings have been applied, perform a test on a single protection element.

Unless previously agreed to the contrary, the customer is responsible for determining the application-specific settings to be applied to the relay and for testing any scheme logic applied by external wiring or configuration of the relay’s internal programmable scheme logic.

Blank commissioning test and setting records are provided at the end of this chapter for completion as required.

As the relay’s menu language is user-selectable, the Commissioning Engineer can change it to allow accurate testing as long as the menu is restored to the customer’s preferred language on completion.

To simplify the specifying of menu cell locations in these Commissioning Instructions, they are given in the form [courier reference: COLUMN HEADING, Cell Text]. For example, the cell for selecting the menu language (first cell under the column heading) is in the System Data column (column 00) so it is given as [0001: SYSTEM DATA, Language].

Caution **Before carrying out any work on the equipment the user should be familiar with the contents of the Safety Section or Safety Guide SFTY/4LM/H11 or later issue and the ratings on the equipment’s rating label.**

2 SETTING FAMILIARIZATION

When first commissioning a P64x relay, allow sufficient time to become familiar with how to apply the settings.

The *Relay Menu Database document* and the *Settings* chapter *(P64x/EN MD, P64x/EN ST)* contain a detailed description of the menu structure of P64x relays. The relay menu database is a separate document which can be downloaded from our website.

With the secondary front cover in place, all keys except the ↵ key are accessible. All menu cells can be read. LEDs and alarms can be reset. However, no protection or configuration settings can be changed, or fault and event records cleared.

Removing the secondary front cover allows access to all keys so that settings can be changed, LEDs and alarms reset, and fault and event records cleared. However, to make changes to menu cells that have access levels higher than the default level, the appropriate password is needed.

Alternatively, if a portable PC with suitable setting software is available (such as MiCOM S1 Studio), the menu can be viewed one page at a time, to display a full column of data and text. This PC software also allows settings to be entered more easily, saved to a file on disk for future reference, or printed to produce a settings record. Refer to the PC software user manual for details. If the software is being used for the first time, allow sufficient time to become familiar with its operation.

3 COMMISSIONING TEST MENU

To minimize the time needed to test MiCOM relays, the relay provides several test facilities under the **COMMISSION TESTS** menu heading. There are menu cells which allow the status of the opto-isolated inputs, output relay contacts, internal digital data bus (DDB) signals and user-programmable LEDs to be monitored. Also, there are cells to test the operation of the output contacts and user-programmable LEDs.

Table 1 shows the relay menu of commissioning tests, including the available setting ranges and factory defaults:

Menu text	Default setting	Settings
COMMISSION TESTS		
Opto I/P Status	-	-
Relay O/P Status	-	-
Test Port Status	-	-
LED Status	-	-
Monitor Bit 1	64 (LED 1)	0 to 511 - see P64x/EN PL for details of Digital Data Bus signals
Monitor Bit 3	66 (LED 3)	
Monitor Bit 4	67 (LED 4)	
Monitor Bit 5	68 (LED 5)	
Monitor Bit 6	69 (LED 6)	
Monitor Bit 7	70 (LED 7)	
Monitor Bit 8	71 (LED 8)	
Test Mode	Disabled	Disabled Test Mode Contacts Blocked
Test Pattern	All bits set to 0	0 = Not Operated 1 = Operated
Contact Test	No Operation	No Operation Apply Test Remove Test
Test LEDs	No Operation	No Operation Apply Test

Table 1 - Commission Tests

3.1 Opto I/P Status

This menu cell displays the status of the relay’s opto-isolated inputs as a binary string, a **1** indicating an energized opto-isolated input and a **0** a de-energized one. If the cursor is moved along the binary numbers, the corresponding label text is displayed for each logic input.

The menu cell can be used during commissioning or routine testing to monitor the status of the opto-isolated inputs while they are sequentially energized with a suitable dc voltage.

3.2 Relay O/P Status

This menu cell displays the status of the Digital Data Bus (DDB) signals that result in energization of the output relays as a binary string, a **1** indicating an operated state and **0** a non-operated state. If the cursor is moved along the binary numbers, the corresponding label text is displayed for each relay output.

The information displayed can be used during commissioning or routine testing to show the status of the output relays when the relay is “in service”. Also, to fault find for output relay damage, compare the status of the output contact under investigation with its associated bit.

Note *When the **Test Mode** cell is set to **Enabled**, this cell continues to show which contacts would operate if the relay was in-service. It does not show the actual status of the output relays.*

3.3 Test Port Status

This menu cell displays the status of the eight DDB signals that have been allocated in the **Monitor Bit** cells. If the cursor is moved along the binary numbers, the corresponding DDB signal text string is displayed for each monitor bit.

By using this cell with suitable monitor bit settings, the state of the DDB signals can be displayed, as various operating conditions or sequences are applied to the relay. Therefore the programmable scheme logic can be tested.

As an alternative to using this cell, the optional monitor/download port test box can be plugged into the monitor/download port behind the bottom access cover. For details see *section 3.11*.

3.4 LED Status

The **LED Status** cell is an 8-bit binary string that shows which of the user-programmable LEDs on the relay are ON when accessing the relay from a remote location. A **1** means that a particular LED is ON and a **0** means that it is OFF.

3.5 Monitor Bits 1 to 8

The eight **Monitor Bit** cells allow the user to select the status of which digital data bus signals can be observed in the **Test Port Status** cell or using the monitor/download port.

Each monitor bit is set by entering the required DDB signal number (0 - 511) from the list of available DDB signals in the *Programmable Logic* chapter *P64x/EN PL*. The pins of the monitor/download port used for monitor bits are shown in Table 2. The signal ground is available on pins 18, 19, 22 and 25.

Monitor Bit	1	2	3	4	5	6	7	8
Monitor/Download Port Pin	11	12	15	13	20	21	23	24

Table 2 - Monitor Bits

Caution **The monitor/download port is not electrically isolated against induced voltages on the communications channel. It should therefore only be used for local communications.**

3.6 Test Mode

The **Test Mode** menu cell is used to allow secondary injection testing to be performed on the relay without operation of the trip contacts. The Test Mode is also used in the IEC60870-5-103 protocol, see the *SCADA Communications* chapter *P64x/EN SC*. It also enables a facility to directly test the output contacts by applying menu-controlled test signals.

To select test mode, set the **Test Mode** menu cell to **Test Mode**. This takes the relay out of service and blocks the maintenance counters. It also causes an alarm condition to be recorded and the yellow **Out of Service** LED switches ON and an alarm message **Prot'n. Disabled** is displayed.

To enable testing of output contacts, set the **Test Mode** cell to **Contacts Blocked**. This blocks the protection from operating the contacts. It also enables the test pattern and contact test functions, used to manually operate the output contacts. Once testing is complete, set the cell back to **Disabled** to restore the relay back to service.

Caution **When the "Test Mode" cell is set to "contacts blocked" the relay scheme logic does not drive the output relays, so the protection does not trip the associated circuit breaker if a fault occurs.**

3.7 Test Pattern

The **Test Pattern** cell is used to select the output relay contacts that will be tested when the **Contact Test** cell is set to **Apply Test**. The cell has a binary string with one bit for each user-configurable output contact, which can be set to **1** to operate the output under test conditions and **0** not to operate it.

3.8 Contact Test

When the **Apply Test** command in this cell is issued, the contacts set to **1** for operation in the **Test Pattern** cell change state. After the test has been applied, the command text on the LCD changes to **No Operation** and the contacts remain in the Test State until reset issuing the **Remove Test** command. The command text on the LCD reverts to **No Operation** after the **Remove Test** command has been issued.

Note *When the **Test Mode** cell is set to **Enabled**, the **Relay O/P Status** cell does not show the current status of the output relays so cannot be used to confirm operation of the output relays. Therefore, it is necessary to monitor the state of each contact in turn.*

3.9 Test LEDs

When the **Apply Test** command in this cell is issued, the eight user-programmable LEDs are ON for approximately two seconds before they switch OFF and the command text on the LCD reverts to **No Operation**.

3.10 Red LED Status and Green LED Status (P643/P645)

The **Red LED Status** and **Green LED Status** cells are 18-bit binary strings that show which of the user-programmable LEDs on the relay are ON when accessing the relay from a remote location. **1** indicates a particular LED is ON and a **0** OFF. When the status of a particular LED in both cells is **1**, this means the LED is yellow.

3.11 Using a Monitor/Download Port Test Box

A monitor/download port test box containing eight LEDs and a switchable audible indicator is available from Schneider Electric, or one of their regional sales offices. It is housed in a small plastic box with a 25-pin male D-connector that plugs directly into the relay's monitor/download port. There is also a 25-pin female D-connector which allows other connections to be made to the monitor/download port while the monitor/download port test box is in place.

Each LED corresponds to one of the monitor bit pins on the monitor/download port with **Monitor Bit 1** on the left hand side when viewed from the front of the relay. The audible indicator can be selected either to sound if a voltage appears on any of the eight monitor pins, or remain silent so that indication of state is by LED alone.

4 EQUIPMENT REQUIRED FOR COMMISSIONING

4.1 Minimum Equipment Required

- Overcurrent test set with interval timer
- 110 V ac voltage supply (if stage 1 of the overcurrent function is set directional)
- Multimeter with suitable ac current range, and ac and dc voltage ranges of 0 to 440 V and 0 to 250 V respectively
- Continuity tester (if not included in multimeter)
- Phase angle meter
- Phase rotation meter
- 100 Ω precision wire wound or metal film resistor, 0.1% tolerance (0°C ±2°C)

Note *Test equipment may contain many of the above features in one unit.*

4.2 Optional Equipment

- Multi-finger test plug type MMLB01 (if test block type MMLG is installed)
- An electronic or brushless insulation tester with a dc output not exceeding 500 V (for insulation resistance testing when required)
- A portable PC, with appropriate software (enabling the rear communications port to be tested, if this is to be used, and saves considerable time during commissioning)
- KITZ K-Bus to EIA(RS)232 protocol converter (if the first rear EIA(RS)485 K-Bus port or second rear port configured for K-Bus is being tested and one is not already installed)
- EIA(RS)485 to EIA(RS)232 converter (if first rear EIA(RS)485 port or second rear port configured for EIA(RS)485 is being tested)
- A printer, for printing a setting record from the portable PC

5 PRODUCT CHECKS

These product checks cover all aspects of the relay that need to be checked to ensure that it has not been physically damaged before commissioning, is functioning correctly and all input quantity measurements are within the stated tolerances.

If the application-specific settings have been applied to the relay before commissioning, it is advisable to make a copy of the settings to allow their restoration later. If programmable scheme logic (other than the default settings with which the relay is supplied) has been applied, the default settings should be restored before commissioning. This can be done by:

- Obtaining a setting file on a diskette from the customer. This requires a portable PC with appropriate setting software for transferring the settings from the PC to the relay.
- Extracting the settings from the relay itself. This requires a portable PC with appropriate setting software.
- Manually creating a setting record. This could be done using a copy of the setting record from the end of this chapter to record the settings as the relay’s menu is sequentially stepped through using the front panel user interface.

If password protection is enabled, and the customer has changed password 2 that prevents unauthorized changes to some of the settings, either the revised password 2 should be provided, or the customer should restore the original password before testing is started.

Note *If the password has been lost, a recovery password can be obtained from Schneider Electric by quoting the serial number of the relay. The recovery password is unique to that relay and will not work on any other relay.*

Caution **Before carrying out any work on the equipment the user should be familiar with the contents of the Safety Section or Safety Guide SFTY/4LM/H11 or later issue and the ratings on the equipment’s rating label.**

5.1 With the Relay Re-Energized

The following group of tests should be carried out without the auxiliary supply applied to the relay and with the trip circuit isolated.

The current and voltage transformer connections must be isolated from the relay for these checks. If a P991 or MMLG test block is provided, insert the test plug type P992 or MMLB01, which open-circuits all wiring routed through the test block.

Before inserting the test plug, refer to the scheme diagram to ensure this will not cause damage or a safety hazard. For example, the test block may be associated with protection current transformer circuits. Before the test plug is inserted into the test block, make sure the sockets in the test plug which correspond to the current transformer secondary windings are linked.

DANGER **Never open-circuit the secondary circuit of a current transformer because the high voltage produced may be lethal. It could also damage insulation.**

If a test block is not provided, isolate the voltage transformer supply to the relay using the panel links or connecting blocks. Short-circuit and disconnect the line current transformers from the relay terminals. Where means of isolating the auxiliary supply and trip circuit (such as isolation links, fuses and MCB) are provided, these should be used. If this is impossible, the wiring to these circuits must be disconnected and the exposed ends suitably terminated to prevent them from being a safety hazard.

5.1.1 Visual Inspection

Caution **Check the rating information under the top access cover on the front of the relay. Check that the relay being tested is correct for the protected line or circuit. Ensure that the circuit reference and system details are entered onto the setting record sheet. Double-check the CT secondary current rating, and be sure to record the actual CT tap which is in use.**

Carefully examine the relay to see that no physical damage has occurred since installation.

Ensure that the case earthing connections, at the bottom left-hand corner at the rear of the relay case, are used to connect the relay to a local earth bar using an adequate conductor.

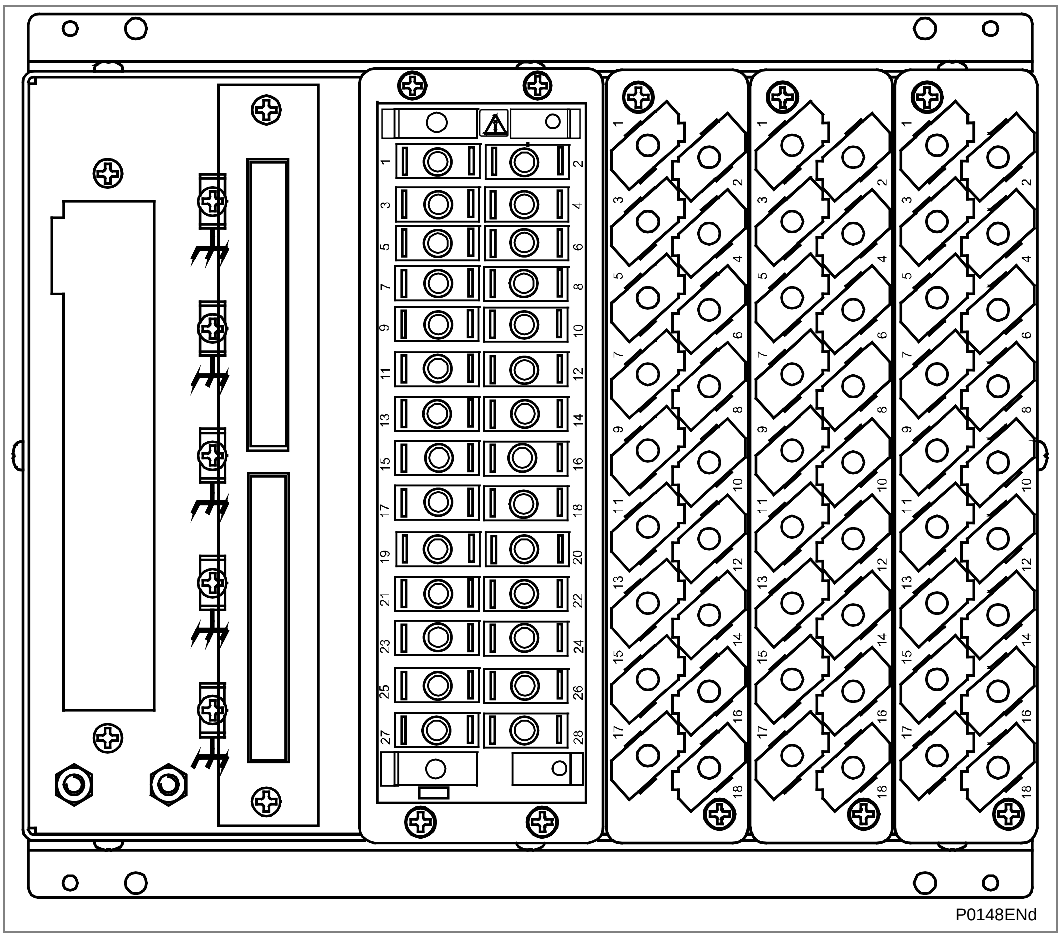


Figure 1 - Rear terminal blocks on size 40TE case

5.1.2 Current Transformer Shorting Contacts

If required, the current transformer shorting contacts can be checked to ensure that they close when the heavy duty terminal block (block reference C in Figure 1) is disconnected from the current input PCB. The P642 relay block reference D (40TE case) uses heavy duty terminal blocks. The heavy duty terminal blocks on the P643/P645 relays are at block references D and E (60TE, 80TE cases).

Current input	**Shorting Contact Between Terminals**		
	P642 (40TE)	**P643 (60TE)**	**P645 (60TE/80TE)**
	1A / 5A CTs	1A / 5A CTs	1A / 5A CTs
IA1	D24-D23	D24-D23	D24-D23
IB1	D26-D25	D26-D25	D26-D25
IC1	D28-D27	D28-D27	D28-D27
IA2	D18-D17	D18-D17	D18-D17
IB2	D20-D19	D20-D19	D20-D19
IC2	D22-D21	D22-D21	D22-D21
IA3		E24-E23	E24-E23
IB3		E26-E25	E26-E25
IC3		E28-E27	E28-E27
IA4			E18-E17
IB4			E20-E19
IC4			E22-E21
IA5			E12-E11
IB5			E14-E13
IC5			E16-E15
IN-TV		D12-D11	D12-D11
IN-LV	D14-D13	D14-D13	D14-D13
IN-HV	D16-D15	D16-D15	D16-D15

Table 3 - Current transformer shorting contact locations

Heavy duty terminal blocks are fastened to the rear panel using four crosshead screws. These are at the top and bottom between the first and second, and third and fourth, columns of terminals (see Figure 2).

Note *Use a magnetic-bladed screwdriver to avoid losing screws or leaving them in the terminal block.*

Pull the terminal block away from the rear of the case and check with a continuity tester that all the shorting switches being used are closed. Table 3 shows the terminals between which shorting contacts are fitted.

Caution **If external test blocks are connected to the relay, take great care when using the associated test plugs such as MMLB and MiCOM P992 since their use may make hazardous voltages accessible. CT* shorting links must be in place before the insertion or removal of MMLB test plugs, to avoid potentially lethal voltages.**

Note *When a MiCOM P992 Test Plug is inserted into the MiCOM P991 Test Block, the secondaries of the line CTs are automatically shorted, making them safe.*

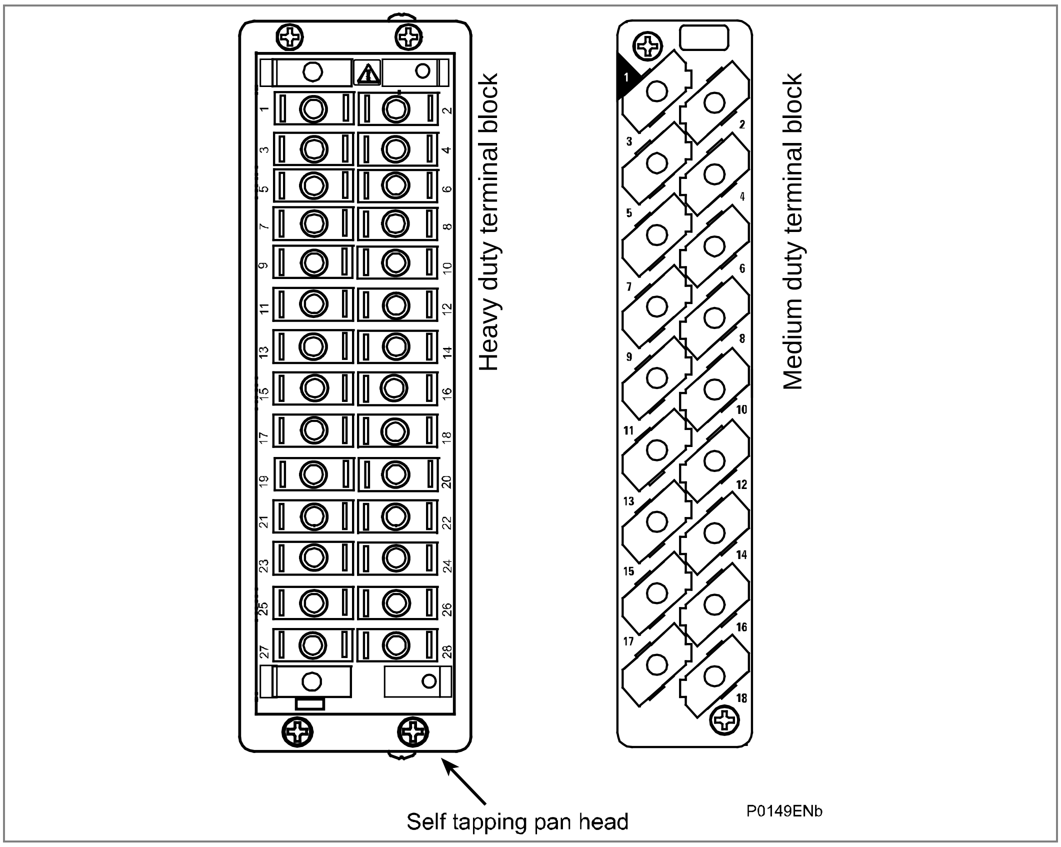


Figure 2 - Location of securing screws for terminal blocks

5.1.3 Insulation

Insulation resistance tests are only necessary during commissioning if it is required for them to be done and they haven’t been performed during installation.

Isolate all wiring from the earth and test the insulation with an electronic or brushless insulation tester at a dc voltage not exceeding 500 V. Terminals of the same circuits should be temporarily connected together.

The main groups of relay terminals are:

- Voltage transformer circuits
- Current transformer circuits
- Auxiliary voltage supply
- Field voltage output and opto-isolated control inputs
- Relay contacts
- First rear EIA(RS)485 communication port
- RTD inputs
- Current loop (analog) inputs and outputs (CLIO)
- Case earth

The insulation resistance should be greater than 100 MΩ at 500 V.

On completion of the insulation resistance tests, ensure all external wiring is correctly reconnected to the unit.

5.1.4 External Wiring

Check that the external wiring is correct to the relevant relay diagram or wiring diagram. The relay diagram number appears on the rating label under the top access cover on the front of the relay. The corresponding connection diagram will have been supplied with the Schneider Electric order acknowledgement for the relay.

If a P991 or MMLG test block is provided, check the connections against the wiring diagram. It is recommended that the supply connections are to the live side of the test block (colored orange with the odd numbered terminals 1, 3, 5, 7, and so on). The auxiliary supply is normally routed through terminals 13 (supply positive) and 15 (supply negative), with terminals 14 and 16 connected to the relay's positive and negative auxiliary supply terminals respectively. However, check the wiring against the schematic diagram for the installation to ensure compliance with the customer's normal practice.

5.1.5 Watchdog Contacts

Using a continuity tester, check that the watchdog contacts are in the states shown in Table 4 for a de-energized relay.

Terminals		Contact state	
		Relay de-energized	Relay energized
F11 - F12 J11 - J12 M11 - M12	(P642 40TE) (P643/P645 60TE) (P645 80TE)	Closed	Open
F13 - F14 J13 - J14 M13 - M14	(P642 40TE) (P643/P645 60TE) (P645 80TE)	Open	Closed

Table 4 - Watchdog contact status

5.1.6 Auxiliary Supply

The relay can be operated from either a dc only or an ac/dc auxiliary supply depending on the relay's nominal supply rating. The incoming voltage must be within the operating range specified in Table 5.

Without energizing the relay, measure the auxiliary supply to ensure it is within the operating range.

Nominal supply rating DC [AC rms]		DC operating range	AC operating range
24 - 48 V	[-]	19 - 65 V	-
48 - 110 V	[40 - 100 V]	37 - 150 V	24 - 110 V
110 - 240 V	[100 - 240 V]	87 - 300 V	80 - 265 V

Table 5 - Operational range of auxiliary supply Vx

Note *The relay can withstand an ac ripple of up to 12% of the upper rated voltage on the dc auxiliary supply.*

Caution **Do not energize the relay using the battery charger with the battery disconnected as this can irreparably damage the relay's power supply circuitry.**

Caution **Energize the relay only if the auxiliary supply is within the operating range. If a test block is provided, it may be necessary to link across the front of the test plug to connect the auxiliary supply to the relay.**

5.2 With the Relay Energized

The following group of tests verify that the relay hardware and software is functioning correctly and should be carried out with the auxiliary supply applied to the relay.

Caution **The current and voltage transformer connections must remain isolated from the relay for these checks. The trip circuit should also remain isolated to prevent accidental operation of the associated circuit breaker.**

5.2.1 Watchdog Contacts

Using a continuity tester, check the watchdog contacts are in the states shown in Table 4 for an energized relay.

5.2.2 LCD Front Panel Display

The liquid crystal display is designed to operate in a wide range of substation ambient temperatures. For this purpose, the Px40 relays have an **LCD Contrast** setting. This allows the user to adjust the lightness or darkness of the displayed characters. The contrast is factory preset to account for a standard room temperature, however it may be necessary to adjust the contrast to give the best in-service display. To change the contrast, at the bottom of the **CONFIGURATION** column, use cell [09FF: LCD Contrast] to increment (darker) or decrement (lighter), as required.

Caution **Before applying a contrast setting, ensure that it does not make the display too light or dark so the menu text becomes unreadable. If this happens, it is possible to restore the display by downloading a MiCOM S1 Studio setting file, with the LCD Contrast set in the typical range of 7 to 11.**

5.2.3 Date and Time

Before setting the date and time, ensure that the factory-fitted battery isolation strip that prevents battery drain during transportation and storage has been removed. With the lower access cover open, the presence of the battery isolation strip can be checked by a red tab protruding from the positive side of the battery compartment. Lightly pressing the battery to prevent it falling out of the battery compartment, pull the red tab to remove the isolation strip.

The data and time should now be set to the correct values. The method of setting depends on whether accuracy is being maintained through the optional inter-range instrumentation group standard B (IRIG-B) port on the rear of the relay.

5.2.3.1 With an IRIG-B Signal

If a satellite time clock signal conforming to IRIG-B is provided and the relay has the optional IRIG-B port fitted, the satellite clock equipment should be energized.

To allow the relay’s time and date to be maintained from an external IRIG-B source cell [0804: DATE and TIME, IRIG-B Sync.] must be set to **Enabled**.

Ensure the relay is receiving the IRIG-B signal by checking that cell [0805: DATE and TIME, IRIG-B Status] reads **Active**.

Once the IRIG-B signal is active, adjust the time offset of the universal coordinated time (satellite clock time) on the satellite clock equipment so that local time is displayed.

Check the time, date and month are correct in cell [0801: DATE and TIME, Date/Time]. The IRIG-B signal does not contain the current year so needs to be set manually in this cell.

If the auxiliary supply fails, with a battery fitted in the compartment behind the bottom access cover, the time and date is maintained. Therefore, when the auxiliary supply is restored, the time and date are correct and need not be set again.

To test this, remove the IRIG-B signal, then remove the auxiliary supply from the relay. Leave the relay de-energized for approximately 30 seconds. On re-energization, the time in cell [0801: DATE and TIME, Date/Time] should be correct. Then reconnect the IRIG-B signal.

5.2.3.2 Without an IRIG-B Signal

If the time and date is not being maintained by an IRIG-B signal, ensure that cell [0804: DATE and TIME, IRIG-B Sync.] is set to **Disabled**.

Set the date and time to the correct local time and date using cell [0801: DATE and TIME, Date/Time].

If the auxiliary supply fails, with a battery fitted in the compartment behind the bottom access cover, the time and date are maintained. Therefore when the auxiliary supply is restored, the time and date are correct and need not be set again.

To test this, remove the auxiliary supply from the relay for approximately 30 seconds. On re-energization, the time in cell [0801: DATE and TIME, Date/Time] should be correct.

5.2.4 Light Emitting Diodes (LEDs)

On power-up, the green LED should switch on and stay on, indicating that the relay is healthy. The relay has non-volatile memory which stores the state (on or off) of the alarm, trip and, if configured to latch, user-programmable LED indicators when the relay was last energized from an auxiliary supply. Therefore these indicators may also switch on when the auxiliary supply is applied.

If any of these LEDs are on, reset them before proceeding with further testing. If the LED successfully resets (the LED switches off), there is no testing required for that LED because it is known to be operational.

5.2.4.1 Testing the Alarm and Out Of Service LEDs

The alarm and out of service LEDs can be tested using the **COMMISSIONING TESTS** menu column. Set cell [0F0D: COMMISSIONING TESTS, Test Mode] to **Contacts Blocked**. Check that the out of service LED is on continuously and the alarm LED flashes.

It is not necessary to return cell [0F0D: COMMISSIONING TESTS, Test Mode] to **Disabled** at this stage because the test mode will be required for later tests.

5.2.4.2 Testing the Trip LED

The trip LED can be tested by initiating a manual circuit breaker trip from the relay. However, the trip LED will operate during the setting checks performed later. Therefore no further testing of the trip LED is required at this stage.

5.2.4.3 Testing the User-Programmable LEDs

To test the user-programmable LEDs set cell [0F10: COMMISSIONING TESTS, Test LEDs] to **Apply Test**. Check that all 8 (P643) or 18 (P643/5) programmable LEDs on the relay switch on.

5.2.5 Field Voltage Supply

The relay generates a field voltage of nominally 48 V that can be used to energize the opto-isolated inputs (alternatively the substation battery may be used).

Measure the field voltage across terminals 7 and 9 on the terminal block shown in Table 6. Check that the field voltage is in the range 40 V to 60 V when no load is connected and that the polarity is correct.

Repeat for terminals 8 and 10.

Supply rail	Terminals		
	P642 (40TE)	**P643/P645 (60TE)**	**P645 (80TE)**
+ve	F7 & F8	J7 & J8	M7 & M8
-ve	F9 & F10	J9 & J10	M9 & M10

Table 6 - Field voltage terminals

5.2.6 Input Opto-Isolators

This test checks that all the opto-isolated inputs are functioning correctly. The P642 relay has 8 to 12 opto-isolated inputs in the 40TE case. The P643 relay has 16 to 24 opto-isolated inputs in the 60TE case. The P645 has 16 to 24 opto-isolated inputs in the 60TE case and 24 opto-isolated inputs in the 80TE.

Energize the opto-isolated inputs one at a time; see the external connection diagrams in chapter *P64x/EN IN* for terminal numbers. Ensure that the correct opto input nominal voltage is set in the **Opto Config**. Menu. Ensure correct polarity and connect the field supply voltage to the appropriate terminals for the input being tested. Each opto input also has selectable filtering. This allows use of a pre-set filter of ½ cycle that renders the input immune to induced noise on the wiring.

Note *The opto-isolated inputs may be energized from an external dc auxiliary supply (such as the station battery) in some installations. Check that this is not the case before connecting the field voltage, otherwise damage to the relay may result. If an external 24/27 V, 30/34 V, 48/54 V, 110/125 V, 220/250 V supply is being used it will be connected to the relay's optically isolated inputs directly. If an external supply is used it must be energized for this test, but only after confirming that it is suitably rated, with less than 12% ac ripple.*

The status of each opto-isolated input can be viewed using either cell [0020: SYSTEM DATA, Opto I/P Status] or [0F01: COMMISSIONING TESTS, Opto I/P Status], a **1** indicating an energized input and a **0** indicating a de-energized input. When each opto-isolated input is energized, one of the characters on the bottom line of the display changes, to indicate the new state of the inputs.

5.2.7 Output Relays

This test checks that all the output relays are functioning correctly. The P642 relay has 8 to 12 output relays in the 40TE case. The P643 relay has 16 to 24 output relays in the 60TE case. The P645 has 16 to 24 output relays in the 60TE case, 24 outputs in the 80TE case.

Ensure that the cell [0F0D: COMMISSIONING TESTS, Test Mode] is set to **Contacts Blocked**.

The output relays should be energized one at a time. To select output relay 1 for testing, set cell [0F0E: COMMISSIONING TESTS, Test Pattern] to 00000000000000000000000000000001.

Connect a continuity tester across the terminals corresponding to output relay 1 as shown in the relevant external connection diagram in the *Installation* chapter *P64x/EN IN*.

To operate the output relay, set cell [0F0F: COMMISSIONING TESTS, Contact Test] to **Apply Test**. Operation is confirmed by the continuity tester operating for a normally open contact and ceasing to operate for a normally closed contact. Measure the resistance of the contacts in the closed state.

Reset the output relay by setting cell [0F0F: COMMISSIONING TESTS, Contact Test] to **Remove Test**.

> *Note* *Ensure that the thermal ratings of anything connected to the output relays during the contact test procedure are not exceeded by the associated output relay being operated for too long. Keep the time between application and removal of contact test to a minimum.*

Repeat the test for the rest of the relays.

Return the relay to service by setting cell [0F0D: COMMISSIONING TESTS, Test Mode] to **Disabled**.

5.2.8 RTD Inputs

This test checks that all the RTD inputs are functioning correctly and is only performed on relays with the RTD board fitted.

A 100 Ω resistor, preferably with a tolerance of 0.1%, should be connected across each RTD in turn. The resistor needs to have a very small tolerance as RTDs complying with BS EN 60751 : 1995 typically have a change of resistance of 0.39 Ω per °C, therefore the use of a precision wire wound or metal film resistor is recommended. It is essential to connect the RTD common return terminal to the appropriate RTD input, otherwise the relay reports an RTD error because it assumes that the RTD wiring has been damaged. The connections required for testing each RTD input are shown in Table 7.

Check that the corresponding temperature displayed in the **MEASUREMENTS 3** column of the menu is 0°C ±2°C. This range takes into account the 0.1% resistor tolerance and relay accuracy of ±1°C. If a resistor of lower accuracy is used during testing, the acceptable setting range needs to be increased.

RTD	Terminal connections		Measurement cell (in “Measurements 3” Column (04) of Menu)
	Resistor between	Wire between	
1	B1 and B2	B2 and B3	[0412: RTD 1 Label]
2	B4 and B5	B5 and B6	[0413: RTD 2 Label]
3	B7 and B8	B8 and B9	[0414: RTD 3 Label]
4	B10 and B11	B11 and B12	[0415: RTD 4 Label]
5	B13 and B14	B14 and B15	[0416: RTD 5 Label]
6	B16 and B17	B17 and B18	[0417: RTD 6 Label]
7	B19 and B20	B20 and B21	[0418: RTD 7 Label]
8	B22 and B23	B23 and B24	[0419: RTD 8 Label]
9	B25 and B26	B26 and B27	[041A: RTD 9 Label]
10	B28 and B29	B29 and B30	[041B: RTD 10 Label]

Table 7 - RTD input terminals

5.2.9 Current Loop Inputs

This test checks that all the current loop (analog) inputs are functioning correctly and is only performed on relays with the Current Loop Input Output (CLIO) board fitted.

For details of the relay terminal connections see the connection diagrams in the *Installation* chapter *P64x/EN IN*. Note that for the current loop inputs, the physical connection of the 0 to 1 mA input is different to that of the 0 to 10, 0 to 20, and 4 to 20 mA inputs, as shown in the connection diagrams.

An accurate dc current source can be used to apply various current levels to the current loop inputs. Another approach is to use the current loop output as a convenient and flexible dc current source to test the input protection functionality. Externally the current loop outputs can be fed into their corresponding current loop inputs. Then by applying a certain level of analog signal, such as V_A, to the relay the required dc output level can be obtained from the current loop output which is feeding the current loop input.

Enable the current loop input to be tested. Set the CLIx minimum and maximum settings and the CLIx Input type for the application.

Apply a dc current to the relay current loop input at 50% of the CLI input maximum range, 0.5 mA (0 to 1 mA CLI), 5 mA (0 to 10 mA CLI) or 10 mA (0 to 20, 4 to 20 mA CLI).

Check the accuracy of the current loop input using the MEASUREMENTS 3 - CLIO Input 1/2/3/4 column of the menu. The display should show (CLIx maximum + CLIx minimum)/2 ±1% full scale accuracy.

5.2.10 Current Loop Outputs

This test checks that all the current loop (analog) outputs are functioning correctly and is only performed on relays with the CLIO board fitted.

For details of the relay terminal connections, see the connection diagrams in the *Installation* chapter *P64x/EN IN*.

Note	*For the current loop outputs the physical connection of the 0 to 1 mA output is different to that of the 0 to 10, 0 to 20, and 4 to 20 mA outputs, as shown in the connection diagrams.*

Enable the current loop output to be tested. Set the CLOx parameter, CLOx minimum and maximum settings and the CLOx output type for the application. Apply the appropriate analog input parameter to the relay equals to (CLOx maximum + CLOx minimum)/2. The current loop output should be at 50% of its maximum rated output. Using a precision resistive current shunt and a high-resolution voltmeter, check that the current loop output is at 50% of its maximum rated output, 0.5 mA (0 to 1 mA CLO), 5 mA (0 to 10 mA CLO) or 10 mA (0 to 20, 4 to 20 mA CLO). The accuracy should be within ±0.5% of full scale + meter accuracy.

5.2.11 First Rear Communications Port

This test should only be performed where the relay is to be accessed from a remote location and varies depending on the communications standard adopted.

It is not the intention of the test to verify the operation of the complete system from the relay to the remote location, just the relay's rear communications port and any protocol converter necessary.

5.2.11.1 Courier Communications

If a K-Bus to EIA(RS)232 KITZ protocol converter is installed, connect a portable PC running the appropriate software (such as MiCOM S1 Studio or PAS&T) to the incoming (remote from relay) side of the protocol converter.

If a KITZ protocol converter is not installed, it may not be possible to connect the PC to the relay installed. In this case a KITZ protocol converter and portable PC running appropriate software should be temporarily connected to the relay's first rear K-Bus port. The terminal numbers for the relay's first rear K-Bus port are shown in Table 8. However, as the installed protocol converter is not being used in the test, only the correct operation of the relay's K-Bus port will be confirmed.

Connection		Terminal		
K-Bus	**MODBUS, VDEW or DNP3.0**	**P642 (40TE)**	**P643/P645 (60TE)**	**P643/P645 (80TE)**
Screen	Screen	F16	J16	M16
1	+ve	F17	J17	M17
2	-ve	F18	J18	M18

Table 8 - EIA(RS)485 terminals

Ensure that the communications baud rate and parity settings in the application software are set the same as those on the protocol converter (usually a KITZ but could be a SCADA RTU). The relay's Courier address in cell [0E02: COMMUNICATIONS, Remote Address] must be set to a value between 1 and 254.

Check that communications can be established with this relay using the portable PC.

If the relay has the optional fiber optic communications port fitted, the port to be used should be selected by setting cell [0E07: COMMUNICATIONS, Physical Link] to **Fiber Optic**. Ensure that the relay address and baud rate settings in the application software are set the same as those in cell [0E04 COMMUNICATIONS, Baud Rate] of the relay. Check, using the Master Station, that communications with the relay can be established.

5.2.11.2 MODBUS Communications

Connect a portable PC running the appropriate MODBUS Master Station software to the relay's first rear EIA(RS)485 port using an EIA(RS)485 to EIA(RS)232 interface converter. The terminal numbers for the relay's EIA(RS)485 port are shown in Table 8.

Ensure that the relay address, baud rate and parity settings in the application software are set the same as those in cells [0E02: COMMUNICATIONS, Remote Address], [0E04: COMMUNICATIONS, Baud Rate] and [0E05: COMMUNICATIONS, Parity] of the relay.

Check that communications with this relay can be established.

If the relay has the optional fiber optic communications port fitted, the port to be used should be selected by setting cell [0E07: COMMUNICATIONS, Physical Link] to **Fiber Optic**. Ensure that the relay address and baud rate settings in the application software are set the same as those in cell [0E04: COMMUNICATIONS, Baud Rate] of the relay. Check, using the Master Station, that communications with the relay can be established.

5.2.11.3 IEC60870-5-103 (VDEW) Communications

If the relay has the optional fiber optic communications port fitted, the port to be used should be selected by setting cell [0E07: COMMUNICATIONS, Physical Link] to **Fiber Optic** or **EIA(RS)485**.

IEC60870-5-103/VDEW communication systems are designed to have a local Master Station and this should be used to verify that the relay's rear fiber optic or EIA(RS)485 port, as appropriate, is working.

Ensure that the relay address and baud rate settings in the application software are set the same as those in cells [0E02: COMMUNICATIONS, Remote Address] and [0E04: COMMUNICATIONS, Baud Rate] of the relay.

Check, using the Master Station, that communications with the relay can be established.

5.2.11.4 DNP3.0 Communications

Connect a portable PC running the appropriate DNP3.0 Master Station Software to the relay's first rear EIA(RS)485 port using an EIA(RS)485 to EIA(RS)232 interface converter. The terminal numbers for the relay's EIA(RS)485 port are shown in Table 8.

Ensure that the relay address, baud rate and parity settings in the application software are set the same as those in cells [0E02: COMMUNICATIONS, Remote address], [0E04: COMMUNICATIONS, Baud Rate] and [0E05: COMMUNICATIONS, Parity] of the relay.

Check that communications with this relay can be established.

If the relay has the optional fiber optic communications port fitted, the port to be used should be selected by setting cell [0E07: COMMUNICATIONS, Physical Link] to **Fiber Optic**. Ensure that the relay address and baud rate settings in the application software are set the same as those in cell [0E04: COMMUNICATIONS, Baud Rate] of the relay. Check that, using the Master Station, communications with the relay can be established.

5.2.11.5 IEC 61850 COMMUNICATIONS

Connect a portable PC running the appropriate IEC61850 Master Station Software or MMS browser to the relay's Ethernet port (RJ45 or ST fiber optic connection). The terminal numbers for the relay's Ethernet port are shown in Table 9.

Configuration of the relay IP parameters (IP Address, Subnet Mask, Gateway) and SNTP time synchronization parameters (SNTP Server 1, SNTP Server 2) is performed by the IED Configurator tool. If these parameters are not available from an SCL file, they must be configured manually.

If the assigned IP address is duplicated elsewhere on the same network, the remote communications operates in an indeterminate way. However, the relay checks for a conflict on every IP configuration change and at power-up. An alarm is raised if an IP conflict is detected. The relay can be configured to accept data from networks other than the local network by using the **Gateway** setting.

Check that communications with this relay can be established.

To communicate with an IEC 61850 IED on Ethernet, it is necessary only to know its IP address. This can then be configured in either of the following:

- An IEC 61850 client (or master), such as a PACiS computer (MiCOM C264) or HMI
- An MMS browser, with which the full data model can be retrieved from the IED without any previous knowledge

Setting changes such as protection settings are not supported in the current IEC 61850 implementation. Such setting changes are done using MiCOM S1 Studio using the front port serial connection of the relay, or over the Ethernet link if preferred. This is known as tunneling. See the *SCADA Communications* chapter*, P64x/EN SC* for more information on IEC 61850.

The connector for the Ethernet port is a shielded RJ45. Table 9 shows the signals and pins on the connector:

Pin	Signal name	Signal definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used

Pin	Signal name	Signal definition
8	-	Not used

Table 9 - Signals on the Ethernet connector

5.2.12 Second Rear Communications Port

This test should only be performed where the relay is to be accessed from a remote location and varies depending on the communications standard being adopted.

It is not the intention of the test to verify the operation of the complete system from the relay to the remote location, just the relay's rear communications port and any protocol converter necessary.

5.2.12.1 K-Bus Configuration

If a K-Bus to EIA(RS)232 KITZ protocol converter is installed, connect a portable PC running the appropriate software (MiCOM S1 Studio or PAS&T) to the incoming (remote from relay) side of the protocol converter.

If a KITZ protocol converter is not installed, it may not be possible to connect the PC to the relay installed. In this case a KITZ protocol converter and portable PC running appropriate software should be temporarily connected to the relay's second rear communications port configured for K-Bus. The terminal numbers for the relay's K-Bus port are shown in Table 10. However, as the installed protocol converter is not being used in the test, only the correct operation of the relay's K-Bus port is confirmed.

Pin*	Connection
4	EIA(RS)485 - 1 (+ ve)
7	EIA(RS)485 - 2 (- ve)
* All other pins unconnected.	

Table 10 - Second rear communications port K-Bus terminals

Ensure that the communications baud rate and parity settings in the application software are set the same as those on the protocol converter (usually a KITZ but could be a SCADA RTU). The relay's Courier address in cell [0E90: COMMUNICATIONS, RP2 Address] must be set to a value between 1 and 254. The second rear communication's port configuration [0E88: COMMUNICATIONS RP2 Port Config.] must be set to K-Bus.

Check that communications can be established with this relay using the portable PC.

5.2.12.2 EIA(RS)485 Configuration

If an EIA(RS)485 to EIA(RS)232 converter (Schneider Electric CK222) is installed, connect a portable PC running the appropriate software (MiCOM S1 Studio) to the EIA(RS)232 side of the converter and the second rear communications port of the relay to the EIA(RS)485 side of the converter.

The terminal numbers for the relay's EIA(RS)485 port are shown in Table 11.

Ensure that the communications baud rate and parity settings in the application software are the same as those in the relay. The relay's Courier address in cell [0E90: COMMUNICATIONS, RP2 Address] must be set to a value between 1 and 254. The second rear communications port's configuration [0E88: COMMUNICATIONS RP2 Port Config.] must be set to EIA(RS)485.

Check that communications can be established with this relay using the portable PC.

5.2.12.3 EIA(RS)232 Configuration

Connect a portable PC running the appropriate software (MiCOM S1 Studio) to the rear EIA(RS)232 port of the relay. This port is actually compliant with EIA(RS)574; the 9-pin version of EIA(RS)232, see www.tiaonline.org.

The second rear communications port connects using the 9-way female D-type connector (SK4). The connection is compliant with EIA(RS)574.

Pin	Connection
1	No Connection
2	RxD
3	TxD
4	DTR#
5	Ground
6	No Connection
7	RTS#
8	CTS#
9	No Connection
# These pins are control lines for use with a modem.	

Table 11 - Second rear communications port EIA(RS)232 terminals

Connections to the second rear port configured for EIA(RS)232 operation can be made using a screened multi-core communication cable up to 15 m long, or a total capacitance of 2500 pF. Terminate the cable at the relay end with a 9-way, metal-shelled, D-type male plug. The terminal numbers for the relay's EIA(RS)232 port are shown in Table 11.

Ensure that the communications baud rate and parity settings in the application software are set the same as those in the relay. The relay's Courier address in cell [0E90: COMMUNICATIONS, RP2 Address] must be set to a value between 1 and 254. The second rear communication's port configuration [0E88: COMMUNICATIONS RP2 Port Config] must be set to EIA(RS)232.

Check that communications can be established with this relay using the portable PC.

5.2.13 Current Inputs

This test verifies that the accuracy of current measurement is within acceptable tolerances.

All relays leave the factory set for operation at a system frequency of 50 Hz. If operation at 60 Hz is required, this must be set in cell [0009: SYSTEM DATA, Frequency].

To avoid spurious operation of protection elements during injection testing, ensure that current operated elements are disabled.

Apply current equal to the line current transformer secondary winding rating to each current transformer input of the corresponding rating in turn, checking its magnitude using a multimeter. Refer to Table 12 for the corresponding reading in the relay's **MEASUREMENTS 1** columns, as appropriate, and record the value displayed.

Menu cell	Apply current to		
	P642 (40TE)	P643 (60TE)	P645 (60TE/80TE)
	1A/5A CTs	1A/5A CTs	1A/5A CTs
[0201: MEASUREMENTS 1, IA1 Magnitude]	D24-D23	D24-D23	D24-D23
[0203: MEASUREMENTS 1, IB1 Magnitude]	D26-D25	D26-D25	D26-D25
[0205: MEASUREMENTS 1, IC1 Magnitude]	D28-D27	D28-D27	D28-D27

Menu cell	Apply current to		
	P642 (40TE)	P643 (60TE)	P645 (60TE/80TE)
	1A/5A CTs	1A/5A CTs	1A/5A CTs
[0207: MEASUREMENTS 1, IA2 Magnitude]	D18-D17	D18-D17	D18-D17
[0209: MEASUREMENTS 1, IB2 Magnitude]	D20-D19	D20-D19	D20-D19
[020B: MEASUREMENTS 1, IC2 Magnitude]	D22-D21	D22-D21	D22-D21
[020D: MEASUREMENTS 1, IA3 Magnitude]		F24-F23	F24-F23
[020F: MEASUREMENTS 1, IB3 Magnitude]		F26-F25	F26-F25
[0211: MEASUREMENTS 1, IC3 Magnitude]		F28-F27	F28-F27
[0213: MEASUREMENTS 1, IA4 Magnitude]			F18-F17
[0215: MEASUREMENTS 1, IB4 Magnitude]			F20-F19
[0217: MEASUREMENTS 1, IC4 Magnitude]			F22-F21
[0219: MEASUREMENTS 1, IA5 Magnitude]			F12-F11
[021B: MEASUREMENTS 1, IB5 Magnitude]			F14-F13
[021D: MEASUREMENTS 1, IC5 Magnitude]			F16-F15
[0265: MEASUREMENTS 1, IN-HV Measured Magnitude]	D16-D15	D16-D15	D16-D15
[026C: MEASUREMENTS 1, IN-LV Measured Magnitude]	D14-D13	D14-D13	D14-D13
[0273: MEASUREMENTS 1, IN-TV Measured Magnitude]		D12-D11	D12-D11

Table 12 - Current input terminals

The measured current values displayed on the relay LCD, or on a portable PC connected to the front communication port, are either in primary or secondary Amperes. If cell [0D02: MEASURE’T SETUP, Local Values] is set to **Primary**, the values displayed should be equal to the applied current multiplied by the corresponding current transformer ratio set in the **CT and VT RATIOS** menu column (see Table 13). If cell [0D02: MEASURE’T SETUP, Local Values] is set to **Secondary**, the value displayed should be equal to the applied current.

Note *If a PC connected to the relay’s rear communications port is used to display the measured current, the process is similar. However, the setting of cell [0D03: MEASURE’T SETUP, Remote Values] determines whether the displayed values are in primary or secondary Amperes.*

The measurement accuracy of the relay is ±1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

Next check that all three phase CTs associated with one winding are of the same polarity, the same current should be applied to phases A, B, and C - phase displaced as for a balanced 3-phase set. This is for phase angles $\angle A = 0^o$, $\angle B = -120^o$, $\angle C = 120^o$, for a standard ABC phase rotation system. Starting from current bias input 1, apply the balanced current and check the measured residual current in the cell [IN-HV Deriv Mag], [IN-LV Deriv Mag], or [IN-TV Deriv Mag] depending on the transformer winding to which the current input is assigned. The residual current measured should be less than 0.05 p.u. If high residual current is measured, one or more of the CT circuits for the end concerned may have a problem (for example, an inverted connection). Repeat the same test on the rest of the current bias inputs.

Menu cell	Corresponding CT ratio (in VT and CT RATIO column (0A) of menu)
[0201: MEASUREMENTS 1, IA1 Magnitude] [0203: MEASUREMENTS 1, IB1 Magnitude] [0205: MEASUREMENTS 1, IC1 Magnitude]	[0A12: Phase CT Primary] [0A13: Phase CT Sec'y]
[0207: MEASUREMENTS 1, IA2 Magnitude] [0209: MEASUREMENTS 1, IB2 Magnitude] [020B: MEASUREMENTS 1, IC2 Magnitude]	[0A16: Phase CT Primary] [0A17: Phase CT Sec'y]
[020D: MEASUREMENTS 1, IA3 Magnitude] [020F: MEASUREMENTS 1, IB3 Magnitude] [0211: MEASUREMENTS 1, IC3 Magnitude]	[0A1A: Phase CT Primary] [0A1B: Phase CT Sec'y]
[0213: MEASUREMENTS 1, IA4 Magnitude] [0215: MEASUREMENTS 1, IB4 Magnitude] [0217: MEASUREMENTS 1, IC4 Magnitude]	[0A1E: Phase CT Primary] [0A1F: Phase CT Sec'y]
[0219: MEASUREMENTS 1, IA5 Magnitude] [021B: MEASUREMENTS 1, IB5 Magnitude] [021D: MEASUREMENTS 1, IC5 Magnitude]	[0A22: Phase CT Primary] [0A23: Phase CT Sec'y]
[0265: MEASUREMENTS 1, IN-HV Measured Magnitude]	[0A5A: E/F CT Primary] [0A5B: E/F CT Sec'y]
[026C: MEASUREMENTS 1, IN-LV Measured Magnitude]	[0A5F: E/F CT Primary] [0A60: E/F CT Sec'y]
[0273: MEASUREMENTS 1, IN-TV Measured Magnitude]	[0A64: E/F CT Primary] [0A65: E/F CT Sec'y]

Table 13 - CT ratio settings

5.2.14 Voltage Inputs

This test verifies that the accuracy of voltage measurement is within the acceptable tolerances.

Apply rated voltage to each voltage transformer input in turn, checking its magnitude using a multimeter. Refer to Table 14 for the corresponding reading in the relay's **MEASUREMENTS 1** column and record the value displayed.

Menu cell	Voltage applied to		
	P642 (40TE)	P643 (60TE)	P645 (60TE/80TE)
[028F: MEASUREMENTS 1, VAN Magnitude]		D2-D1	D2-D1
[0291: MEASUREMENTS 1, VBN Magnitude]		D4-D3	D4-D3
[0293: MEASUREMENTS 1, VCN Magnitude]		F2-F1	F2-F1
[0295: MEASUREMENTS 1, VX Measured Mag]		F4-F3	F4-F3
[0295]: MEASUREMENTS 1, VX Measured Mag] [029C]: MEASUREMENTS 1, VAB Measured Mag]	C4-C3		
[029E]: MEASUREMENTS 1, VBC Measured Mag]	C2-C1		

Table 14 - Voltage input terminals

The measured voltage values displayed on the relay LCD or a portable PC connected to the front communication port are either in primary or secondary volts. If cell [0D02: MEASURE'T SETUP, Local Values] is set to **Primary**, the values displayed should be equal to the applied voltage multiplied by the corresponding voltage transformer ratio set in the **VT and CT RATIOS** menu column (see Table 15). If cell [0D02: MEASURE'T SETUP, Local Values] is set to **Secondary**, the value displayed should be equal to the applied voltage.

Note	*If a PC connected to the relay's rear communications port is used to display the measured voltage, the process is similar. However, the setting of cell [0D03: MEASURE'T SETUP, Remote Values] determines whether the displayed values are in primary or secondary volts.*

The measurement accuracy of the relay is ±1%. However, an additional allowance must be made for the accuracy of the test equipment being used.

Menu cell	Corresponding VT ratio (in "VT and CT RATIO" Column (0A) of Menu)
[021A: MEASUREMENTS 1, VAN Magnitude] [021C: MEASUREMENTS 1, VBN Magnitude] [021E: MEASUREMENTS 1, VCN Magnitude]	[0A03: Main VT Primary] [0A04: Main VT Sec'y]
[0220: MEASUREMENTS 1, VX Measured Mag]	[0A07: VX VT Primary] [0A08: VX VT Sec'y]

Table 15 - VT ratio settings

6 SETTING CHECKS

The setting checks ensure that all of the application-specific relay settings (both the relay’s function and Programmable Scheme Logic (PSL) settings) for the particular installation have been correctly applied to the relay.

Important **If the application-specific settings are not available, ignore sections 6.1 and 6.2.**

Note *The trip circuit should remain isolated during these checks to prevent accidental operation of the associated circuit breaker.*

6.1 Apply Application-Specific Settings

There are different methods of applying the settings:

- Transferring settings from a pre-prepared setting file to the relay using a portable PC running the appropriate software (MiCOM S1 Studio) use the relay’s front EIA(RS)232 port, under the bottom access cover, or the first rear communications port (Courier protocol with a KITZ protocol converter connected), or the second rear communications port. This is the preferred method for transferring function settings as it is much faster and there is less margin for error. If PSL other than the default settings with which the relay is supplied is used, this is the only way of changing the settings.
- If a setting file has been created for the particular application and provided on a diskette, the commissioning time is further reduced, especially if application-specific PSL is applied to the relay.
- Enter the settings manually using the relay’s operator interface. This method is not suitable for changing the PSL.

Caution **When the installation needs application-specific Programmable Scheme Logic (PSL), it is essential that the appropriate .psl file is downloaded (sent) to the relay, for each setting group that will be used. If the user fails to download the required .psl file to any setting group that may be brought into service, the factory default PSL will still be resident. This may have severe operational and safety consequences.**

6.2 Check Application-Specific Settings

Carefully check applied settings against the required application-specific settings to ensure they have been entered correctly. However, this is not considered essential if a customer-prepared setting file on diskette has been transferred to the relay using a portable PC.

There are two methods of checking the settings:

- Extract the settings from the relay using a portable PC running the appropriate software (MiCOM S1 Studio) using the front EIA(RS)232 port, under the bottom access cover, or the first rear communications port (Courier protocol with a KITZ protocol converter connected), or the second rear communications port. Compare the settings transferred from the relay with the original written application-specific setting record (for cases where the customer has only provided a printed copy of the required settings but a portable PC is available).

- Step through the settings using the relay’s operator interface and compare them with the original application-specific setting record.

Unless previously agreed to the contrary, the application-specific PSL is not checked as part of the commissioning tests.

Due to the versatility and possible complexity of the PSL, it is beyond the scope of these commissioning instructions to detail suitable test procedures. Therefore, when PSL tests must be performed, written tests that satisfactorily demonstrate the correct operation of the application-specific scheme logic should be devised by the engineer who created it. These tests should be provided to the Commissioning Engineer with the diskette containing the PSL setting file.

6.3 Demonstrate Correct Relay Operation

Tests 4.2.9 and 4.2.10 have already demonstrated that the relay is within calibration, so the purpose of these tests is as follows:

- To confirm that the primary protection function of the P643/P644/P645 relay, the current differential protection, can trip according to the correct application settings.
- To verify correct setting of the backup phase overcurrent protection (P642/P643/P645).
- To verify correct assignment of the trip contacts, by monitoring the response to a selection of fault injections.

6.4 Transformer Differential Protection (P642/P643/P645)

To avoid spurious operation of any other protection elements, all protection elements except the transformer differential protection should be disabled for the duration of the differential element tests. This is done in the relay’s **CONFIGURATION** column. Make a note of which elements need to be re-enabled after testing.

The P642/P643/P645 transformer differential protection has three elements, one for each phase. The biased differential protection uses the maximum bias current in the three phases to bias the elements. The detailed bias characteristic is described in the *Operation* chapter *P64x/EN OP*.

6.4.1 Low Set Element Current Sensitivity (Is1)

Connect the equipment so that current can be injected through terminals D24 and D23. Slowly increase the current from 0 Amps and note the pick-up value at which the relay operates. Reduce the current slowly and note the drop-off value at which it resets. Check that the pick-up and drop-off are within the range shown in Table 16.

In Table 16 below, $I = \dfrac{I_{s1}}{amplitude \quad matching \quad factor}$

Is1 is the low set setting which will be found in the cell [Is1] under the **GROUP 1 DIFF PROTECTION** menu heading. The amplitude matching factor is used to compensate for a mismatch in currents due to the line side current transformer ratios. There is one amplitude matching factor for the HV side, which is in the cell [Match Factor HV], one for the LV side found in the cell [Match Factor LV], and one for the TV side found in the cell [Match Factor TV]. These are under the **GROUP 1 SYSTEM CONFIG** menu heading. Use the appropriate amplitude matching factor to calculate the current to inject: this depends on whether it is being injected into the HV, LV, or TV current transformer inputs.

	Current level
Pick-up	0.90 x I to 1.1 x I

	Current level
Drop-off	0.90 x pick-up to 1 x pick-up

Table 16 - Low set element pick-up and drop-off

Repeat the above test for each of the remaining phases on the HV side, and for all three phases on the LV and TV sides. These are shown in Table 22.

As the CT inputs to each phase have been verified by both the measurement checks and the low set differential trip checks, it is only necessary to check the operating time and the high set current sensitivity for each phase element on one side of the transformer only.

6.4.2 Low Set Element Operating Time

Connect the relay so that current can be injected through terminals D24 and D23, but in addition connect the relay contacts for this protection function to both trip the test set and to stop a timer. Configure the test set so that when the current is applied to the relay, the timer starts.

Inject 5 x I into the HV side A phase (terminals D24 & D23). Check that the operating time for the relay is within the range 30 ms to 35 ms. Repeat this test for both the remaining phases on the HV side, as shown in Table 12.

6.4.3 High Set Element Current Sensitivity (Is HS1)

Caution **The relay may be damaged by applying excessive current for long durations during testing, or in recurrent bursts without allowing time for the relay to cool down.**

This test checks the instantaneous current sensitivity of the differential high set element. This test can only be performed if the test set can inject sufficient current into the relay to cause the element to trip at the calculated application setting.

The relay should be connected so that current can be injected through terminals D24 and D23. Also the output relay configured as Idiff HS1 Trip A (DDB 903) should be connected to trip the test set and to stop a timer.

Caution **It is important to trip the test set to avoid sustained application of excessive currents.**

It is recommended that the low set differential is still enabled during this test. The timer should be started when the current is applied to the relay. As the setting is above the continuous current rating of the relay, DO NOT INCREASE THE CURRENT SLOWLY, since this may damage the relay before it can operate. Instead, set the current level then suddenly apply it. Two tests have to be performed for this particular protection function. These are shown in Table 17.

Is HS1 (Trip)	Is HS1 (No Trip)
1.1 x I	0.90 x I

Table 17 - High set element sensitivity

The first test to be performed is at the higher current level, to check that the instantaneous element operates.

In Table 17, $I = \frac{Is\ \ HS1}{amplitude\ \ matching\ \ factor}$

Is HS1 is the high set setting which is in the cell [Is HS1] under the **GROUP 1 DIFF PROTECTION** menu heading. The amplitude matching factor is used to compensate for a mismatch in currents due to the line side current transformer ratios. This is found in the cell [Match Factor HV] under the **GROUP 1 SYSTEM CONFIG** menu heading.

Inject 1.1 x I and ensure that the selected output relay operates.

Caution	**For the second test it is important that the current is not applied for longer than one second.**

Inject 0.9 x I for one second and ensure that the selected output relay does not operate. Repeat the above two tests for the two remaining elements of the HV side of the transformer as shown in Table 12.

6.4.4 High Set Element Operating Time

This test can only be performed if the test set can inject sufficient current into the relay to cause the element to trip at the calculated application setting. Connect the relay so that current can be injected through terminals D24 and D23, but in addition connect the relay contacts for this protection function to both trip the test set and to stop a timer. Configure the test set so that when the current is applied to the relay, the timer starts. Inject 3 x I into the HV side A phase terminals D24 and D23. Check that the operating time for the relay is within the range 10 ms to 15 ms.

Repeat this test for both of the remaining phases on the HV side, as shown in Table 12.

6.4.5 Differential through Fault Stability by Primary Injection

To check for through fault stability, it is preferable, especially for a new transformer installation to simulate a through-fed external fault, by a real primary fault simulation. This is achieved by placing a three-phase bolted short circuit on the downstream side of the LV CTs, and energizing the HV winding from a three-phase medium voltage supply. Typically, the HV winding is energized only from a voltage rated in the range 400 to 440 V, to limit the through fault current. In such a through fault situation, the relay should not trip.

Note The procedure for primary testing is not covered here, as it must respect utility safety rules, permits to work, and sanctions for testing.

6.4.6 CT Secondary Wiring Differential through Fault Stability Test by Secondary Injection

Secondary injection can be used to verify settings. For a two-winding transformer, a fault current flowing out of the LV side is simulated, with a balancing set of currents on one or two phases flowing into the HV side. If all settings and CT orientations are correct, no trip should occur, and minimal differential current are measured by the relay. For a relay with more than two bias inputs (P643 and P645 models), the external fault injection must be repeated for each additional set of CT inputs. For example, when a P643 is used to protect a three-winding transformer, there should be an injection for a through-fed fault Terminal 1 CT to Terminal 2 CT, then afterwards for Terminal 1 CT to Terminal 3 CT. When using a P643 to protect a two-winding transformer or a P645, it should be checked in [HV CT Terminals], [LV CT Terminals] and [TV CT Terminals] under the **GROUP 1 SYSTEM CONFIG** menu heading which CT inputs are configured to each transformer winding. The injection of through-fed faults is between CTs assigned to different transformer windings.

Caution	**During these tests, disable all the current operated protection functions except the differential protection. Make a note of all the functions that must be enabled after the testing is completed.**

6.4.6.1 Yy Transformers and Autotransformer

This test simulates current flowing through the transformer to an external fault.

Consider a two-winding transformer application, and that Terminal 1 CT (D23, D24) is assigned to the HV winding and Terminal 5 CT (F11, F12) is assigned to the LV winding. A fault current is injected, flowing out of phase A at Terminal 5 CT. The same zero sequence filtering setting is applied for the HV and LV windings; therefore, if the current simulated is 1 pu out of Terminal 5 CT, the input current to balance at Terminal 1 CT is also 1 pu.

Connect the test equipment as shown in Figure 3 for a Yy0 transformer connection:

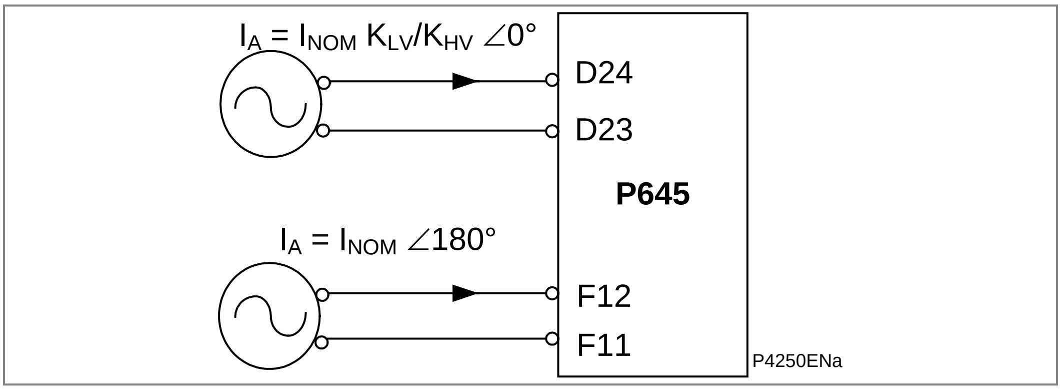

$I_A = I_{NOM}\ K_{LV}/K_{HV}\ \angle 0°$
D24
D23
P645
$I_A = I_{NOM}\ \angle 180°$
F12
F11
P4250ENa

Figure 3 - Test equipment connection for a Yy0 transformer

A single phase current equal to the CT secondary rating (1 A or 5 A) is simulated to flow OUT on phase A, Terminal 5 CT. On an automatic test set, use $I_{NOM}\ \angle 180^o$.

To balance, a current is applied to one phase input at Terminal 1 CT. The magnitude should be a current equal to $(K_{LV} / K_{HV}) \times I_{NOM}$, and at a phase angle as shown in Table 18:

	Terminal 5 CT injected phase	LV current terminal 5 CT	Terminal 1 CT injected phase	HV current terminal 1 CT
Yy0, Autotrans former	A	$I_{NOM}\ \angle 180^o$	A	$I_{NOM} . K_{LV} / K_{HV}\ \angle 0^o$
Yy2	A	$I_{NOM}\ \angle 180^o$	C	$I_{NOM} . K_{LV} / K_{HV}\ \angle 180^o$
Yy4	A	$I_{NOM}\ \angle 180^o$	B	$I_{NOM} . K_{LV} / K_{HV}\ \angle 0^o$
Yy6	A	$I_{NOM}\ \angle 180^o$	A	$I_{NOM} . K_{LV} / K_{HV}\ \angle 180^o$
Yy8	A	$I_{NOM}\ \angle 180^o$	C	$I_{NOM} . K_{LV} / K_{HV}\ \angle 0^o$
Yy10	A	$I_{NOM}\ \angle 180^o$	B	$I_{NOM} . K_{LV} / K_{HV}\ \angle 180^o$

Table 18 - Injected current for Yy ends

The amplitude matching factors K_{HV} and K_{LV} can be found in [Match Factor HV] and [Match Factor LV] respectively under the **GROUP 1 SYSTEM CONFIG** menu heading.

Apply the fault currents for approximately one second. If end Terminal 1 CT and Terminal 5 CT are in the correct orientation no trip should occur. It is important to read the displayed differential currents [IA Differential], [IB Differential] and [IC Differential] under **MEASUREMENT 3** menu heading to check that these measurements are low. These measurements must show less than 0.1 pu (10%), to prove that a balance is achieved.

The reason that the differential currents must be read is that in certain busbar applications the Idiff> trip threshold may be set *higher* than Inom, so that even an incorrect CT connection would not cause a trip.

It is not necessary to repeat the injection for other phases, because their orientation has already been checked in *section 5.2.13, Current Inputs*.

Figure 4 shows the transformer connections for the configurations shown in Table 18.

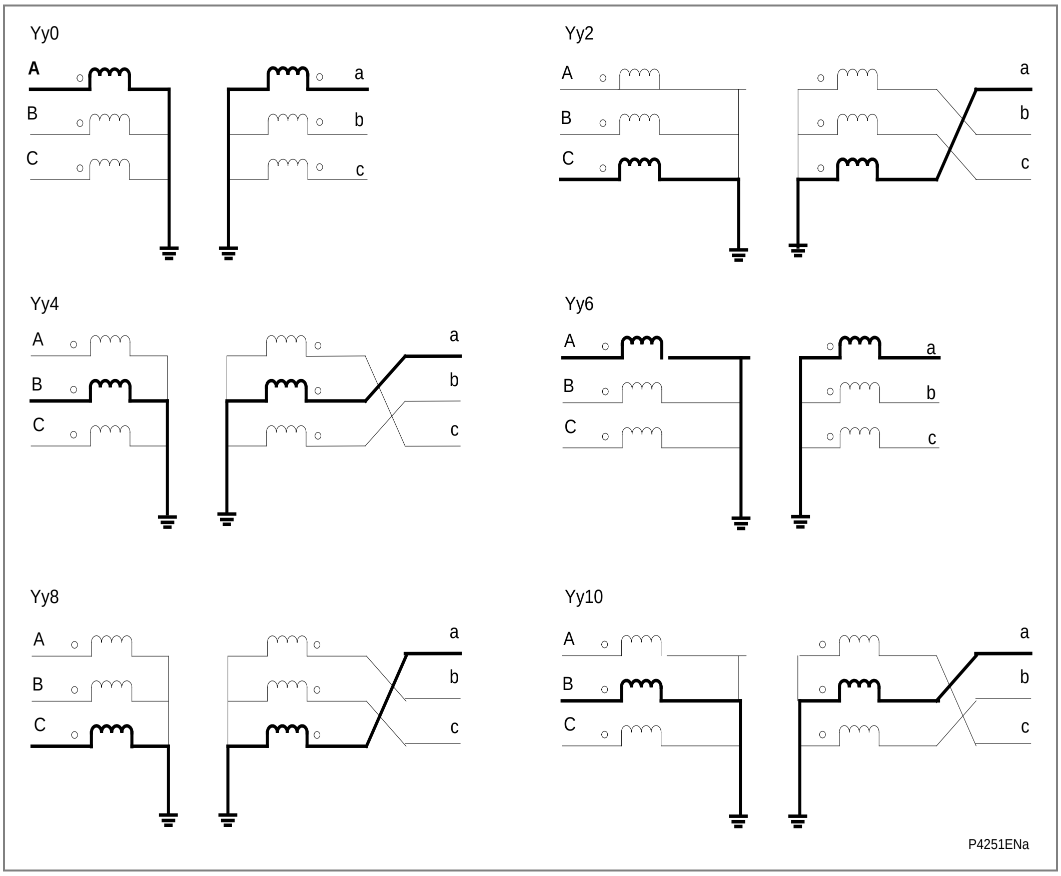


Figure 4 - Yy transformer connections

6.4.6.2 Dy and Yd Applications

This test simulates current flowing through the transformer to an external fault.

A fault current flowing out of the A phase on whichever winding is the star (wye) end is injected. For a Dy configuration it is the LV side, for a Yd configuration it is the HV side. The star winding phase A shares the same power transformer limb as two phases on the opposite side, so that a two-phase current loop needs to be injected to achieve a balance.

For ease of injection, a single phase current equal to the CT secondary rating (1 A or 5 A) is simulated to flow OUT on phase A of the wye end. On an automatic test set, use $I_{NOM} \angle 180^o$. To balance, a current is applied to two phase CT inputs (delta side). Table 19 shows the currents to be injected. The magnitude should be a current equal to $[K_{wye} / (\sqrt{3}.K_{delta})] \times I_{NOM}$, and at the phase angles as shown in Table 19:

	Star end injected phase	Current (Star)	Delta side injected loop	Current
Dy1 or Yd11	A	$I_{NOM} \angle 180^o$	A-C	$I_A = I_{NOM} . K_{WYE} / \sqrt{3}K_{DELTA} \angle 0^o$ $I_C = I_{NOM} . K_{WYE} / \sqrt{3}K_{DELTA} \angle 180^o$
Dy3 or Yd9	A	$I_{NOM} \angle 180^o$	C-B	$I_C = I_{NOM} . K_{WYE} / \sqrt{3}K_{DELTA} \angle 0^o$ $I_B = I_{NOM} . K_{WYE} / \sqrt{3}K_{DELTA} \angle 180^o$

	Star end injected phase	Current (Star)	Delta side injected loop	Current
Dy5 or Yd7	A	$I_{NOM} \angle 180^o$	A-B	$I_A = I_{NOM} . K_{WYE} / \sqrt{3}K_{DELTA} \angle 0^o$ $I_B = I_{NOM} . K_{WYE} / \sqrt{3}K_{DELTA} \angle 180^o$
Dy7 or Yd5	A	$I_{NOM} \angle 180^o$	A-C	$I_A = I_{NOM} . K_{WYE} / \sqrt{3}K_{DELTA} \angle 0^o$ $I_C = I_{NOM} . K_{WYE} / \sqrt{3}K_{DELTA} \angle 180^o$
Dy9 or Yd3	A	$I_{NOM} \angle 180^o$	B-C	$I_B = I_{NOM} . K_{WYE} / \sqrt{3}K_{DELTA} \angle 0^o$ $I_C = I_{NOM} . K_{WYE} / \sqrt{3}K_{DELTA} \angle 180^o$
Dy11 or Yd1	A	$I_{NOM} \angle 180^o$	A-B	$I_A = I_{NOM} . K_{WYE} / \sqrt{3}K_{DELTA} \angle 0^o$ $I_B = I_{NOM} . K_{WYE} / \sqrt{3}K_{DELTA} \angle 180^o$

Table 19 - Injected current for delta-star ends

For a Yd1 configuration, connect the test equipment as shown in Figure 5.

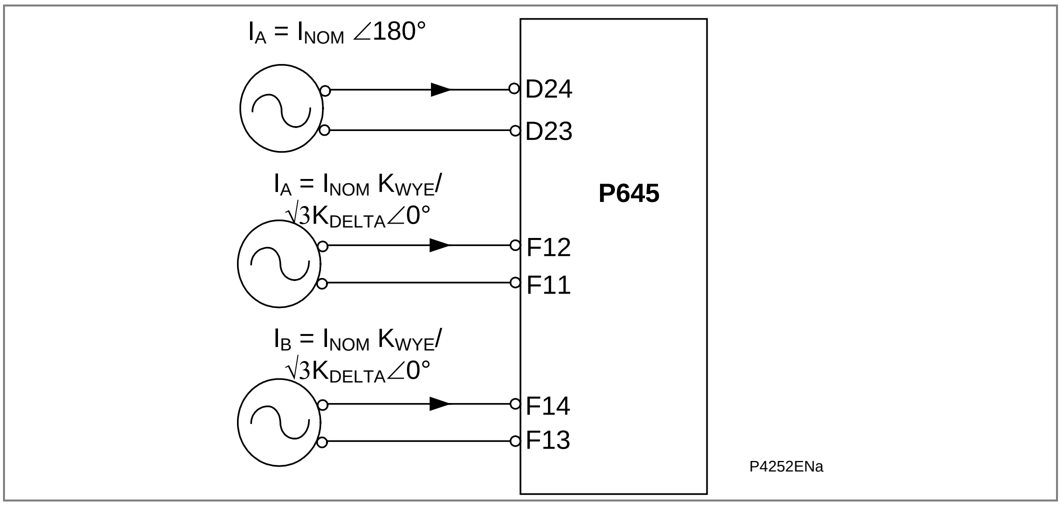

$I_A = I_{NOM} \angle 180°$
D24
D23
P645
$I_A = I_{NOM} K_{WYE} / \sqrt{3}K_{DELTA} \angle 0°$
F12
F11
$I_B = I_{NOM} K_{WYE} / \sqrt{3}K_{DELTA} \angle 0°$
F14
F13
P4252ENa

Figure 5 - Test equipment connection for a Yd1 transformer

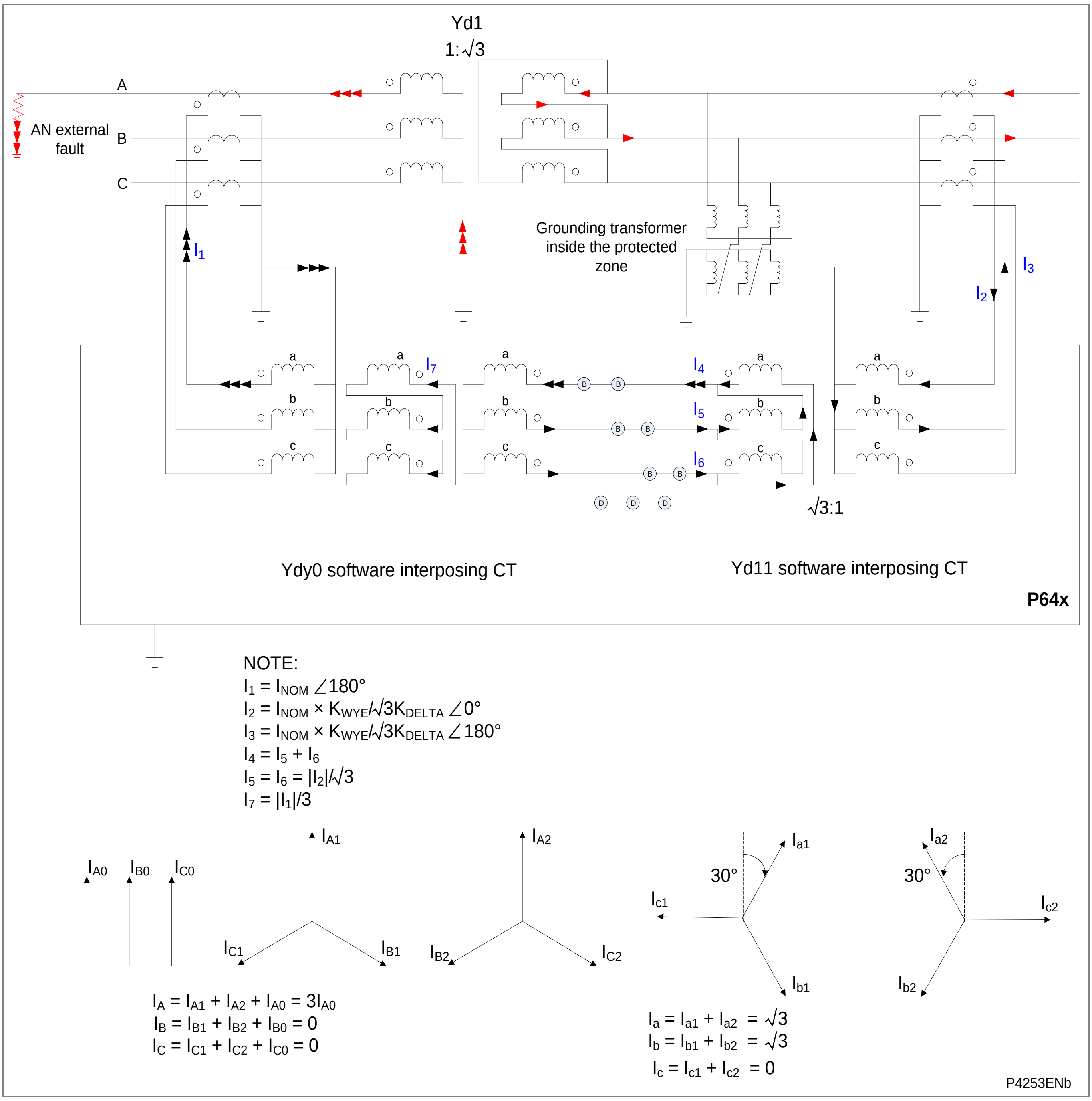
The amplitude matching factors K_{wye} and K_{delta} can be found in [Match Factor HV] and [Match Factor LV] under the **GROUP 1 SYSTEM CONFIG** menu heading

The delta side loop current may be applied as two separate current outputs from a test set, or one current looped out through the first phase specified, and returning back through the latter phase input.

Apply the fault currents for approximately one second. If end Terminal 1 CT and Terminal 5 CT are in the correct orientation no trip should occur. It is important to read the displayed differential currents [IA Differential], [IB Differential] and [IC Differential] under the **MEASUREMENT 3** menu heading to check that these measurements are low. These measurements must show less than 0.1 p.u. (10%), to prove that a balance is achieved.

It is not necessary to repeat the injection for other phases, because their orientation has already been checked in *section 5.2.13, Current Inputs*.

Figure 6 shows a Yd9 transformer with the current distribution for an AN external fault on the Y side of the transformer. During the test shown in Figure 5, the following current distribution occurs in the P64x.


Yd1
1:√3
A
AN external fault
B
C
I1
Grounding transformer inside the protected zone
I3
I2
a
b
c
I7
I4
I5
I6
√3:1
B
D
Ydy0 software interposing CT
Yd11 software interposing CT
P64x
IA0
IB0
IC0
IA1
IB1
IC1
IA2
IB2
IC2
30°
Ia1
Ib1
Ic1
30°
Ia2
Ib2
Ic2
P4253ENb

NOTE:

$I_1 = I_{NOM} \angle 180°$

$I_2 = I_{NOM} \times K_{WYE}/\sqrt{3}K_{DELTA} \angle 0°$

$I_3 = I_{NOM} \times K_{WYE}/\sqrt{3}K_{DELTA} \angle 180°$

$I_4 = I_5 + I_6$

$I_5 = I_6 = |I_2|/\sqrt{3}$

$I_7 = |I_1|/3$

$I_A = I_{A1} + I_{A2} + I_{A0} = 3I_{A0}$

$I_B = I_{B1} + I_{B2} + I_{B0} = 0$

$I_C = I_{C1} + I_{C2} + I_{C0} = 0$

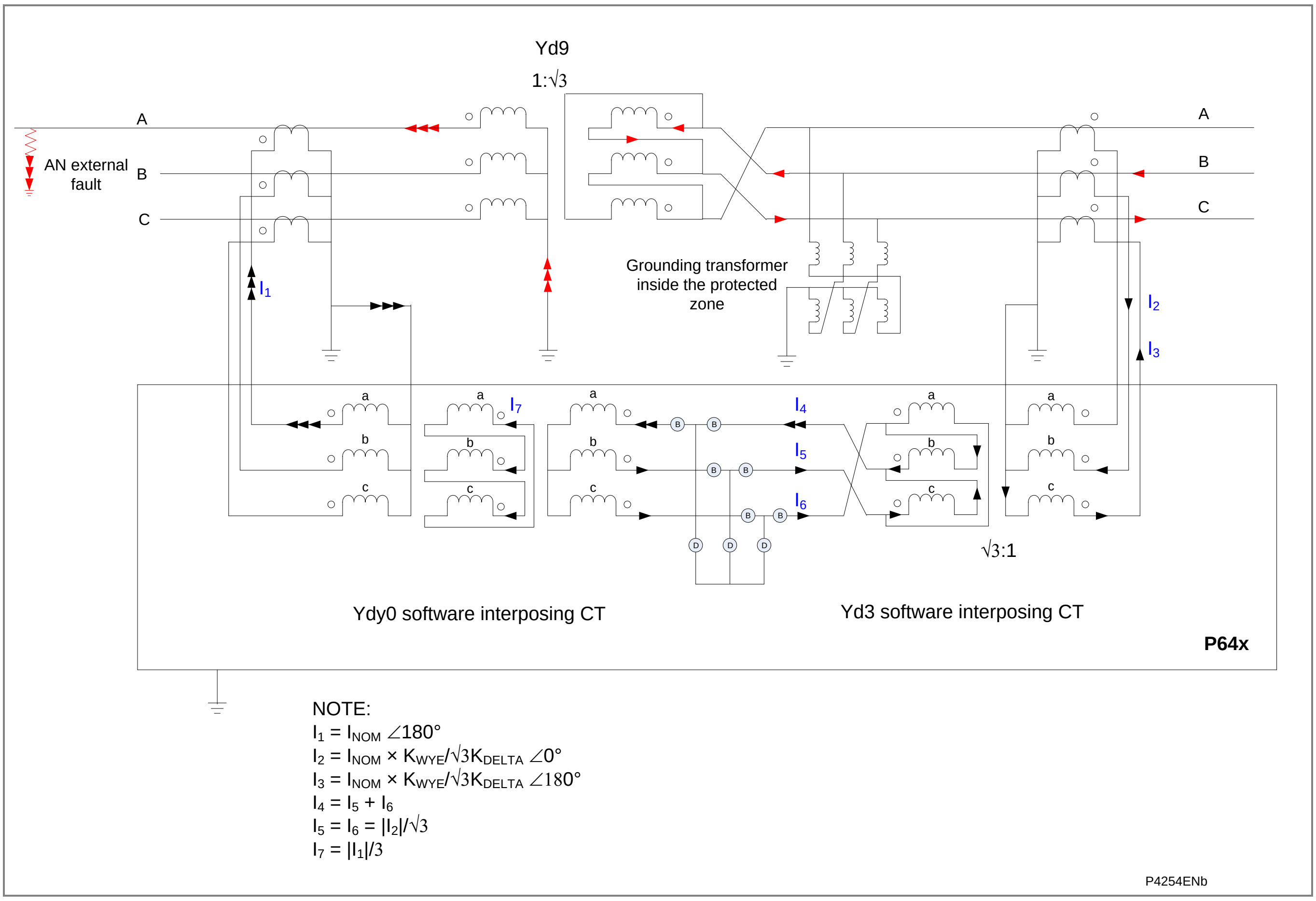
$I_a = I_{a1} + I_{a2} = \sqrt{3}$

$I_b = I_{b1} + I_{b2} = \sqrt{3}$

$I_c = I_{c1} + I_{c2} = 0$

Figure 6 - Yd9 configuration AN external fault current distribution

Figure 7 shows the transformer connections for the configurations shown in Table 19.


Yd9
1:√3
A
B
C
AN external fault
A
B
C
I1
I2
I3
Grounding transformer inside the protected zone
a
b
c
I7
I4
I5
I6
√3:1
Ydy0 software interposing CT
Yd3 software interposing CT
P64x
P4254ENb

NOTE:
$I_1 = I_{NOM} \angle 180°$
$I_2 = I_{NOM} \times K_{WYE}/\sqrt{3}K_{DELTA} \angle 0°$
$I_3 = I_{NOM} \times K_{WYE}/\sqrt{3}K_{DELTA} \angle 180°$
$I_4 = I_5 + I_6$
$I_5 = I_6 = |I_2|/\sqrt{3}$
$I_7 = |I_1|/3$

Figure 7 - Yd transformer connections

6.4.6.3 Dd Applications

This test simulates current flowing through the transformer to an external fault.

In many such applications, there may be in-zone earthing transformers, so it is easier to simulate an external phase-phase fault, to avoid simulating a zero sequence current. If Terminal 1 CT is assigned to the HV end and Terminal 5 CT to the LV end, and the current simulated is 1 pu out of Terminal 5 CT, the input current to balance at Terminal 1 CT is easy to determine. In the simplest application of a Dd0 transformer, an A-B fault is simulated flowing out of the LV side, fed by an A-B loop input on the HV side.

For ease of injection, a loop current equal to the CT secondary rating (1 A or 5 A) is simulated to flow OUT on phase A, Terminal 5 CT, and looping back through phase B, Terminal 5 CT. On an automatic test set, use $I_{NOM} \angle 180^o$. Because four-phase CT inputs to the relay are energized at once, it is necessary that the test set output current for this LV side is set as a single phase but looping through two phase CT inputs.

To balance, a loop current is applied at Terminal 1 CT (the HV winding). The magnitude should be a current equal to $(K_{LV}/K_{HV}) \times I_{NOM}$, and at a phase angle as shown below. The test set is configured to generate only one single phase output for this winding, looped through two phase CT inputs. Therefore in total, the output requirements can be satisfied by a test set typically having only up to three current outputs.

	Terminal 5 CT injected phase	LV current terminal 5 CT	Terminal 1 CT injected phase	HV current terminal 1 CT
Dd0	A-B	$I_{NOM} \angle 180^o$	A-B	$I_{NOM} . K_{LV} / K_{HV} \angle 0^o$
Dd2	A-B	$I_{NOM} \angle 180^o$	C-B	$I_{NOM} . K_{LV} / K_{HV} \angle 0^o$

	Terminal 5 CT injected phase	LV current terminal 5 CT	Terminal 1 CT injected phase	HV current terminal 1 CT
Dd4	A-B	$I_{NOM} \angle 180^o$	C-A	$I_{NOM} . K_{LV} / K_{HV} \angle 0^o$
Dd6	A-B	$I_{NOM} \angle 180^o$	B-A	$I_{NOM} . K_{LV} / K_{HV} \angle 0^o$
Dd8	A-B	$I_{NOM} \angle 180^o$	B-C	$I_{NOM} . K_{LV} / K_{HV} \angle 0^o$
Dd10	A-B	$I_{NOM} \angle 180^o$	A-C	$I_{NOM} . K_{LV} / K_{HV} \angle 0^o$

Table 20 - Current injected for Dd ends

The amplitude matching factors K_{HV} and K_{LV} can be found in [Match Factor HV] and [Match Factor LV] respectively under the GROUP 1 SYSTEM CONFIG menu heading.

For the Dd0 configuration, connect the test equipment as shown in Figure 8.

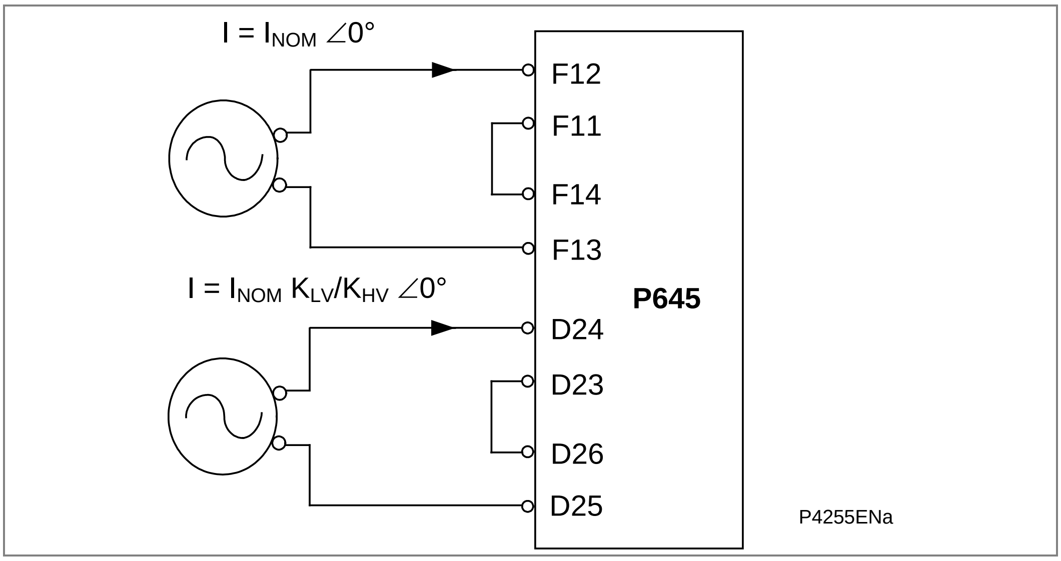


Figure 8 - Test equipment connection for a Dd0 transformer

Apply the fault currents for approximately one second. If end Terminal 1 CT and Terminal 5 CT are in the correct orientation no trip should occur. It is important to read the displayed differential currents [IA Differential], [IB Differential] and [IC Differential] under the **MEASUREMENT 2** menu heading to check that these measurements are low. These measurements must show less than 0.1 p.u. (10%), to prove that a balance is achieved.

It is not necessary to repeat the injection for other phases, because their orientation has already been checked in *section 5.2.13, Current Inputs*.

Figure 9 shows the transformer connections for the configurations shown in Table 20.

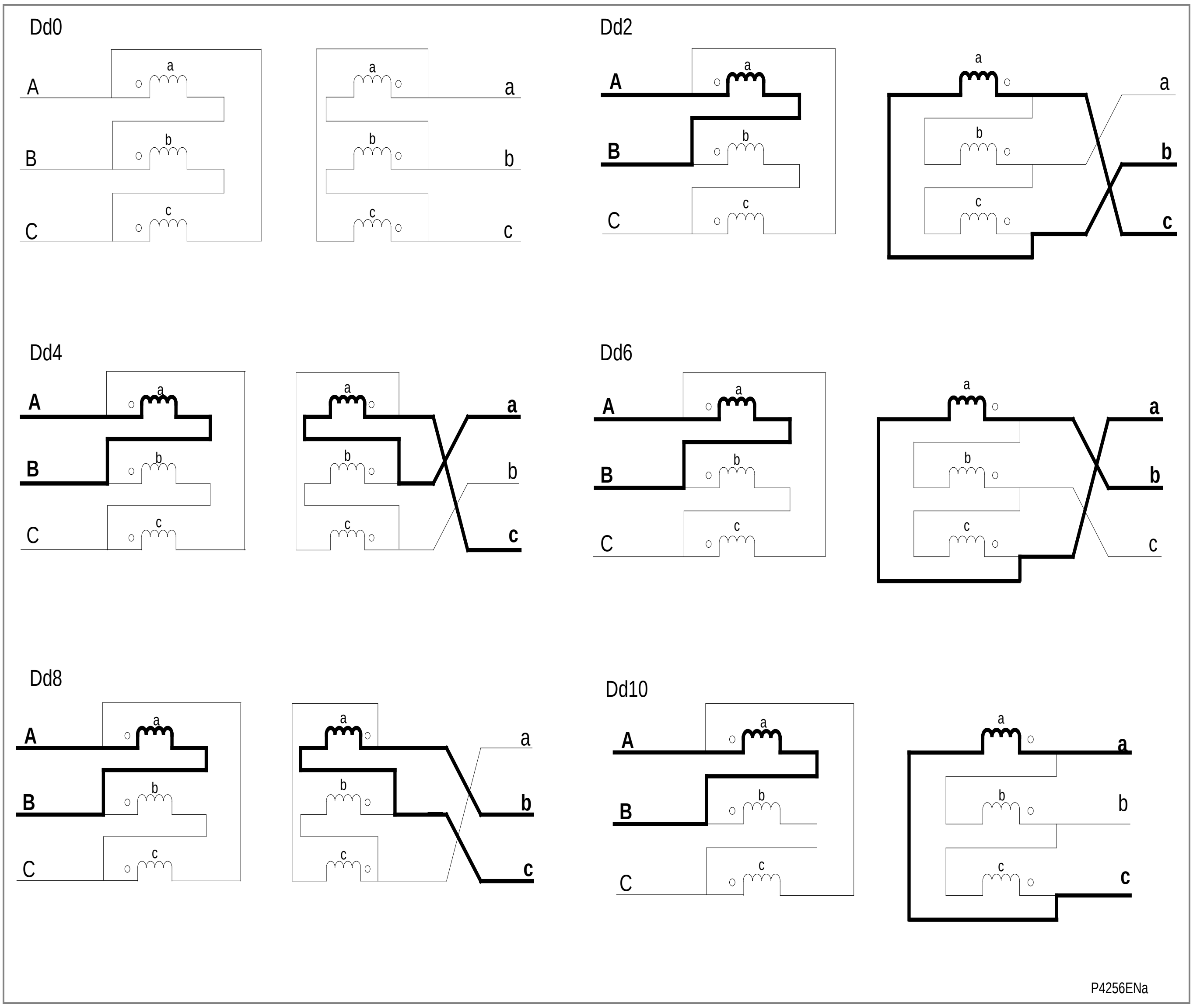


Figure 9 - Dd transformer connections

6.4.7 Low Set Element Bias Characteristic

This test checks the low set element bias characteristic. The relay has a three slope bias characteristic, therefore this test is performed at three points on the bias curve, one at 0% slope, at 30% slope, and at 80% slope, corresponding with bias currents of 0.4 p.u., 0.8 p.u., and 1.5 p.u. respectively.

If three LEDs have been assigned to give phase segregated trip information, Idiff Trip A, IDiff Trip B and IDiff Trip C (DDB 899, 900, 901), these may be used to indicate correct per-phase operation. If not, monitor options need to be used (see the next paragraph).

Go to the **COMMISSION TESTS** column in the menu, scroll down and change cells [0F07: Monitor Bit 1] to 899, [0F08: Monitor Bit 2] to 900 and [0F09: Monitor Bit 3] to 901. Cell [0F05: Test Port Status] will now appropriately set or reset the bits that now represent Phase A Trip (DDB 899), Phase B Trip (DDB 900) and Phase C Trip (DDB 901) with the rightmost bit representing Phase A Trip. From now on, monitor the indication of [0F05: Test Port Status].

It is important in this case that the injected currents are 180º out of phase. Connect the relay to the test equipment as shown in Figure 10.

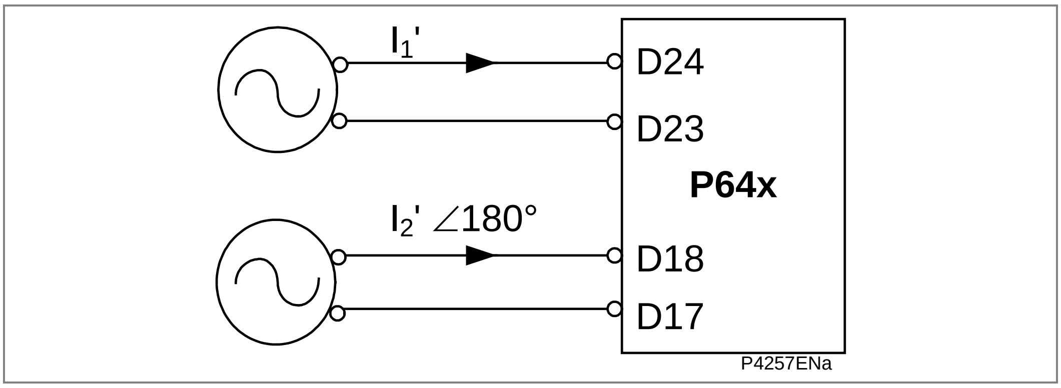


Figure 10 - Low set element bias characteristic test equipment connection

In total, six tests should be performed, one to cause the relay to trip and one to not cause the relay to trip, for the three sections of the bias curve. From Table 21, select the appropriate current values for each test, depending upon the setting and rating of the relay. Using the equations below, calculate the current values to apply to the relay, (I1’ and I2’). In all cases the current should be applied for no longer than one second, and should be within ±5% of the calculated values.

Error! Objects cannot be created from editing field codes.

Error! Objects cannot be created from editing field codes.

In (amps)	Is1 (pu)	0%				K1 = 30%				K2 = 80%			
		Trip		No trip		Trip		No trip		Trip		No trip	
		I1	I2	I1	I2	I1	I2	I1	I2	I1	I2	I1	I2
1	0.2	0.51	0.29	0.49	0.31	0.94	0.67	0.91	0.69	1.89	1.12	1.82	1.19
5	0.2	2.55	1.45	2.45	1.55	4.7	3.35	4.55	3.45	9.45	5.6	9.1	5.95

Table 21 - Low set element bias characteristic test

6.4.8 Second-Harmonic Blocking

This test checks that the second harmonic blocking is functioning, and it requires a current source capable of generating second-harmonic current. Once enabled, it blocks the low set differential element if the percentage of second harmonic over fundamental component per phase basis exceeds the setting Ih(2)%>.

To run the test, proceed as follows:

1. Connect two current test sources to one phase of any current bias input. Figure 11 shows the current sources connected to A phase of current bias input 1:

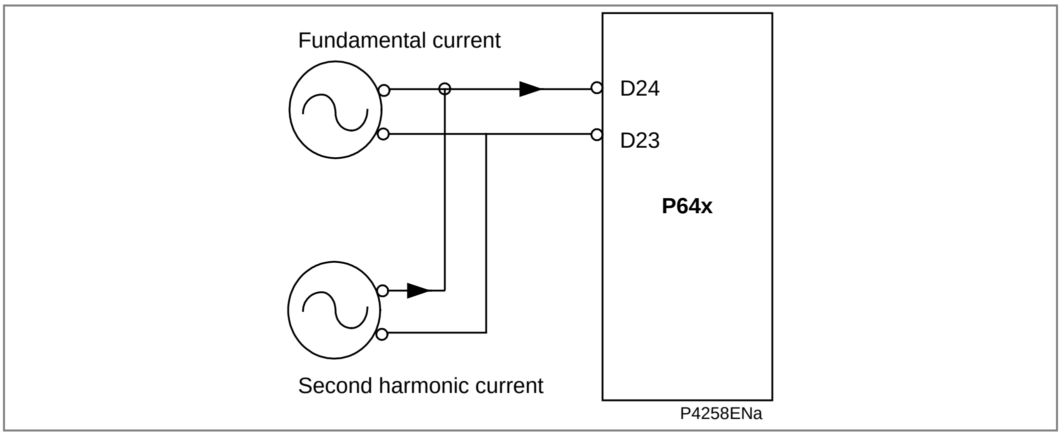


Figure 11 - Second harmonic test

2. Inject 4 x I of fundamental current, where:

   $$I = \frac{I_{s1}}{K_{CT1}}$$

   Is1 is the low set setting, K_{CT1} is the Terminal 1 CT amplitude matching factor which is used to compensate for a mismatch in currents due to the line side current transformer ratios. This is found in the cell [Match Factor HV] under the **GROUP 1 SYSTEM CONFIG** menu heading.
3. Ensure that Id Bias Trip A [DDB 909] asserts.
4. Apply and ramp up second-harmonic current to dropout the low set differential element.
5. Turn on the second current source for second-harmonic current (120 Hz if Frequency = 60 and 100 Hz if Frequency = 50). Starting at zero current, slowly increase the magnitude of this second current source until Id Bias Trip A [DDB 909] resets.
6. Note the value of the applied current from the second test source. The current from the second-harmonic source is shown by:

$$\text{Second harmonic current} = \frac{Ih(2)\%}{100} \times \text{ fundamental current } \pm 10\%$$

6.4.9 Fifth-Harmonic Blocking

This test checks that the fifth-harmonic blocking is functioning, and it requires a current source capable of generating fifth-harmonic current. Once enabled, it blocks the low set differential element if the percentage of second harmonic over fundamental component per phase basis exceeds the setting Ih(5)%>.

Connect two current test sources to one phase of any current bias input. Figure 12 shows the current sources connected to current bias input 1.

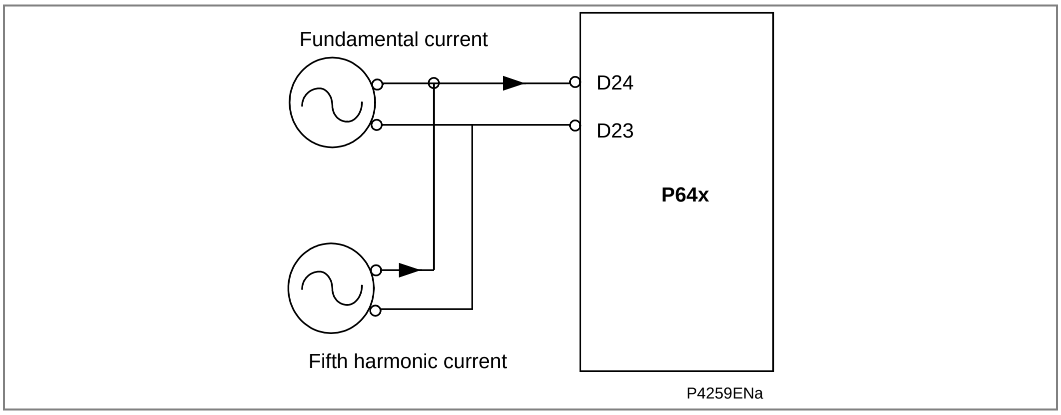


Figure 12 - Fifth-harmonic

Inject 4 x I of fundamental current, where:

$$I = \frac{I_{s1}}{K_{CT1}}$$

Is1 is the low set setting. K_{CT1} is the Terminal 1 CT amplitude matching factor which is used to compensate for a mismatch in currents due to the line side current transformer ratios. This is found in the cell [Match Factor HV] under the **GROUP 1 SYSTEM CONFIG** menu heading. Ensure that Id Bias Trip A [DDB 909] asserts.

Apply and ramp up fifth-harmonic current to dropout the low-set differential element. Turn on the second current source for fifth-harmonic current (300 Hz if Frequency = 60, 250 Hz if Frequency = 50). Starting at zero current, slowly increase the magnitude of this second current source until Id Bias Trip A [DDB 909] resets. Note the value of the applied current from the second test source. The current from the fifth-harmonic source is given by:

$$\text{Fifth harmonic current } = \frac{Ih(5)\%}{100} \times \text{ fundamental current } \pm 10\%$$

6.5 Restricted Earth Fault (REF) Setting Checks

6.5.1 Checking Restricted Earth Fault (REF) Sensitivity

These tests are performed on a per-winding basis, for all elements (REF HV, REF LV, REF TV) that are used in the application. The tripping sensitivity for the REF differential protection of one winding with a single end infeed is given by:

$$I = \frac{\text{n Is1 set}}{\text{scaling factor}}$$

n Is1 set: HV, LV, TV REF setting

Scaling factor = Neutral CTR / Line CTR

Apply a current slightly less than I to the I_Y (HV) CT input. Observe that no trip should occur, and the red Trip LED remains OFF.

Ramp up the current until a trip occurs and the Trip LED switches ON.

Record the current at which the relay tripped. The measured current should be within ± 10% of the HV Is1 setting.

Note	*If the REF provides low-impedance balanced earth fault protection for a delta winding, there is no I_Y input connected. In such cases, inject instead into the A phase CT input for the winding concerned. It may also be necessary to disable temporarily other protection elements that may trip, to view only the REF operation.*

Repeat the REF tests for each winding where it is implemented.

6.5.2 REF/BEF Primary Injection Tests

Primary injection tests are required to check that the current transformers are correctly connected.

Caution	**The procedure for primary testing must respect utility safety rules, permits to work and sanctions for testing. It is important that the primary injection test is undertaken for the REF function, because even stability with loadflow cannot be used as a test of REF stability. While balanced load is flowing, there is no way of knowing whether the star point-ground CT is correctly oriented. Therefore an installation might falsely appear correct on-load until there is an external earth fault on the system, and a maloperation could occur.**

6.5.2.1 Checking REF through Stability by Primary Injection

Where REF is providing *low-impedance* balanced earth fault protection for *delta* windings, no additional testing is required. This is because no I_Y CT input is connected, and all phase CT orientations have already been proven to be in the same sense for the differential protection.

In all applications to protect grounded star (wye) windings, it is not possible to prove that all CT inputs have the correct directionality, without a primary injection test.

To check for through stability, it is important, especially for a new transformer installation to simulate a through-fed external earth fault, by a primary fault simulation. This is achieved by temporarily shorting the entire A-phase winding to the star point, and then circulating fault current in a loop through the A-phase CT primary, the short, and the I_Y CT primary. In such a through-fault situation, the relay should not trip.

Before commencing any primary injection tests it is essential to ensure that the circuit is dead, isolated from the remainder of the system and that only those earth connections associated with the primary injection test equipment are in position.

The stability of the scheme can be checked by injecting through the neutral current transformer and each phase current transformer in turn. Figure 13 shows the connections for the P64x when the relays are used in a high-impedance differential scheme.

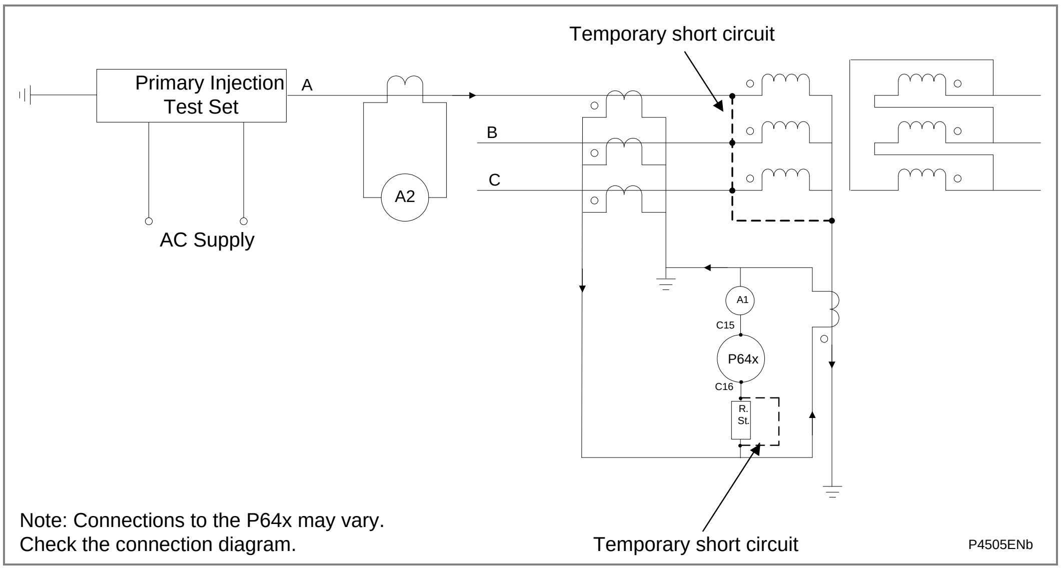

Temporary short circuit
Primary Injection Test Set
A
B
C
A2
AC Supply
A1
C15
P64x
C16
R. St.
Note: Connections to the P64x may vary.
Check the connection diagram.
Temporary short circuit
P4505ENb

Figure 13 - REF - Primary injection - stability test set up

During the stability test, it is necessary to measure the spill current in the relay circuit, therefore the stabilising resistor should be shorted out. The current should be increased up to as near full load as possible and the current flowing through ammeter A1 noted. If the connections are correct, this current would be very low, only a few milliamps. A high reading, (twice the injected current, referred through the current transformer ratio) indicates that one of the current transformer connections is reversed. This test should be repeated for the B-phase CT and neutral CT, and then for the C-phase CT and neutral CT.

The sensitivity of the protection can be checked by injecting with the single phase test set through each of the main current transformers in turn. This is shown in Figure 14. While carrying out this test it is advisable to measure the voltage across the relay coil and stabilizing resistance, and so to check the approximate voltage developed by the main current transformer to cause relay operation.

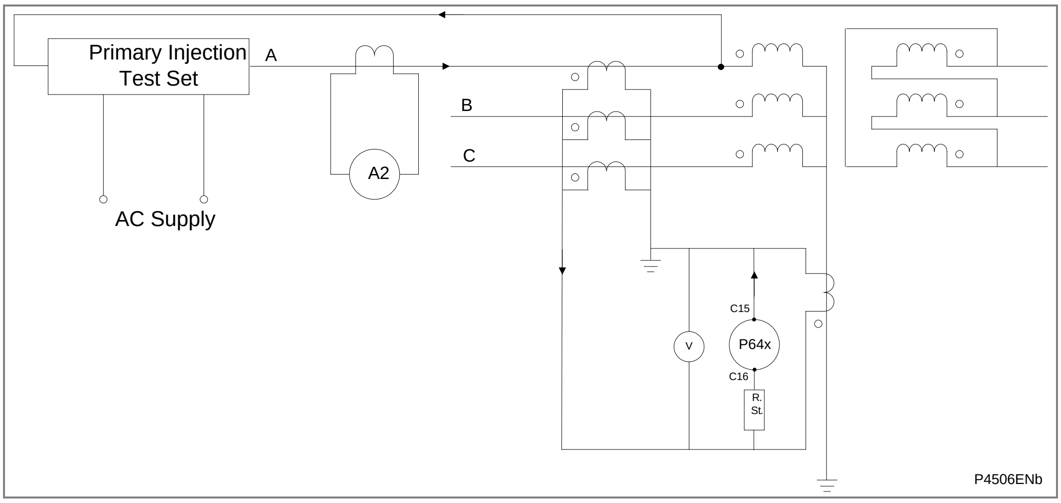

Primary Injection Test Set
A
B
C
A2
AC Supply
C15
V
P64x
C16
R. St.
P4506ENb

Figure 14 - REF/BEF - Primary injection - sensitivity test set up

6.6 Overflux Protection

The overflux protection has five independent elements, one is used to give an alarm indication and the other four are used to cause a trip.

6.6.1 Overflux Alarm Sensitivity

The one-phase VT is associated with the winding 2 overfluxing element, and the three-phase VT is associated with the winding 1 overfluxing element.

1. Configure the equipment so that an AC voltage (any phase-phase pair may be used) can be applied to terminals F4 and F3, starting a timer when the voltage is applied, and stopping the timer when the output relay energizes.
2. Configure an output relay in the PSL as W1 V/Hz> Alarm [DDB 501]. For a duration greater than the time set in the cell [V/Hz Alarm Delay], found in the **GROUP 1 OVERFLUXING** menu heading, **Volts/Hz W1** sub-heading, apply a voltage of:

   $$V = \text{V/Hz Alm Set} \times \text{f} \times 0.95$$

   to terminals F4 and F3, where V/Hz Alm Set is found in the **GROUP 1 OVERFLUXING** menu heading, **Volts/Hz W1** sub-heading, and f is the system frequency.
3. Ensure that the selected output relay does not energize.
4. Apply a voltage of:

   $$V = \text{V/Hz Alm Set} \times \text{f} \times 1.05$$

   to terminals F4 and F3 and ensure that the selected output relay does energize and that the time is within ±20% of the time set in the cell [V/Hz Alarm Delay], found in the **GROUP 1 OVERFLUXING** menu heading, **Volts/Hz W1** sub-heading.
5. Repeat the same test for the W2 V/Hz> Alarm [DDB 503] if applicable.

6.6.2 Overflux Trip Sensitivity

The first stage overfluxing element can be either definite time (DT) or inverse minimum definite time (IDMT). This will be found under the **GROUP 1 OVERFLUXING** menu heading, **Volts/Hz W1** sub-heading. If the cell [V/Hz>1 Function] is set to DT, operation of the output relay should occur in t ±20%, where t is the value in the cell [V/Hz>1 Delay] which is also found in the **GROUP 1 OVERFLUXING** menu heading, **Volts/Hz W1** sub-heading.

If the cell [V/Hz>1 Function] is set to IDMT, operation should occur in:

$$t = \frac{\text{V/Hz} > 1\,\text{Trip TMS}}{\left(\dfrac{\text{V/Hz}}{\text{V/Hz} > 1\,\text{Trip Set}} - 1\right)^2}$$

This characteristic is plotted on the graph shown in Figure 15.

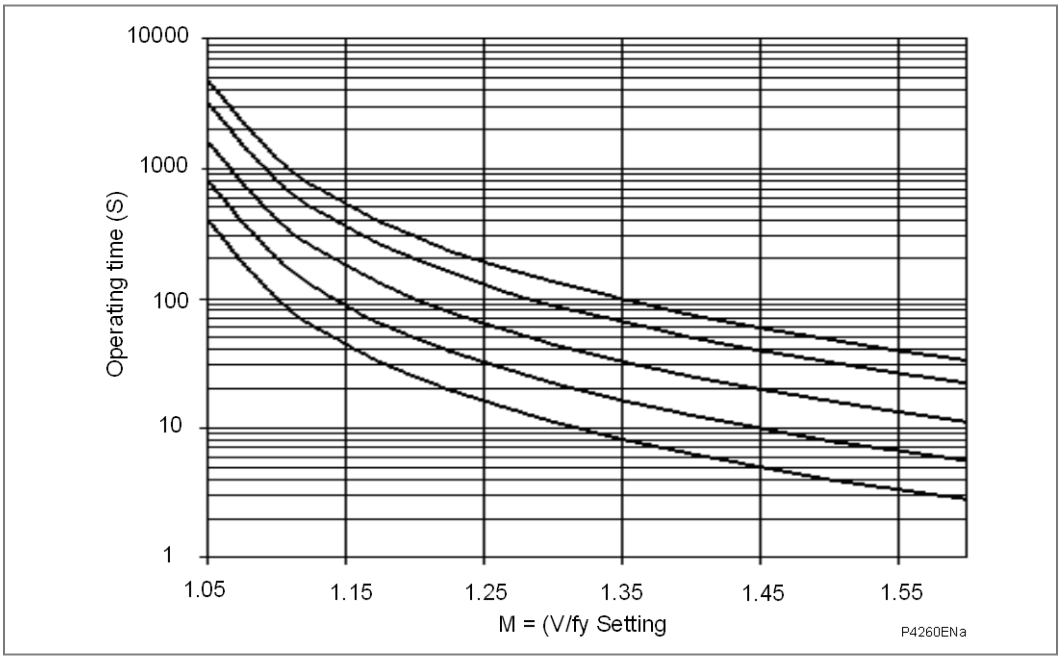


Figure 15 - IDMT overfluxing protection characteristic

For a duration greater than the time t calculated from the equation above, apply a voltage of:

$$V = \text{V/Hz} > 1\,\text{Trip Set} \times \text{f} \times 0.95$$

where V/Hz>1 Trip Set is found in the **GROUP 1 OVERFLUXING** menu heading, **Volts/Hz W1** sub-heading and f is the system frequency. Ensure that the selected output relay does not energize.

Next, apply a voltage of:

$$V = \text{V/Hz Trip Set} \times \text{f} \times 1.05$$

then confirm that the selected output relay does energize and the time is within ±20% of the time t above.

6.7 Backup Phase Overcurrent Protection

The overcurrent protection function I > 1 element should be tested.

To avoid spurious operation of any other protection elements, all protection elements except the overcurrent protection should be disabled for the duration of the overcurrent element tests. This is done in the relay’s **CONFIGURATION** column. Make a note of which elements need to be re-enabled after testing.

6.7.1.1 Connect the Test Circuit

Determine which output relay has been selected to operate when a I > 1 trip occurs by viewing the relay’s programmable scheme logic.

The programmable scheme logic can only be changed using the appropriate software. If this software is not available, the default output relay allocations are still applicable.

If the trip outputs are phase-segregated (a different output relay allocated for each phase), the relay assigned for tripping on “A” phase faults should be used.

If stage 1 is not mapped directly to an output relay in the programmable scheme logic, output relay 3 (H5 - H6 in the 60TE case and L5 - L6 in the 80TE case) should be used for the test as relay 3 initiates the trip LED.

HV Three Pole Tripping	DDB 960:	POC 1 I□> 1 Trip
HV Single Pole Tripping	DDB 961:	POC 1 I□> 1 Trip A
	DDB 962:	POC 1 I□> 1 Trip B
	DDB 963:	POC 1 I□> 1 Trip C
LV Three Pole Tripping	DDB 976:	POC 2 I□> 1 Trip
LV Single Pole Tripping	DDB 977:	POC 2 I□> 1 Trip A
	DDB 978:	POC 2 I□> 1 Trip B
	DDB 979:	POC 2 I□> 1 Trip C
TV Three Pole Tripping	DDB 992:	POC 3 I□> 1 Trip
TV Single Pole Tripping	DDB 993:	POC 3 I > 1 Trip A
	DDB 994:	POC 3 I > 1 Trip B
	DDB 995:	POC 3 I > 1 Trip C

For details of the associated terminal numbers refer to the external connection diagrams in the *Installation* chapter *P64x/EN IN*.

6. Connect the output relay so that its operation will trip the test set and stop the timer.
7. Connect the current output of the test set to the **HV-A** phase current transformer input of the relay to test the POC 1 I > 1 Trip.
8. Connect the current output of the test set to the **LV-A** phase current transformer input of the relay to test the POC 2 I > 1 Trip.
9. Connect the current output of the test set to the **TV-A** phase current transformer input of the relay to test the POC 3 I > 1 Trip.
10. Ensure that the timer starts when the current is applied to the relay.

6.7.1.2 Perform the Test

1. Ensure that the timer is reset.
2. Apply a current of twice the setting in cell [3505: GROUP 1 OVERCURRENT, I > 1 Current Set] to the relay and note the time displayed when the timer stops.
3. Check the red trip LED and yellow alarm LED come on when the relay operates.
4. Check “Alarms/Faults Present - Started Phase A, Tripped Phase A, POC 1 Start I > 1, POC 1 Trip I > 1” is on the display.
5. Reset all alarms. Note, the trip LED is initiated from operation of relay 3.

6.7.1.3 Check the Operating Time

Check that the operating time recorded by the timer is within the range shown in Table 22.

Note	*Except for the definite time characteristic, the operating times shown in Table 22 are for a time multiplier or time dial setting of 1. Therefore, to obtain the operating time at other time multiplier or time dial settings, the time shown in Table 22 must be multiplied by the setting of cell [3507: GROUP 1 OVERCURRENT1, I□> 1 TMS], [3537: GROUP 1 OVERCURRENT2, I□> 1 TMS] or [3567: GROUP 1 OVERCURRENT3, I□> 1 TMS] for IEC or UK characteristics or cell [3508: GROUP 1 OVERCURRENT1, Time Dial], [3538: GROUP 1 OVERCURRENT2, I□> 1 Time Dial] or [3568: GROUP 1 OVERCURRENT3, I□> 1 Time Dial] for IEEE and US characteristics.*

Also, for definite time and inverse characteristics there is an additional delay of up to 0.02 seconds and 0.08 seconds respectively that may need to be added to the relay's acceptable range of operating times.

For all characteristics, allowance must be made for the accuracy of the test equipment being used.

Characteristic	**Operating time at twice current setting and time multiplier/time dial setting of 1.0**	
	Nominal (seconds)	**Range (seconds)**
DT	[3506: I>1 Time Delay] setting	Setting ±5%
IEC S Inverse	10.03	9.53 - 10.53
IEC V Inverse	13.50	12.83 - 14.18
IEC E Inverse	26.67	25.34 - 28
UK LT Inverse	120.00	114.00 - 126.00
IEEE M Inverse	3.8	3.61 - 3.99
IEEE V Inverse	7.03	6.68 - 7.38
IEEE E Inverse	9.52	9.04 - 10
US Inverse	2.16	2.05 - 2.27
US ST Inverse	12.12	11.51 - 12.73

Table 22 - Characteristic operating times for Overcurrent1 I>1, Overcurrent2 I> and Overcurrent I>

On completion of the tests, any protection elements that were disabled for testing purposes must have their original settings restored in the **CONFIGURATION** column.

6.8 Thermal Overload Protection

Consider a two winding transformer, with the thermal element monitoring the bias current. First, calculate the full load current through the HV winding and LV winding. The reference power and the nominal voltage of each winding should be considered.

$$\mathrm{FLC_{HV}} = \frac{\mathrm{S_{ref}}}{\sqrt{3} \times \mathrm{Vnon_{HV}}} \qquad \mathrm{FLC_{LV}} = \frac{\mathrm{S_{ref}}}{\sqrt{3} \times \mathrm{Vnon_{LV}}}$$

Where:

S_{ref} = reference power given in the setting cell **Ref Power S**.
V_{nonHV} = HV nominal voltage given in the setting cell **HV Nominal**.
V_{nonLV} = LV nominal voltage given in the setting cell **LV Nominal**.

A spreadsheet showing the theoretical operating time of the thermal element can be provided on request. If the monitored winding is the bias current, the Ku factor required in the spreadsheet is calculated as follows:

$$K_u = \frac{\frac{I_{HV}}{FLC_{HV}} + \frac{I_{LV}}{FLC_{LV}}}{2 \times IB}$$

Where:

I_{HV} = current flowing through the HV winding (this is the current to be injected through the CT assigned to the HV winding)
I_{LV} = current flowing through the LV winding (this is the current to be injected through the CT assigned to the LV winding)
IB = rated load in pu
K_u = ratio of ultimate load to rated load

Report the following measurements:

Top oil temperature at tripping: ____________________

Hottest spot temperature at tripping: ____________________

Thermal model operating time (spreadsheet): ____________________

Operating time recorded by the test equipment: ____________________

Error - top oil operating time: ____________________

Error - hottest spot operating time: ____________________

When the operating time of the top oil element is tested, set the hottest spot element operating time delay high enough to avoid any interference. When the operating time of the hottest spot element is tested, set the top oil element operating time delay high enough to avoid any interference.

If the monitor winding is set as either HV winding or LV winding, then K_u is calculated as follows:

$$K_u = \frac{I_{HV}}{IFLC_{HV} \times IB} \qquad K_u = \frac{I_{LV}}{IFLC_{LV} \times IB}$$

6.9 Current Transformer Supervision

Under configuration only enable the differential and supervision elements. Consider the CTS settings shown in Table 23:

Parameter	Setting
Diff CTS	Enabled
CTS Status	Restrain
CTS Time Delay	2.000 s
CTS I1	10.00%
CTS I2/I1>1	20.00%
CTS I2/I1>2	40.00%

Table 23 - CTS settings

Consider a two winding transformer and that a P642 is being used. Inject full load current in inputs 1 and 2 simulating a load condition.

$$FLC_{HV} \times In = \frac{\dfrac{HVrating}{\sqrt{3} \times HVnominal}}{CT1_{prim}} \qquad FLC_{LV} \times In = \frac{\dfrac{LVrating}{\sqrt{3} \times LVnominal}}{CT2_{prim}}$$

Where:
HV rating = HV power
LV rating = LV power
HV nominal = HV nominal voltage
LV nominal = LV nominal voltage
CT1prim = CT1 nominal primary current
CT2prim = CT2 nominal primary current
In = CT nominal secondary current
Inject balance current in current input 1.
Ia = FLCHV × In ∠0°
Ib = FLCHV × In ∠-120°
Ic = FLCHV × In ∠120°
Inject balance current in current input 2:
Ia = FLCLV × In ∠210°
Ib = FLCLV × In ∠90°
Ic = FLCLV × In ∠330°

Notice that the differential element does not trip because a load condition is being simulated. To simulate a problem in the A phase wiring, suddenly decrease to zero the A phase current of current input 1:

Ia = 0 ∠0°
Ib = FLCHV × In ∠-120°
Ic = FLCHV × In ∠120°

Note that the CT fail alarm is asserted, and the differential function is blocked.

Measure current input 1 positive and negative sequence currents from the Measurement 1 column. The I2/I1 ratio should be ≥ 40%.

I1-1 Magnitude: ___________________

I2-1 Magnitude: ___________________

I2/I1 CT1 ratio: ___________________

Sufficient positive sequence current is flowing through the current inputs 1 and 2 (the threshold is 0.1 In). No inrush condition is present and the Inhibit CTS signal is low. As a result, the Is1 setting is increased to Is-CTS.

Measure the differential current and bias current from the Measurement 3 column:

Ia bias = ___________________ Ia diff = ___________________

Ib bias = ___________________ Ib diff = ___________________

Ic bias =___________________ Ic diff = ___________________

Localize these points within the differential characteristic. Note that the differential function did not trip because the Is1 setting has been increased to Is-CTS.

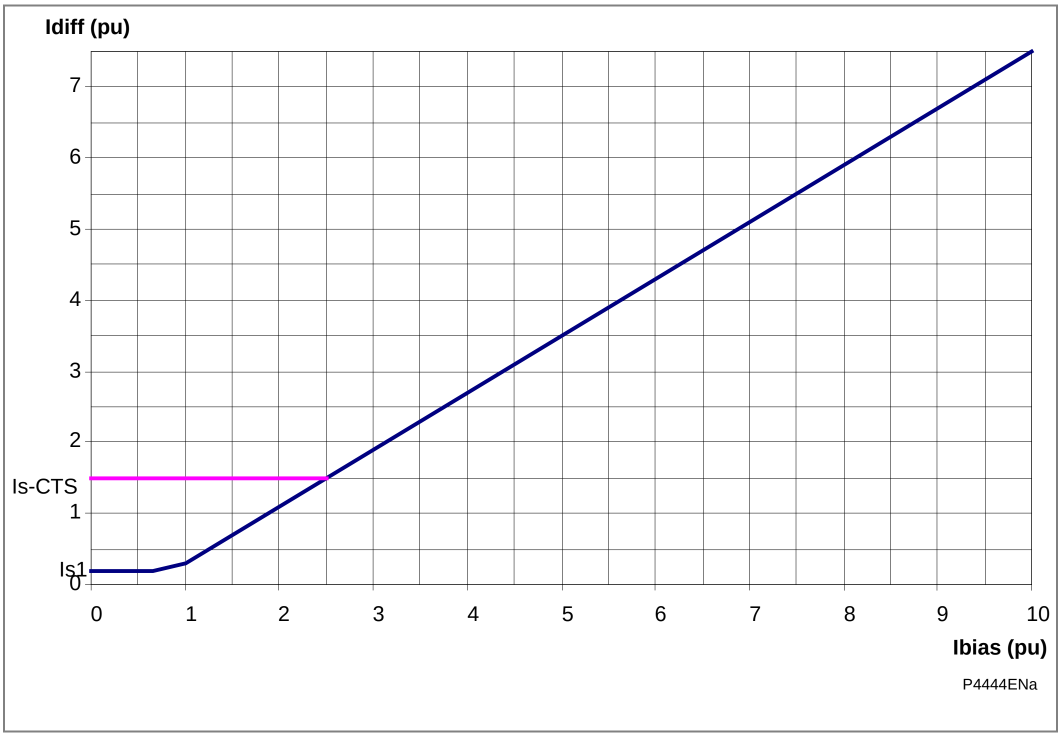


Figure 16 - CTS - Differential characteristic

Suddenly increase the A phase current from zero to 4 × FLCHV × In:

Ia = 4 × FLCHV × In ∠0°

Ib = FLCHV × In ∠-120°

Ic = FLCHV × In ∠120°

The differential element will trip. Record the differential and bias measurements and localize these points in the differential characteristic.

Ia bias = ____________________ Ia diff = ____________________

Ib bias = ____________________ Ib diff = ____________________

Ic bias = ____________________ Ic diff = ____________________

6.10 Through Fault Monitoring

Consider the through fault monitoring default settings shown in Table 24.

Parameter	Setting
Through Fault	Enabled
Monitored Input	HV
TF I> Trigger	3.850 pu
TF I2t> Alarm	100 pu

Table 24 - Through fault monitoring settings

The I^2t is described as follows:

$$I^2t = \left(\frac{1}{x} \times FLC\right)^2 \times 2$$

Where:

X = transformer reactance, which would limit the through fault current flowing through the transformer

FLC = full load current of the winding being monitored. To calculate this current use the winding power rating and nominal voltage.

2 = maximum duration limit in seconds for the worst case of mechanical duty

If the reactance is 10% and the I2t> Alarm is 100 pu, then at 10 times FLC, the through fault alarm should be asserted. The test equipment should register the time elapsed from the beginning of the injection to the assertion of the alarm as 2 s. When a current less than the maximum through fault current flows, the time required by the alarm to be asserted is as follows:

$$t = \frac{\left(\frac{1}{X}\right)^2 \times 2}{I^2}$$

Where:

I = current flowing through the monitored winding in pu

Inject 4 A in current input 1:

Ia = 4 In ∠0°

Ib = 4 In ∠-120°

Ic = 4 In ∠120°

After 2 s approximately from the beginning of the injection, a through fault alarm is generated. A through fault event is generated as soon as the current through the monitor winding is above TF I> Trigger. To monitor the time, wire the relay output 4 to an input in the test equipment.

Time registered by the test equipment: ____________________

IA peak: ____________________

IB peak: ____________________

IC peak: ____________________

I2t A phase: ____________________

I2t B phase: ____________________

I2t C phase: ____________________

7 ON-LOAD CHECKS

The following on-load measuring checks ensure the external wiring to the current and voltage inputs is correct but can only be carried out if there are no restrictions which prevent energizing the plant being protected.

Caution	**Remove all test leads and temporary shorting leads, and replace any external wiring that has been removed to allow testing.**

If any of the external wiring had to be disconnected from the relay to perform any of the foregoing tests, make sure that all connections are restored according to the relevant external connection or scheme diagram.

7.1 Voltage Connections

Caution	**Using a multimeter, measure the voltage transformer secondary voltages to ensure they are correctly rated. Check that the system phase rotation is correct using a phase rotation meter.**

Compare the values of the secondary phase voltages with the relay’s measured values, which can be found in the **MEASUREMENTS 1** menu column.

If cell [0D02: MEASURE’T SETUP, Local Values] is set to **Secondary**, the values displayed on the relay LCD or a portable PC connected to the front EIA(RS)232 communication port should be equal to the applied secondary voltage. The values should be within 1% of the applied secondary voltages. However, an additional allowance must be made for the accuracy of the test equipment being used.

If cell [0D02: MEASURE’T SETUP, Local Values] is set to **Primary**, the values displayed should be equal to the applied secondary voltage multiplied the corresponding voltage transformer ratio set in the **CT & VT RATIOS** menu column (see Table 25). Again, the values should be within 1% of the expected value, plus an additional allowance for the accuracy of the test equipment being used.

Voltage	Cell in MEASUREMENTS 1 Column (02)	Corresponding VT ratio (in “VT and CT RATIO” Column (0A) of Menu)
V_{AB}	[029C: VAB Magnitude]	[0A03: Main VT Primary] [0A04: Main VT Sec’y]
V_{BC}	[029E: VBC Magnitude]	
V_{CA}	[02A0: VCA Magnitude]	
V_{AN}	[028F: VAN Magnitude]	
V_{BN}	[0291: VBN Magnitude]	
V_{CN}	[0293: VCN Magnitude]	
V_X	[0295: Vx Measured Mag]	[0A07: V_X VT Primary] [0A08: V_X VT Sec’y]

Table 25 - Measured voltages and VT ratio settings

7.2 Current Connections

Caution	**Measure the current transformer secondary values for each input using a multimeter connected in series with corresponding relay current input.**

Check that the current transformer polarities are correct by measuring the phase angle between the current and voltage, either against a phase meter already installed on site and known to be correct or by determining the direction of power flow by contacting the system control center.

Ensure the current flowing in the neutral circuit of the current transformers is negligible.

Compare the values of the secondary phase currents and phase angle with the relay’s measured values, which can be found in the **MEASUREMENTS 1** menu column.

Note	*Under normal load conditions the earth fault function measures little or no current. It is therefore necessary to simulate a phase-to-neutral fault. This can be achieved by temporarily disconnecting one or two of the line current transformer connections to the relay and shorting the terminals of these current transformer secondary windings.*

Check that the IA/IB/IC Differential currents measured on the relay are less than 10% of the IA/IB/IC Bias currents, see the **MEASUREMENTS 3** menu. Check that the I2 Magnitude negative phase sequence current measured by the relay is not greater than expected for the particular installation, see the **MEASUREMENTS 1** menu. Check that the active and reactive power measured by the relay are correct, see the Measurements 2 menu. The power measurement modes are described in the *Measurements and Recording* chapter*, P64x/EN MR*.

If cell [0D02: MEASURE’T SETUP, Local Values] is set to **Secondary**, the current displayed on the relay LCD or a portable PC connected to the front EIA(RS)232 communication port should be equal to the applied secondary current. The values should be within 1% of the applied secondary currents. However, an additional allowance must be made for the accuracy of the test equipment being used.

If cell [0D02: MEASURE’T SETUP, Local Values] is set to **Primary**, the current displayed should be equal to the applied secondary current multiplied by the corresponding current transformer ratio set in the **CT & VT RATIOS** menu column (see Table 12). Again the values should be within 10% of the expected value, plus an additional allowance for the accuracy of the test equipment being used.

Note	*If the relay is applied with a single dedicated current transformer for the earth fault function, it may not be possible to check the relay’s measured values as the neutral current will be almost zero.*

8 FINAL CHECKS

The tests are now complete.

Caution	**Remove all test or temporary shorting leads. If it has been necessary to disconnect any of the external wiring from the relay to perform the wiring verification tests, make sure all connections are replaced according to the relevant external connection or scheme diagram.**

Ensure that the relay is restored to service by checking that cell [0F0F: COMMISSIONING TESTS, Test Mode] is set to **Disabled**.

If the relay is in a new installation, the thermal memory, transformer loss of life and overfluxing elements may be reset if required. These elements may be reset under the **MEASUREMENTS 3** menu heading. If the required access level is not active, the relay prompts for a password so that the setting change can be made.

If the menu language was changed to allow accurate testing, it should now be restored to the customer’s preferred language.

If an MMLG test block is installed, remove the MMLB01 test plug and replace the MMLG cover so that the protection is put into service.

Ensure that all event records, fault records, disturbance records, alarms and LEDs have been reset before leaving the relay.

If applicable, replace the secondary front cover on the relay.

9 COMMISSIONING TEST RECORD

9.1 Date Record

Date: ________________ Engineer: ________________

Station: Circuit: ________________

System Frequency: Hz

VT Ratio: /V CT Ratio (tap in use): /A

9.2 Front Plate Information

Transformer protection relay	**MiCOM P64**
Model number	
Serial number	
Rated current In	1 A ☐ 5 A ☐
Rated voltage Vn	
Auxiliary voltage Vx	

9.3 Test Equipment Used

This section should be completed to allow future identification of protective devices that have been commissioned using equipment that is later found to be defective or incompatible but may not be detected during the commissioning procedure.

Overcurrent test set	Model: Serial No:	
Phase angle meter	Model: Serial No:	
Phase rotation meter	Model: Serial No:	
Insulation tester	Model: Serial No:	
Setting software:	Type: Version:	

9.4 Product Checks

	Have all relevant safety instructions been followed?	Yes ☐ No ☐
5.	PRODUCT CHECKS	
5.1	With the relay de-energized	
5.1.1	Visual inspection	
	Relay damaged?	Yes ☐ No ☐
	Rating information correct for installation?	Yes ☐ No ☐
	Case earth installed?	Yes ☐ No ☐
5.1.2	Current transformer shorting contacts close?	Yes ☐ No ☐ Not checked ☐
5.1.3	Insulation resistance > 100 MΩ at 500 V dc	Yes ☐ No ☐ Not tested ☐
5.1.4	External wiring	
	Wiring checked against diagram?	Yes ☐ No ☐
	Test block connections checked?	Yes ☐ No ☐ N/A ☐
5.1.5	Watchdog contacts (auxiliary supply off)	
	Terminals 11 and 12 Contact closed?	Yes ☐ No ☐
	Contact resistance	______ Ω ☐ Not measured
	Terminals 13 and 14 Contact open?	Yes ☐ No ☐
5.1.6	Measured auxiliary supply	V ac/dc
5.2	With the relay energized	
5.2.1	Watchdog contacts (auxiliary supply on)	
	Terminals 11 and 12 Contact open?	Yes ☐ No ☐
	Terminals 13 and 14 Contact closed?	Yes ☐ No ☐
	Contact resistance	______ Ω ☐ Not measured
5.2.2	LCD front panel display	
	LCD contrast setting used	
5.2.3	Date and time	
	Clock set to local time?	Yes ☐ No ☐
	Time maintained when auxiliary supply removed?	Yes ☐ No ☐
5.2.4	Light emitting diodes	
	Relay healthy (green) LED working?	Yes ☐ No ☐
	Alarm (yellow) LED working?	Yes ☐ No ☐
	Out of service (yellow) LED working?	Yes ☐ No ☐
	Trip (red) LED working?	Yes ☐ No ☐
	All 8 (P642), 18 (P643/5) programmable LEDs working?	Yes ☐ No ☐

5.2.5 Field supply voltage

Value measured between terminals 7 and 9	V dc
Value measured between terminals 8 and 10	V dc

5.2.6 Input opto-isolators

Opto input 1	working?	Yes ☐	No ☐	
Opto input 2	working?	Yes ☐	No ☐	
Opto input 3	working?	Yes ☐	No ☐	
Opto input 4	working?	Yes ☐	No ☐	
Opto input 5	working?	Yes ☐	No ☐	
Opto input 6	working?	Yes ☐	No ☐	
Opto input 7	working?	Yes ☐	No ☐	
Opto input 8	working?	Yes ☐	No ☐	
Opto input 9	working?	Yes ☐	No ☐	N/A ☐
Opto input 10	working?	Yes ☐	No ☐	N/A ☐
Opto input 11	working?	Yes ☐	No ☐	N/A ☐
Opto input 12	working?	Yes ☐	No ☐	N/A ☐
Opto input 13	working?	Yes ☐	No ☐	N/A ☐
Opto input 14	working?	Yes ☐	No ☐	N/A ☐
Opto input 15	working?	Yes ☐	No ☐	N/A ☐
Opto input 16	working?	Yes ☐	No ☐	N/A ☐
Opto input 17	working?	Yes ☐	No ☐	N/A ☐
Opto input 18	working?	Yes ☐	No ☐	N/A ☐
Opto input 19	working?	Yes ☐	No ☐	N/A ☐
Opto input 20	working?	Yes ☐	No ☐	N/A ☐
Opto input 21	working?	Yes ☐	No ☐	N/A ☐
Opto input 22	working?	Yes ☐	No ☐	N/A ☐
Opto input 23	working?	Yes ☐	No ☐	N/A ☐
Opto input 24	working?	Yes ☐	No ☐	N/A ☐
Opto input 25	working?	Yes ☐	No ☐	N/A ☐
Opto input 26	working?	Yes ☐	No ☐	N/A ☐
Opto input 27	working?	Yes ☐	No ☐	N/A ☐
Opto input 28	working?	Yes ☐	No ☐	N/A ☐
Opto input 29	working?	Yes ☐	No ☐	N/A ☐
Opto input 30	working?	Yes ☐	No ☐	N/A ☐
Opto input 31	working?	Yes ☐	No ☐	N/A ☐
Opto input 32	working?	Yes ☐	No ☐	N/A ☐

5.2.7 Output relays

Relay 1	working?	Yes ☐ No ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 2	working?	Yes ☐ No ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 3	working?	Yes ☐ No ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 4	working?	Yes ☐ No ☐
	Contact resistance (N/C)	______ Ω ☐ Not measured
	(N/O)	______ Ω ☐ Not measured
Relay 5	working?	Yes ☐ No ☐
	Contact resistance (N/C)	______ Ω ☐ Not measured
	(N/O)	______ Ω ☐ Notmeasured
Relay 6	working?	Yes ☐ No ☐
	Contact resistance (N/C)	______ Ω ☐ Not measured
	(N/O)	______ Ω ☐ Not measured
Relay 7	working?	Yes ☐ No ☐
	Contact resistance (N/C)	______ Ω ☐ Not measured
	(N/O)	______ Ω ☐ Not measured
Relay 8	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance (N/C)	______ Ω ☐ Not measured
	(N/O)	______ Ω ☐ Not measured
Relay 9	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 10	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 11	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance (N/C)	______ Ω ☐ Not measured
	(N/O)	______ Ω ☐ Not measured
Relay 12	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance (N/C)	______ Ω ☐ Not measured
	(N/O)	______ Ω ☐ Not measured
Relay 13	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance (N/C)	______ Ω ☐ ot measured
	(N/O)	______ Ω ☐ Not measured
Relay 14	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance (N/C)	______ Ω ☐ Not measured
	(N/O)	______ Ω ☐ Not measured
Relay 15	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance (N/C)	______ Ω ☐ Not measured
	(N/O)	______ Ω ☐ Not measured
Relay 16	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance (N/C)	______ Ω ☐ Not measured
	(N/O)	______ Ω ☐ Not measured
Relay 17	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 18	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 19	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 20	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 21	working?	Yes ☐ No ☐ N/A ☐

	Contact resistance	______ Ω ☐ Not measured
Relay 22	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 23	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance (N/C)	______ Ω ☐ Not measured
	(N/O)	______ Ω ☐ Not measured
Relay 24	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance (N/C)	______ Ω ☐ Not measured
	(N/O)	______ Ω ☐ Not measured
Relay 25	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 26	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 27	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 28	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 29	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 30	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance	______ Ω ☐ Not measured
Relay 31	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance (N/C)	______ Ω ☐ Not measured
	(N/O)	______ Ω ☐ Not measured
Relay 32	working?	Yes ☐ No ☐ N/A ☐
	Contact resistance (N/C)	______ Ω ☐ Not measured
	(N/O)	______ Ω ☐ Not measured

5.2.8 RTD inputs

Resistor tolerance

RTD 1 reading	[0460: RTD 1 Label]	°C
RTD 2 reading	[0461: RTD 2 Label]	°C
RTD 3 reading	[0462: RTD 3 Label]	°C
RTD 4 reading	[0463: RTD 4 Label]	°C
RTD 5 reading	[0464: RTD 5 Label]	°C
RTD 6 reading	[0465: RTD 6 Label]	°C
RTD 7 reading	[0466: RTD 7 Label]	°C
RTD 8 reading	[0467: RTD 8 Label]	°C
RTD 9 reading	[0468: RTD 9 Label]	°C
RTD 10 reading	[0469: RTD 10 Label]	°C

5.2.9	Current loop inputs	0 - 1 mA ☐ 0 - 10 mA ☐
	CLI input type	0 - 20 mA ☐ 4 - 20 mA ☐
	CLI1 reading at 50% CLI maximum range	
	[0470: CLI1 Input Label]	
	CLI2 reading at 50% CLI maximum range	
	[0471: CLI2 Input Label]	
	CLI3 reading at 50% CLI maximum range	
	[0472: CLI3 Input Label]	
	CLI4 reading at 50% CLI maximum range	
	[0473: CLI4 Input Label]	

		0 - 1 mA ☐ 0 - 10 mA ☐
5.2.10	Current loop outputs	0 - 20 mA ☐ 4 - 20 mA ☐
	CLO output type	mA
	CLO1 output current at 50% of rated output	mA
	CLO2 output current at 50% of rated output	mA
	CLO3 output current at 50% of rated output	mA
	CLO4 output current at 50% of rated output	mA

5.2.11	First rear communications port	
		K-Bus ☐ MODBUS ☐
	Communication standard	IEC60870-5-103 ☐
	Communications established?	Yes ☐ No ☐
	Protocol converter tested?	Yes ☐ No ☐ N/A ☐

		K-Bus ☐
5.2.12	Second rear communications port	EIA(RS)485 ☐
		EIA(RS)232 ☐
	Communication port configuration	Yes ☐ No ☐
	Communications established?	Yes ☐ No ☐ N/A ☐
	Protocol converter tested?	

5.2.13 Current inputs

Displayed current	Primary ☐	Secondary ☐
Phase T1 CT ratio $\left(\frac{\text{[Phase CT Primary]}}{\text{[Phase CT Sec'y]}}\right)$	_____	N/A ☐
Phase T2 CT ratio $\left(\frac{\text{[Phase CT Primary]}}{\text{[Phase CT Sec'y]}}\right)$	_____	N/A ☐
Phase T3 CT ratio $\left(\frac{\text{[Phase CT Primary]}}{\text{[Phase CT Sec'y]}}\right)$	_____	N/A ☐
Phase T4 CT ratio $\left(\frac{\text{[Phase CT Primary]}}{\text{[Phase CT Sec'y]}}\right)$	_____	N/A ☐
Phase T5 CT ratio $\left(\frac{\text{[Phase CT Primary]}}{\text{[Phase CT Sec'y]}}\right)$	_____	N/A ☐
TN1 CT ratio $\left[\frac{IY\ HV\ CT\ \Pr imary}{IY\ HV\ CT\ Sec'y}\right]$	_____	N/A ☐
TN2 CT ratio $\left[\frac{IY\ LV\ CT\ \Pr imary}{IY\ LV\ CT\ Sec'y}\right]$	_____	N/A ☐
IY (TV) CT ratio $\left[\frac{IY\ TV\ CT\ \Pr imary}{IY\ TV\ CT\ Sec'y}\right]$	_____	N/A ☐

Input CT	Applied value	Displayed value	
IA (1)	A	A	
IB (1)	A	A	
IC (1)	A	A	
IA (2)	A	A	
IB (2)	A	A	
IC (2)	A	A	
IA (3) (P643/5)	A	_____ A	N/A ☐
IB (3) (P643/5)	A	_____ A	N/A ☐
IC (3) (P643/5)	A	_____ A	N/A ☐
IA (4) (P645)	A	_____ A	N/A ☐
IB (4) (P645)	A	_____ A	N/A ☐
IC (4) (P645)	A	_____ A	N/A ☐
IA (5) (P645)	A	_____ A	N/A ☐
IB (5) (P645)	A	_____ A	N/A ☐
IC (5) (P645)	A	_____ A	N/A ☐

IN HV (TN1 CT)	A	A	
IN LV (TN2 CT)	A	A	
IN TV (TN3 CT)	A	_____ A	N/A ☐

5.2.14 Voltage inputs

Displayed voltage — Primary ☐ Secondary ☐

Main VT ratio

$$\left(\frac{\text{[Main VT Primary]}}{\text{[Main VT Sec'y.]}}\right)$$

_____ N/A ☐

V_X VT ratio

$$\left[\frac{V_x VT\ \Pr imary}{V_X VT\ Secondary}\right]$$

_____ N/A ☐

Input VT	Applied Value	Displayed value
Va (optional P643/5)	V	V
Vb (optional P643/5)	V	V
Vc (optional P643/5)	V	V
V_X (P642/3/5)	V	V

6.	SETTING CHECKS	
6.1	Application-specific function settings applied?	Yes ☐ No ☐
	Application-specific programmable scheme logic settings applied?	Yes ☐ No ☐ N/A ☐
6.2	Application-specific function settings verified?	Yes ☐ No ☐ N/A ☐
	Application-specific programmable scheme logic tested?	Yes ☐ No ☐ N/A ☐
6.3	Demonstrate correct relay operation	
6.3.1	Transformer differential protection (P642/P643/P644/P645)	
6.3.1.2	Transformer Differential lower slope pickup	A
6.3.1.3	Transformer Differential upper slope pickup	A
6.3.2.1	Transformer Differential Phase A contact routing OK?	Yes ☐ No ☐
	Transformer Differential Phase A trip time	s
6.3.2.2	Transformer Differential Phase B contact routing OK?	Yes ☐ No ☐
	Transformer Differential Phase B trip time	s
6.3.2.3	Transformer Differential Phase C contact routing OK?	Yes ☐ No ☐
	Transformer Differential Phase C trip time	s
	Average trip time, Phases A, B and C	s
6.3.3	Overcurrent protection (P642/P643/P645)	
	Protection function timing tested?	Yes ☐ No ☐
	Overcurrent type (set in cell [I>1 Direction])	Directional ☐ Non-directional ☐
	Applied current	A
	Expected operating time	s
	Measured operating time	s

7. ON-LOAD CHECKS

Test wiring removed?	Yes ☐	No ☐	N/A ☐
Disturbed customer wiring re-checked?	Yes ☐	No ☐	N/A ☐
On-load test performed?	Yes ☐	No ☐	

7.1

VT wiring checked?	Yes ☐	No ☐	N/A ☐
Phase rotation correct?	Yes ☐	No ☐	
Displayed voltage	Primary ☐	Secondary ☐	
Main VT ratio $\left(\frac{\text{[Main VT Primary]}}{\text{[Main VT Sec'y.]}}\right)$	_____ V	N/A ☐	
V_X VT ratio $\left[\frac{V_xVT\ \mathrm{Pr}\,imary}{V_XVT\ Secondary}\right]$	_____ V	N/A ☐	

Voltages	Applied Value	Displayed value
V_{AN}/V_{AB}	V	V
V_{BN}/V_{BC}	V	V
V_{CN}/V_{CA}	V	V
V_X	V	V

7.2	CT wiring checked?	Yes ☐	No ☐	N/A ☐
	CT polarities correct?	Yes ☐	No ☐	
	Displayed current	Primary ☐	Secondary ☐	
	Phase CT (1) ratio $\left(\frac{\text{[Phase CT Primary]}}{\text{[Phase CT Sec'y]}}\right)$	_____	N/A ☐	
	Phase CT (2) ratio $\left(\frac{\text{[Phase CT Primary]}}{\text{[Phase CT Sec'y]}}\right)$	_____	N/A ☐	
	Phase CT (3) ratio $\left(\frac{\text{[Phase CT Primary]}}{\text{[Phase CT Sec'y]}}\right)$	_____	N/A ☐	
	Phase CT (4) ratio $\left(\frac{\text{[Phase CT Primary]}}{\text{[Phase CT Sec'y]}}\right)$	_____	N/A ☐	
	Phase CT (5) ratio $\left(\frac{\text{[Phase CT Primary]}}{\text{[Phase CT Sec'y]}}\right)$	_____	N/A ☐	
	TN1 CT ratio $\left[\frac{IY\ HV\ CT\ \Pr imary}{IY\ HV\ CT\ Sec'y}\right]$	_____	N/A ☐	
	TN2 CT ratio $\left[\frac{IY\ LV\ CT\ \Pr imary}{IY\ LV\ CT\ Sec'y}\right]$	_____	N/A ☐	
	TN3 CT ratio $\left[\frac{IY\ TV\ CT\ \Pr imary}{IY\ TV\ CT\ Sec'y}\right]$	_____	N/A ☐	

Input CT	Applied Value	Displayed Value		
IA (1)	A	A		
IB (1)	A	A		
IC (1)	A	A		
IA (2)	A	A		
IB (2)	A	A		
IC (2)	A	A		
IA (3) (P643/5)	A	_____ A	N/A	☐
IB (3) (P643/5)	A	_____ A	N/A	☐
IC (3) (P643/5)	A	_____ A	N/A	☐
IA (4) (P645)	A	_____ A	N/A	☐
IB (4) (P645)	A	_____ A	N/A	☐
IC (4) (P645)	A	_____ A	N/A	☐
IA (5) (P645)	A	_____ A	N/A	☐
IB (5) (P645)	A	_____ A	N/A	☐
IC (5) (P645)	A	_____ A	N/A	☐
TN1 CT	A	_____ A	N/A	☐
TN2 CT	A	_____ A	N/A	☐
TN3 CT	A	_____ A	N/A	☐

8. FINAL CHECKS

Test wiring removed?	Yes ☐ No ☐ N/A ☐
Disturbed customer wiring re-checked?	Yes ☐ No ☐ N/A ☐
Test mode disabled?	Yes ☐ No ☐
Current counters reset?	Yes ☐ No ☐ N/A ☐
Event records reset?	Yes ☐ No ☐
Fault records reset?	Yes ☐ No ☐
Disturbance records reset?	Yes ☐ No ☐
Alarms reset?	Yes ☐ No ☐
LEDs reset?	Yes ☐ No ☐
Secondary front cover replaced?	Yes ☐ No ☐ N/A ☐

Commissioning Engineer

Customer Witness

Date:

Date:

10 SETTING RECORD

10.1 Date Record

Date:		**Engineer:**	
Station:		**Circuit:**	
		System Frequency:	Hz

10.2 Front Plate Information

Transformer protection relay	**MiCOM P64**
Model number	
Serial number	
Rated current In	1 A ☐ 5 A ☐
Rated voltage Vn	
Auxiliary voltage Vx	

10.3 Setting Groups Used

Group 1	Yes ☐ No ☐
Group 2	Yes ☐ No ☐
Group 3	Yes ☐ No ☐
Group 4	Yes ☐ No ☐

10.4 0000 - System Data

0000	**SYSTEM DATA**	
0001	Language	English ☐ Francais ☐ Deutsch ☐ Español ☐
0002	Password	
0003	Sys Fn Links	
0004	Description	
0005	Plant Reference	
0006	Model Number	
0008	Serial Number	
0009	Frequency	
000A	Comms Level	
000B	Relay Address	
000C	Plant Status	
000D	Control Status	
000E	Active group	
0011	Software Ref 1	
0030	Opto I/P Status	
0040	Rly O/P Status	

0000	SYSTEM DATA	
0050	Alarm Status 1	
0051	Alarm Status 2	
0052	Alarm Status 3	
0053	Usr Alarm Status	
00D0	Access Level	
00D1	Password Control	Level 0 ☐ Level 1 ☐ Level 2 ☐
00D2	Password Level 1	
00D3	Password Level 2	

10.5 0800 - Date and Time

0800	DATE AND TIME		
0801	Date/Time		
08NA	Date		
08NA	Time		
0804	IRIG-B Sync	Disabled ☐	Enabled ☐
0805	IRIG-B Status	Inactive ☐	Active ☐
0806	Battery Status	Dead ☐	Healthy ☐
0807	Battery Alarm		
0813	SNTP Status		
0820	LocalTime Enable		
0821	LocalTime Offset		
0822	DST Enable		
0823	DST Offset		
0824	DST Start		
0825	DST Start Day		
0826	DST Start Month		
0827	DST Start Mins		
0828	DST End		
0829	DST End Day		
082A	DST End Month		
082B	DST End Mins		
0830	RP1 Time Zone		
0831	RP2 Time Zone		
0832	DNPOE Time Zone		
0833	Tunnel Time Zone		

10.6 0900 - Configuration

0900	CONFIGURATION	
0901	Restore Defaults	
0902	Setting Group	Select using Menu ☐ Select using Optos ☐
0903	Active Settings	Group 1 ☐ Group 2 ☐ Group 3 ☐ Group 4 ☐

0900	CONFIGURATION	
0904	Save Changes	
0905	Copy From	
0906	Copy To	
0907	Setting Group 1	Disabled ☐ Enabled ☐
0908	Setting Group 2	Disabled ☐ Enabled ☐
0909	Setting Group 3	Disabled ☐ Enabled ☐
090A	Setting Group 4	Disabled ☐ Enabled ☐
090C	Diff Protection	Disabled ☐ Enabled ☐
090E	REF Protection	Disabled ☐ Enabled ☐
0910	Overcurrent	Disabled ☐ Enabled ☐
0911	NPS Overcurrent	Disabled ☐ Enabled ☐
0912	Thermal Overload	Disabled ☐ Enabled ☐
0913	Earth Fault	Disabled ☐ Enabled ☐
0916	Residual O/V NVD	Disabled ☐ Enabled ☐
0918	Overfluxing V/Hz	Disabled ☐ Enabled ☐
091B	Through Fault	Disabled ☐ Enabled ☐
091D	Volt Protection	Disabled ☐ Enabled ☐
091E	Freq Protection	Disabled ☐ Enabled ☐
091F	RTD Inputs	Disabled ☐ Enabled ☐
0920	CB Fail	Disabled ☐ Enabled ☐
0921	Supervision	Disabled ☐ Enabled ☐
0925	Input Labels	Invisible ☐ Visible ☐
0926	Output Labels	Invisible ☐ Visible ☐
0927	RTD Labels	Invisible ☐ Visible ☐
0928	CT & VT Ratios	Invisible ☐ Visible ☐
0929	Record Control	Invisible ☐ Visible ☐
092A	Disturb Recorder	Invisible ☐ Visible ☐
092B	Measure’t Setup	Invisible ☐ Visible ☐
092C	Comms Settings	Invisible ☐ Visible ☐
092D	Commissioning Tests	Invisible ☐ Visible ☐
092E	Setting Values	Primary ☐ Secondary ☐
092F	Control Inputs	Invisible ☐ Visible ☐
0930	CLIO Inputs	Disabled ☐ Enabled ☐
0931	CLIO Outputs	Disabled ☐ Enabled ☐
0935	Ctrl I/P Config	Invisible ☐ Visible ☐
0936	Ctrl I/P Labels	Invisible ☐ Visible ☐
0939	Direct Access	Invisible ☐ Visible ☐
0949	IEC GOOSE	Invisible ☐ Visible ☐
0950	Function Keys	Invisible ☐ Visible ☐
09FF	LCD Contrast	

10.7 0A00 - CT AND VT RATIOS

0A00	CT AND VT RATIOS	
0A01	Main VT Location	
0A03	Main VT Primary	
0A04	Main VT Sec’y	
0A07	Aux’ VT Primary	
0A08	Aux’ VT Sec’y	
0A10	T1 CT	
0A11	Polarity	
0A12	Primary	
0A13	Secondary	
0A14	T2 CT	
0A15	Polarity	
0A16	Primary	
0A17	Secondary	
0A18	T3 CT	
0A19	Polarity	
0A1A	Primary	
0A1B	Secondary	
0A1C	T4 CT	
0A1D	Polarity	
0A1E	Primary	
0A1F	Secondary	
0A20	T5 CT	
0A21	Polarity	
0A22	Primary	
0A23	Secondary	
0A58	TN1 CT	
0A59	Polarity	
0A5A	Primary	
0A5B	Secondary	
0A5D	TN2 CT	
0A5E	Polarity	
0A5F	Primary	
0A60	Secondary	
0A62	TN3 CT	
0A63	Polarity	
0A64	Primary	
0A65	Secondary	

10.8 0B00 - Record Control

0B00	RECORD CONTROL	
0B01	Clear Events	

0B00	RECORD CONTROL	
0B02	Clear Faults	
0B03	Clear Maint	
0B04	Alarm Event	Disabled ☐ Enabled ☐
0B05	Relay O/P Event	Disabled ☐ Enabled ☐
0B06	Opto Input Event	Disabled ☐ Enabled ☐
0B07	General Event	Disabled ☐ Enabled ☐
0B08	Fault Rec Event	Disabled ☐ Enabled ☐
0B09	Maint Rec Event	Disabled ☐ Enabled ☐
0B0A	Protection Event	Disabled ☐ Enabled ☐
0B030	Clear Disc Recs	
0B40	DDB 31 - 0	
0B41	DDB 63 - 32	
0B42	DDB 95 - 64	
0B43	DDB 127 - 96	
0B44	DDB 159 - 128	
0B45	DDB 191 - 160	
0B46	DDB 223 - 192	
0B47	DDB 255 - 224	
0B48	DDB 287 - 256	
0B49	DDB 319 - 288	
0B4A	DDB 351 - 320	
0B4B	DDB 383 - 352	
0B4C	DDB 415 - 384	
0B4D	DDB 447 - 416	
0B4E	DDB 479 - 448	
0B4F	DDB 511 - 480	
0B50	DDB 543 - 512	
0B51	DDB 575 - 544	
0B52	DDB 607 - 576	
0B53	DDB 639 - 608	
0B54	DDB 671 - 640	
0B55	DDB 703 - 672	
0B56	DDB 735 - 704	
0B57	DDB 767 - 736	
0B58	DDB 799 - 768	
0B59	DDB 831 - 800	
0B5A	DDB 863 - 832	
0B5B	DDB 895 - 864	
0B5C	DDB 927 - 896	
0B5D	DDB 959 - 928	
0B5E	DDB 991 - 960	
0B5F	DDB 1023 - 992	
0B60	DDB 1055-1024	
0B61	DDB 1087-1056	

0B00	RECORD CONTROL	
0B62	DDB 1119-1088	
0B63	DDB 1151-1120	
0B64	DDB 1183-1152	
0B65	DDB 1215-1184	
0B66	DDB 1247-1216	
0B67	DDB 1279-1248	
0B68	DDB 1311-1280	
0B69	DDB 1343-1312	
0B6A	DDB 1375-1344	
0B6B	DDB 1407-1376	
0B6C	DDB 1439-1408	
0B6D	DDB 1471-1440	
0B6E	DDB 1503-1472	
0B6F	DDB 1535-1504	
0B70	DDB 1567-1536	
0B71	DDB 1599-1568	
0B72	DDB 1631-1600	
0B73	DDB 1663-1632	
0B74	DDB 1695-1664	
0B75	DDB 1727-1696	
0B76	DDB 1759-1728	
0B77	DDB 1791-1760	
0B78	DDB 1823-1792	
0B79	DDB 1855-1824	
0B7A	DDB 1887-1856	
0B7B	DDB 1919-1888	
0B7C	DDB 1951-1920	
0B7D	DDB 1983-1952	
0B7E	DDB 2015-1984	
0B7F	DDB 2047-2016	

10.9 0C00 - Disturb. Recorder

0C00	DISTURB. RECORDER	
0C52	Duration	
0C54	Trigger Position	
0C56	Trigger Mode	Single ☐ Extended ☐
0C58	Analog Channel 1	
0C59	Analog Channel 2	
0C5A	Analog Channel 3	
0C5B	Analog Channel 4	
0C5C	Analog Channel 5	
0C5D	Analog Channel 6	
0C5E	Analog Channel 7	

0C00	DISTURB. RECORDER	
0C5F	Analog Channel 8	
0C60	Analog Channel 9	
0C61	Analog Channel 10	
0C62	Analog Channel 11	
0C63	Analog Channel 12	
0C64	Analog Channel 13	
0C65	Analog Channel 14	
0C66	Analog Channel 15	
0C67	Analog Channel 16	
0C68	Analog Channel 17	
0C69	Analog Channel 18	
0C6A	Analog Channel 19	
0C6B	Analog Channel 20	
0C6C	Analog Channel 21	
0C6D	Analog Channel 22	
0C6E	Analog Channel 23	
0C6F	Analog Channel 24	
0C70	Analog Channel 25	
0C71	Analog Channel 26	
0C72	Analog Channel 27	
0C73	Analog Channel 28	
0C74	Analog Channel 29	
0C75	Analog Channel 30	
0C80	Digital Input 1	
0C81	Input 1 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0C82	Digital Input 2	
0C83	Input 2 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0C84	Digital Input 3	
0C85	Input 3 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0C86	Digital Input 4	
0C87	Input 4 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0C88	Digital Input 5	
0C89	Input 5 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0C8A	Digital Input 6	
0C8B	Input 6 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0C8C	Digital Input 7	
0C8D	Input 7 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0C8E	Digital Input 8	
0C8F	Input 8 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0C90	Digital Input 9	
0C91	Input 9 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0C92	Digital Input 10	
0C93	Input 10 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0C94	Digital Input 11	

0C00	DISTURB. RECORDER	
0C95	Input 11 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0C96	Digital Input 12	
0C97	Input 12 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0C98	Digital Input 13	
0C99	Input 13 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0C9A	Digital Input 14	
0C9B	Input 14 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0C9C	Digital Input 15	
0C9D	Input 15 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0C9E	Digital Input 16	
0C9F	Input 16 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CA0	Digital Input 17	
0CA1	Input 17 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CA2	Digital Input 18	
0CA3	Input 18 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CA4	Digital Input 19	
0CA5	Input 19 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CA6	Digital Input 20	
0CA7	Input 20 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CA8	Digital Input 21	
0CA9	Input 21 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CAA	Digital Input 22	
0CAB	Input 22 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CAC	Digital Input 23	
0CAD	Input 23 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CAE	Digital Input 24	
0CAF	Input 24 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CB0	Digital Input 25	
0CB1	Input 25 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CB2	Digital Input 26	
0CB3	Input 26 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CB4	Digital Input 27	
0CB5	Input 27 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CB6	Digital Input 28	
0CB7	Input 28 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CB8	Digital Input 29	
0CB9	Input 29 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CBA	Digital Input 30	
0CBB	Input 30 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CBC	Digital Input 31	
0CBD	Input 31 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐
0CBE	Digital Input 32	
0CBF	Input 32 Trigger	No Trigger ☐ Trigger L - H ☐ Trigger H - L ☐

10.10 0D00 - Measure’t. Setup

0D00	MEASURE’T. SETUP	
0D01	Default Display	3Ph + N Current 3Ph Voltage Power Date & Time Description Plant Reference Frequency Access Level
0D02	Local Values	Primary ☐ Secondary ☐
0D03	Remote Values	Primary ☐ Secondary ☐
0D04	Measurement Ref	VA ☐ VB ☐ VC ☐ IA ☐ IB ☐ IC ☐
0D05	Measurement Mode	

10.11 0E00 - Communications

0E00	COMMUNICATIONS	
0E01	RP1 Protocol	Courier ☐ IEC870-5-103 ☐ MODBUS ☐ DNP3.0 ☐
0E02	RP1 Address	
0E03	RP1 Inactivity Timer	
0E04	RP1 Baud Rate	1200 ☐ 2400 ☐ 4800 ☐ 9600 ☐ 19200 ☐ 38400 ☐
0E05	RP1 Parity	Odd ☐ Even ☐ None ☐
0E06	RP1 Measure’t Period	
0E07	RP1 Physical Link	Copper ☐ Fiber Optic ☐
0E08	RP1 Time Sync	Disabled ☐ Enabled ☐
0E09	MODBUS IEC Time	Standard ☐ Reverse ☐
0E0A	RP1 CS103 Blocking	Disabled ☐ Monitor Blocking ☐ Command Blocking ☐
0E0B	RP1 Card Status	K Bus OK ☐ EIA(RS)485 OK ☐ Fiber Optic OK ☐
0E0C	RP1 Port Config	EIA(RS)232 ☐ EIA(RS)485 ☐ K-Bus ☐
0E8D	RP1 Comms. Mode	IEC60870 FT1.2 ☐ 10-bit No Parity ☐
0E0E	RP1 Baud Rate	
0E11	DNP need time	
0E12	DNP app fragment	
0E13	DNP app timeout	
0E14	DNP SBO timeout	
0E15	DNP link timeout	
0E1F	NIC Protocol	
0E22	NIC MAC Address	

0E00	COMMUNICATIONS	
0E64	NIC Tunl Timeout	
0E6A	NIC Link Report	Alarm ☐ Event ☐ None ☐
0E6B	NIC Link Timeout	
0E80	REAR PORT2 (RP2)	
0E81	RP2 Protocol	Courier ☐
0E84	RP2 Card Status	Unsupported ☐ Card Not Fitted ☐ EIA(RS)232 OK ☐ EIA(RS)485 OK ☐ K-Bus OK ☐
0E88	RP2 Port Config	EIA(RS)232 ☐ EIA(RS)485 ☐ K-Bus OK ☐
0E8A	RP2 Comms Mode	IEC60870 FT1.2 ☐ 10-bit No Parity ☐
0E90	RP2 Address	
0E92	RP2 Inactive Timer	
0E94	RP2 Baud Rate	1200 ☐ 2400 ☐ 4800 ☐ 9600 ☐ 19200 ☐ 38400 ☐
0EB1	DNP need time	
0EB2	DNP app fragment	
0EB3	DNP app timeout	
0EB4	DNP SBO timeout	

10.12 0F00 - Commission Tests

0F00	COMMISSION TESTS	
0F01	Opto I/P Status	
0F03	Rly O/P Status	
0F05	Test Port Status	
0F07	Monitor Bit 1	
0F08	Monitor Bit 2	
0F09	Monitor Bit 3	
0F0A	Monitor Bit 4	
0F0B	Monitor Bit 5	
0F0C	Monitor Bit 6	
0F0D	Monitor Bit 7	
0F0E	Monitor Bit 8	
0F0F	Test Mode	Test Mode ☐ Contacts Blocked ☐
0F10	Test Pattern	
0F11	Contact Test	
0F12	Test Leds	
0F15	Red Led Status	
0F16	Green Led Status	
0F20	DDB 31 - 0	
0F21	DDB 63 - 32	
0F22	DDB 95 - 64	

0F00	COMMISSION TESTS	
0F23	DDB 127 - 96	
0F24	DDB 159 - 128	
0F25	DDB 191 - 160	
0F26	DDB 223 - 192	
0F27	DDB 255 - 224	
0F28	DDB 287 - 256	
0F29	DDB 319 - 288	
0F2A	DDB 351 - 320	
0F2B	DDB 383 - 352	
0F2C	DDB 415 - 384	
0F2D	DDB 447 - 416	
0F2E	DDB 479 - 448	
0F2F	DDB 511 - 480	
0F30	DDB 543 - 512	
0F31	DDB 575 - 544	
0F32	DDB 607 - 576	
0F33	DDB 639 - 608	
0F34	DDB 671 - 640	
0F35	DDB 703 - 672	
0F36	DDB 735 - 704	
0F37	DDB 767 - 736	
0F38	DDB 799 - 768	
0F39	DDB 831 - 800	
0F3A	DDB 863 - 832	
0F3B	DDB 895 - 864	
0F3C	DDB 927 - 896	
0F3D	DDB 959 - 928	
0F3E	DDB 991 - 960	
0F3F	DDB 1023 - 992	
0F40	DDB 1055-1024	
0F41	DDB 1087-1056	
0F42	DDB 1119-1088	
0F43	DDB 1151-1120	
0F44	DDB 1183-1152	
0F45	DDB 1215-1184	
0F46	DDB 1247-1216	
0F47	DDB 1279-1248	
0F48	DDB 1311-1280	
0F49	DDB 1343-1312	
0F4A	DDB 1375-1344	
0F4B	DDB 1407-1376	
0F4C	DDB 1439-1408	
0F4D	DDB 1471-1440	
0F4E	DDB 1503-1472	

0F00	COMMISSION TESTS	
0F4F	DDB 1535-1504	
0F50	DDB 1567-1536	
0F51	DDB 1599-1568	
0F52	DDB 1631-1600	
0F53	DDB 1663-1632	
0F54	DDB 1695-1664	
0F55	DDB 1727-1696	
0F56	DDB 1759-1728	
0F57	DDB 1791-1760	
0F58	DDB 1823-1792	
0F59	DDB 1855-1824	
0F5A	DDB 1887-1856	
0F5B	DDB 1919-1888	
0F5C	DDB 1951-1920	
0F5D	DDB 1983-1952	
0F5E	DDB 2015-1984	
0F5F	DDB 2047-2016	

10.13 1100 - Opto Config

1100	OPTO CONFIG	
1101	Nominal V	24-27 V ☐ 30-34 V ☐ 48-54 V ☐ 110-125 V ☐ 220-250 V ☐ Custom
1102	Opto Input 1	24-27 V ☐ 30-34 V ☐ 48-54 V ☐ 110-125 V ☐ 220-250 V ☐
1103	Opto Input 2	24-27 V ☐ 30-34 V ☐ 48-54 V ☐ 110-125 V ☐ 220-250 V ☐
1104	Opto Input 3	24-27 V ☐ 30-34 V ☐ 48-54 V ☐ 110-125 V ☐ 220-250 V ☐
1105	Opto Input 4	24-27 V ☐ 30-34 V ☐ 48-54 V ☐ 110-125 V ☐ 220-250 V ☐
1106	Opto Input 5	24-27 V ☐ 30-34 V ☐ 48-54 V ☐ 110-125 V ☐ 220-250 V ☐
1107	Opto Input 6	24-27 V ☐ 30-34 V ☐ 48-54 V ☐ 110-125 V ☐ 220-250 V ☐
1108	Opto Input 7	24-27 V ☐ 30-34 V ☐ 48-54 V ☐ 110-125 V ☐ 220-250 V ☐
1109	Opto Input 8	24-27 V ☐ 30-34 V ☐ 48-54 V ☐ 110-125 V ☐ 220-250 V ☐
110A	Opto Input 9	24-27 V ☐ 30-34 V ☐ 48-54 V ☐ 110-125 V ☐ 220-250 V ☐
110B	Opto Input 10	24-27 V ☐ 30-34 V ☐ 48-54 V ☐ 110-125 V ☐ 220-250 V ☐
110C	Opto Input 11	24-27 V ☐ 30-34 V ☐ 48-54 V ☐ 110-125 V ☐ 220-250 V ☐
110D	Opto Input 12	24-27 V ☐ 30-34 V ☐ 48-54 V ☐ 110-125 V ☐ 220-250 V ☐

1100	**OPTO CONFIG**			
110E	Opto Input 13	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
110F	Opto Input 14	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
1110	Opto Input 15	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
1111	Opto Input 16	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
1112	Opto Input 17	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
1113	Opto Input 18	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
1114	Opto Input 19	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
1115	Opto Input 20	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
1116	Opto Input 21	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
1117	Opto Input 22	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
1118	Opto Input 23	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
1119	Opto Input 24	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
111A	Opto Input 25	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
111B	Opto Input 26	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
111C	Opto Input 27	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
111D	Opto Input 28	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
111E	Opto Input 29	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
111F	Opto Input 30	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
1120	Opto Input 31	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐
1121	Opto Input 32	24-27 V ☐ 110-125 V ☐	30-34 V ☐ 220-250 V	48-54 V ☐ ☐

1150	Opto Filter Ctrl																
1180	Characteristic	Standard 60% - 80% ☐	50% - 70% ☐														

10.14 1200 - Control Inputs

1200 CONTROL INPUTS		
1201	Ctrl I/P Status	
1202	Control Input 1	

1200 CONTROL INPUTS		
1203	Control Input 2	
1204	Control Input 3	
1205	Control Input 4	
1206	Control Input 5	
1207	Control Input 6	
1208	Control Input 7	
1209	Control Input 8	
120A	Control Input 9	
120B	Control Input 10	
120C	Control Input 11	
120D	Control Input 12	
120E	Control Input 13	
120F	Control Input 14	
121	Control Input 15	
1211	Control Input 16	
1212	Control Input 17	
1213	Control Input 18	
1214	Control Input 19	
1215	Control Input 20	
1216	Control Input 21	
1217	Control Input 22	
12.18	Control Input 23	
12.19	Control Input 24	
12.1A	Control Input 25	
12.1B	Control Input 26	
12.1C	Control Input 27	
12.1D	Control Input 28	
12.1E	Control Input 29	
12.1F	Control Input 30	
12.2	Control Input 31	
12.21	Control Input 32	

10.15 1300 - Ctrl I/P Config

1300	CTRL I/P CONFIG																
1301	Hotkey Enabled																

1300	CTRL I/P CONFIG	
1310	Control Input 1	Latched ☐ Pulsed ☐
1311	Ctrl Command 1	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1314	Control Input 2	Latched ☐ Pulsed ☐
1315	Ctrl Command 2	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1318	Control Input 3	Latched ☐ Pulsed ☐
1319	Ctrl Command 3	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
131C	Control Input 4	Latched ☐ Pulsed ☐
131D	Ctrl Command 4	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1320	Control Input 5	Latched ☐ Pulsed ☐
1321	Ctrl Command 5	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1324	Control Input 6	Latched ☐ Pulsed ☐
1325	Ctrl Command 6	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1328	Control Input 7	Latched ☐ Pulsed ☐
1329	Ctrl Command 7	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
132C	Control Input 8	Latched ☐ Pulsed ☐
132D	Ctrl Command 8	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1330	Control Input 9	Latched ☐ Pulsed ☐
1331	Ctrl Command 9	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1334	Control Input 10	Latched ☐ Pulsed ☐
1335	Ctrl Command 10	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1338	Control Input 11	Latched ☐ Pulsed ☐
1339	Ctrl Command 11	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
133C	Control Input 12	Latched ☐ Pulsed ☐
133D	Ctrl Command 12	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1340	Control Input 13	Latched ☐ Pulsed ☐
1341	Ctrl Command 13	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1344	Control Input 14	Latched ☐ Pulsed ☐
1345	Ctrl Command 14	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1348	Control Input 15	Latched ☐ Pulsed ☐
1349	Ctrl Command 15	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐

1300	CTRL I/P CONFIG	
134C	Control Input 16	Latched ☐ Pulsed ☐
134D	Ctrl Command 16	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1350	Control Input 17	Latched ☐ Pulsed ☐
1351	Ctrl Command 17	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1354	Control Input 18	Latched ☐ Pulsed ☐
1355	Ctrl Command 18	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1358	Control Input 19	Latched ☐ Pulsed ☐
1359	Ctrl Command 19	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
135C	Control Input 20	Latched ☐ Pulsed ☐
135D	Ctrl Command 20	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1360	Control Input 21	Latched ☐ Pulsed ☐
1361	Ctrl Command 21	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1364	Control Input 22	Latched ☐ Pulsed ☐
1365	Ctrl Command 22	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1368	Control Input 23	Latched ☐ Pulsed ☐
1369	Ctrl Command 23	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
136C	Control Input 24	Latched ☐ Pulsed ☐
136D	Ctrl Command 24	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1370	Control Input 25	Latched ☐ Pulsed ☐
1371	Ctrl Command 25	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1374	Control Input 26	Latched ☐ Pulsed ☐
1375	Ctrl Command 26	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1378	Control Input 27	Latched ☐ Pulsed ☐
1379	Ctrl Command 27	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
137C	Control Input 28	Latched ☐ Pulsed ☐
137D	Ctrl Command 28	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1380	Control Input 29	Latched ☐ Pulsed ☐
1381	Ctrl Command 29	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
1384	Control Input 30	Latched ☐ Pulsed ☐
1385	Ctrl Command 30	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐

1300	CTRL I/P CONFIG	
1388	Control Input 31	Latched ☐ Pulsed ☐
1389	Ctrl Command 31	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐
138C	Control Input 32	Latched ☐ Pulsed ☐
138D	Ctrl Command 32	On/Off ☐ Set/Reset ☐ In/Out ☐ Enabled/Disabled ☐

10.16 1700 - Function Keys

1700	FUNCTION KEYS	
1701	Fn. Key Status	Locked ☐ Disabled☐
1702	Fn. Key 1	Unlocked ☐ Locked ☐ Disabled☐
1703	Fn. Key 1 Mode	Normal ☐ Toggled ☐
1704	Fn. Key 1 Label	
1705	Fn. Key 2	Unlocked ☐ Locked ☐ Disabled☐
1706	Fn. Key 2 Mode	Normal ☐ Toggled ☐
1707	Fn. Key 2 Label	
1708	Fn. Key 3	Unlocked ☐ Locked ☐ Disabled☐
1709	Fn. Key 3 Mode	Normal ☐ Toggled ☐
170A	Fn. Key 3 Label	
170B	Fn. Key 4	Unlocked ☐ Locked ☐ Disabled☐
170C	Fn. Key 4 Mode	Normal ☐ Toggled ☐
170D	Fn. Key 4 Label	
170E	Fn. Key 5	Unlocked ☐ Locked ☐ Disabled☐
170F	Fn. Key 5 Mode	Normal ☐ Toggled ☐
1710	Fn. Key 5 Label	
1711	Fn. Key 6	Unlocked ☐ Locked ☐ Disabled☐
1712	Fn. Key 6 Mode	Normal ☐ Toggled ☐
1713	Fn. Key 6 Label	
1714	Fn. Key 7	Unlocked ☐ Locked ☐ Disabled☐
1715	Fn. Key 7 Mode	Normal ☐ Toggled ☐
1716	Fn. Key 7 Label	
1717	Fn. Key 8	Unlocked ☐ Locked ☐ Disabled☐
1718	Fn. Key 8 Mode	Normal ☐ Toggled ☐
1719	Fn. Key 8 Label	
171A	Fn. Key 9	Unlocked ☐ Locked ☐ Disabled☐
171B	Fn. Key 9 Mode	Normal ☐ Toggled ☐
171C	Fn. Key 9 Label	
171D	Fn. Key 10	Unlocked ☐ Locked ☐ Disabled☐
171E	Fn. Key 10 Mode	Normal ☐ Toggled ☐
171F	Fn. Key 10 Label	

10.17 1900 - IED Configurator

1900	IED CONFIGURATOR	
1905	Switch Conf.Bank	
190A	Restore MCL	
1910	Active Conf.Name	
1911	Active Conf.Rev	
1920	Inact.Conf.Name	
1921	Inact.Conf.Rev	
1930	IP PARAMETERS	
1931	IP Address	
1932	Subnet Address	
1933	Gateway	
1940	SNTP PARAMETERS	
1941	SNTP Server 1	
1942	SNTP Server 2	
1950	IEC 61850 SCL	
1951	IED Name	
1960	IEC 61850 GOOSE	
1961	GoID	
1970	GoEna	
1971	Test Mode	
1972	VOP Test Pattern	
1973	Ignore Test Flag	

10.18 2800 - User Alarms

2800	USER ALARMS	
2801	Manual Reset	
2810	Labels	
2811	User Alarm 1	
2812	User Alarm 2	
2813	User Alarm 3	
2814	User Alarm 4	
2815	User Alarm 5	
2816	User Alarm 6	
2817	User Alarm 7	
2818	User Alarm 8	
2819	User Alarm 9	
281A	User Alarm 10	
281B	User Alarm 11	
281C	User Alarm 12	
281D	User Alarm 13	
281E	User Alarm 14	
281F	User Alarm 15	

2800	USER ALARMS	
2820	User Alarm 16	
2821	User Alarm 17	
2822	User Alarm 18	
2823	User Alarm 19	
2824	User Alarm 20	
2825	User Alarm 21	
2826	User Alarm 22	
2827	User Alarm 23	
2828	User Alarm 24	
2829	User Alarm 25	
282A	User Alarm 26	
282B	User Alarm 27	
282C	User Alarm 28	
282D	User Alarm 29	
282E	User Alarm 30	
282F	User Alarm 31	
2830	User Alarm 32	

10.19 2900 - Ctrl I/P Labels

2900	CTRL I/P LABELS	
2901	Control Input 1	
2902	Control Input 2	
2903	Control Input 3	
2904	Control Input 4	
2905	Control Input 5	
2906	Control Input 6	
2907	Control Input 7	
2908	Control Input 8	
2909	Control Input 9	
290A	Control Input 10	
290B	Control Input 11	
290C	Control Input 12	
290D	Control Input 13	
290E	Control Input 14	
290F	Control Input 15	
2910	Control Input 16	
2911	Control Input 17	
2912	Control Input 18	
2913	Control Input 19	
2914	Control Input 20	
2915	Control Input 21	
2916	Control Input 22	
2917	Control Input 23	

2900	CTRL I/P LABELS	
2918	Control Input 24	
2919	Control Input 25	
291A	Control Input 26	
291B	Control Input 27	
291C	Control Input 28	
291D	Control Input 29	
291E	Control Input 30	
291F	Control Input 31	
2920	Control Input 32	

10.20 B700 - PSL Data

B700	PSL DATA	
B701	Grp 1 PSL Ref	
B702	Date/Time	
B703	Grp 1 PSL ID	
B711	Grp 2 PSL Ref	
B712	Date/Time	
B713	Grp 2 PSL ID	
B721	Grp 3 PSL Ref	
B722	Date/Time	
B723	Grp 3 PSL ID	
B731	Grp 4 PSL Ref	
B732	Date/Time	
B733	Grp 4 PSL ID	

10.21 Protection Settings:

Protection Settings:

- Group 1 protection settings use 3000/4000 Courier cell addresses
- Group 2 protection settings use 5000/6000 Courier cell addresses
- Group 3 protection settings use 7000/8000 Courier cell addresses
- Group 4 protection settings use 9000/A000 Courier cell addresses

10.22 3000 - System Config

3000	SYSTEM CONFIG	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
3001	Winding Config				
3002	Winding Type				
3003	HV CT Terminals				
3004	LV CT Terminals				

3000	SYSTEM CONFIG	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
3005	TV CT Terminals				
3007	Sref				
3008	HV Connection				
3009	HV Grounding				
300A	HV Nominal				
300B	HV Rating				
300C	% Reactance				
300D	LV Vector Group				
300E	LV Connection				
300F	LV Grounding				
3010	LV Nominal				
3011	LV Rating				
3012	TV Vector Group				
3013	TV Connection				
3014	TV Grounding				
3015	TV Nominal				
3016	TV Rating				
3020	Match Factor CT1				
3021	Match Factor CT2				
3022	Match Factor CT3				
3023	Match Factor CT4				
3024	Match Factor CT5				
305E	Phase Sequence				
305F	VT Reversal				
3060	CT1 Reversal				
3061	CT2 Reversal				
3062	CT3 Reversal				
3063	CT4 Reversal				
3064	CT5 Reversal				

10.23 3100 - Diff Protection

3100	DIFF PROTECTION	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
3101	Trans Diff				
3102	Set Mode				
3103	Is1				
3104	K1				
3105	Is2				
3106	K2				
3107	tDiff LS				
3108	Is-CTS				
3110	Is-HS1				

3100	DIFF PROTECTION	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
3111	HS2 Status				
3112	Is-HS2				
3120	Zero seq filt HV				
3121	Zero seq filt LV				
3122	Zero seq filt TV				
3128	2nd harm blocked				
3129	Ih(2)%>				
312A	Cross blocking				
312B	CTSat and NoGap				
3133	5th harm blocked				
3134	Ih(5)%>				
3140	Circuitry Fail				
3141	Is-cctfail				
3142	K-cctfail				
3143	tls-cctfail				

10.24 3200 - REF Protection

3200	REF PROTECTION				
Group 1 settings		Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
3201	REF HV status				
3202	HV CT Input				
3203	HV IS1 Set				
3204	HV IS2 Set				
3205	HV IREF K1				
3206	HV IREF K2				
3207	HV tREF				
3220	REF LV status				
3221	LV CT Input				
3222	LV IS1 Set				
3223	LV IS2 Set				
3224	LV IREF K1				
3225	LV IREF K2				
3226	LV tREF				
3230	REF TV status				
3231	TV CT Input				
3232	TV IS1 Set				
3233	TV IS2 Set				
3234	TV IREF K1				
3235	TV IREF K2				
3236	TV tREF				
3240	REF AUTO status				

3200	REF PROTECTION				
Group 1 settings		Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
3241	AUTO CT Input				
3242	AUTO IS1 Set				
3243	AUTO IS2 Set				
3244	AUTO IREF K1				
3245	AUTO IREF K2				
3246	AUTO tREF				

10.25 3400 - NPS Overcurrent

3400	NPS OVERCURRENT	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
3401	NPS O/C 1				
3402	I2>1 Status				
3403	I2>1 Char				
3404	I2>1 Directional				
3405	I2>1 Current Set				
3406	I2>1 Time Delay				
3407	I2>1 TMS				
3408	I2>1 Time Dial				
3409	I2>1 k(RI)				
340A	I2>1 Reset Char				
340B	I2>1 TReset				
3412	I2>2 Status				
3413	I2>2 Char				
3414	I2>2 Direction				
3415	I2>2 Current Set				
3416	I2>2 Time Delay				
3417	I2>2 TMS				
3418	I2>2 Time Dial				
3419	I2>2 k(RI)				
341A	I2>2 Reset Char				
341B	I2>2 TReset				
3421	I2>3 Status				
3422	I2>3 Direction				
3423	I2>3 Current Set				
3424	I2>3 Time Delay				
3427	I2>4 Status				
3428	I2>4 Direction				
3429	I2>4 Current Set				
342A	I2>4 Time Delay				
342D	I2> VTS Block				
342E	I2> V2pol Set				

3400	**NPS OVERCURRENT**	**Group 1 settings**	**Group 2 settings**	**Group 3 settings**	**Group 4 settings**
Group 1 settings					
342F	I2> Char Angle				
3431	NPS O/C 2				
3432	I2>1 Status				
3433	I2>1 Char				
3434	I2>1 Directional				
3435	I2>1 Current Set				
3436	I2>1 Time Delay				
3437	I2>1 TMS				
3438	I2>1 Time Dial				
3439	I2>1 k(RI)				
343A	I2>1 Reset Char				
343B	I2>1 TReset				
3442	I2>2 Status				
3443	I2>2 Char				
3444	I2>2 Direction				
3445	I2>2 Current Set				
3446	I2>2 Time Delay				
3447	I2>2 TMS				
3448	I2>2 Time Dial				
3449	I2>2 k(RI)				
344A	I2>2 Reset Char				
344B	I2>2 TReset				
3451	I2>3 Status				
3455	I2>3 Direction				
3453	I2>3 Current Set				
3454	I2>3 Time Delay				
3457	I2>4 Status				
3458	I2>4 Direction				
3459	I2>4 Current Set				
345A	I2>4 Time Delay				
345D	I2> VTS Block				
345E	I2> V2pol Set				
345F	I2> Char Angle				
3461	NPS O/C 3				
3462	I2>1 Status				
3463	I2>1 Char				
3464	I2>1 Directional				
3465	I2>1 Current Set				
3466	I2>1 Time Delay				
3467	I2>1 TMS				
3468	I2>1 Time Dial				
3469	I2>1 k(RI)				
346A	I2>1 Reset Char				

3400	NPS OVERCURRENT	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
346B	I2>1 TReset				
3472	I2>2 Status				
3473	I2>2 Char				
3474	I2>2 Direction				
3475	I2>2 Current Set				
3476	I2>2 Time Delay				
3477	I2>2 TMS				
3478	I2>2 Time Dial				
3479	I2>2 k(RI)				
347A	I2>2 Reset Char				
347B	I2>2 TReset				
3481	I2>3 Status				
3485	I2>3 Direction				
3483	I2>3 Current Set				
3484	I2>3 Time Delay				
3487	I2>4 Status				
3488	I2>4 Direction				
3489	I2>4 Current Set				
348A	I2>4 Time Delay				
348D	I2> VTS Block				
348E	I2> V2pol Set				
348F	I2> Char Angle				

10.26 3500 - Overcurrent

3500	OVERCURRENT	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
3501	Overcurrent1				
3502	I>1 Status				
3503	I>1 Char				
3504	I>1 Direction				
3505	I>1 Current Set				
3506	I>1 Time Delay				
3507	I>1 TMS				
3508	I>1 Time Dial				
3509	I>1 K (RI)				
350A	I>1 Reset Char				
350B	I>1 tRESET				
3512	I>2 Status				
3513	I>1 Char				
3514	I>2 Direction				
3515	I>2 Current Set				
3516	I>2 Time Delay				

3500	OVERCURRENT	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
3517	I>2 TMS				
3518	I>2 Time Dial				
3519	I>2 K (RI)				
351A	I>2 Reset Char				
351B	I>2 tRESET				
3521	I>3 Status				
3522	I>3 Direction				
3523	I>3 Current Set				
3524	I>3 Time Delay				
3527	I>4 Status				
3528	I>4 Direction				
3529	I>4 Current Set				
352A	I>4 Time Delay				
352D	I> Char Angle				
352E	I> Function Link				
3531	Overcurrent2				
3532	I>1 Status				
3533	I>1 Char				
3534	I>1 Direction				
3535	I>1 Current Set				
3536	I>1 Time Delay				
3537	I>1 TMS				
3538	I>1 Time Dial				
3539	I>1 K (RI)				
353A	I>1 Reset Char				
353B	I>1 tRESET				
3542	I>2 Status				
3543	I>1 Char				
3544	I>2 Direction				
3545	I>2 Current Set				
3546	I>2 Time Delay				
3547	I>2 TMS				
3548	I>2 Time Dial				
3549	I>2 K (RI)				
354A	I>2 Reset Char				
354B	I>2 tRESET				
3551	I>3 Status				
3552	I>3 Direction				
3553	I>1 Char				
3553	I>3 Current Set				
3554	I>3 Time Delay				
3557	I>4 Status				
3558	I>4 Direction				

3500	OVERCURRENT	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
3559	I>4 Current Set				
355A	I>4 Time Delay				
355D	I> Char Angle				
355E	I> Function Link				
3561	Overcurrent3				
3562	I>1 Status				
3563	I>1 Char				
3564	I>1 Direction				
3565	I>1 Current Set				
3566	I>1 Time Delay				
3567	I>1 TMS				
3568	I>1 Time Dial				
3569	I>1 K (RI)				
356A	I>1 Reset Char				
356B	I>1 tRESET				
3572	I>2 Status				
3574	I>2 Direction				
3575	I>2 Current Set				
3576	I>2 Time Delay				
3577	I>2 TMS				
3578	I>2 Time Dial				
3579	I>2 K (RI)				
357A	I>2 Reset Char				
357B	I>2 tRESET				
3581	I>3 Status				
3582	I>3 Direction				
3583	I>3 Current Set				
3584	I>3 Time Delay				
3587	I>4 Status				
3588	I>4 Direction				
3589	I>4 Current Set				
358A	I>4 Time Delay				
358D	I> Char Angle				
358E	I> Function Link				
3591	V CONTROLED O/C				
3592	VCO>1				
3593	VCO>1 Char				
3594	VCO>1 Direction				
3595	VCO>1 Curr' Set				
3596	VCO>1 Time Delay				
3597	VCO>1 TMS				
3598	VCO>1 Time Dial				
3599	VCO>1 k (RI)				

3500	OVERCURRENT	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
359A	VCO>1 Reset Char				
359B	VCO>1 tRESET				
359C	VCO>1 Angle				
359D	VCO>1 V<Setting				
359E	VCO>1 K Setting				
35A2	VCO>2				
35A3	VCO>2 Char				
35A4	VCO>2 Direction				
35A5	VCO>2 Curr' Set				
35A6	VCO>2 Time Delay				
35A7	VCO>2 TMS				
35A8	VCO>2 Time Dial				
35A9	VCO>2 k (RI)				
35AA	VCO>2 Reset Char				
35AB	VCO>2 tRESET				
35AC	VCO>2 Angle				
35AD	VCO>2 V<Setting				
35AE	VCO>2 K Setting				

10.27 3700 - Thermal Overload

3700	THERMAL OVERLOAD	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
3711	Monit'd winding				
3712	Ambient T				
3715	Amb CLIO Type				
3716	Amb CLIO Min				
3717	Amb CLIO Max				
3718	Average Amb T				
3721	Top Oil Temp				
3724	TOP CLIO Type				
3725	TOP CLIO Min				
3726	TOP CLIO Max				
3729	IB				
372A	Rated NoLoadLoss				
372B	Hot Spot Overtop				
372C	Top Oil Overamb				
372D	Cooling Mode				
372E	Cooling Status				
372F	Cooling Mode1				
3730	Winding exp m				
3731	Oil exp n				
3732	Cooling Mode2				

3700	THERMAL OVERLOAD	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
3733	Winding exp m				
3734	Oil exp n				
3735	Cooling Mode3				
3736	Winding exp m				
3737	Oil exp n				
3738	Cooling Mode4				
3739	Winding exp m				
373A	Oil exp n				
373B	Hot spot rise co				
373C	Top oil rise co				
3740	Thermal Overload Status				
375E	Hot Spot>1 Set				
375F	tHot Spot>1 Set				
3760	Hot Spot>2 Set				
3761	tHot Spot>2 Set				
3762	Hot Spot>3 Set				
3763	tHot Spot>3 Set				
3764	Top Oil>1 Set				
3765	tTop Oil>1 Set				
3766	Top Oil>2 Set				
3767	tTop Oil>2 Set				
3768	Top Oil>3 Set				
3769	tTop Oil>3 Set				
376A	tPre-trip Set				
3780	LOL Status				
3781	Life Hours at HS				
3782	Designed HS temp				
3783	Constant B Set				
3784	FAA> Set				
3785	tFAA> Set				
3786	LOL>1 Set				
3787	tLOL> Set				
3788	Reset Life Hours				

10.28 3800 - Earth Fault

3800	EARTH FAULT	Group 1 settings	Group 1 settings	Group 1 settings	Group 1 settings
Group 1 settings					
3801	Earth Fault 1				
3802	EF 1 Input				
3803	EF 1 Derived				
3804	EF 1 Measured				
3805	IN>1 Status				

3800	EARTH FAULT	Group 1 settings	Group 1 settings	Group 1 settings	Group 1 settings
Group 1 settings					
3806	IN>1 Char				
3807	IN>1 Direction				
3808	IN>1 Current				
3809	IN>1 IDG Is				
380A	IN>1 Time Delay				
380B	IN>1 TMS				
380C	IN>1 Time Dial				
380D	IN>1 k (RI)				
380E	IN>1 IDG Time				
380F	IN>1 Reset Char				
381	IN>1 tRESET				
3815	IN>2 Status				
3816	IN>2 Char				
3817	IN>2 Direction				
3818	IN>2 Current				
3819	IN>2 IDG Is				
381A	IN>2 Time Delay				
381B	IN>2 TMS				
381C	IN>2 Time Dial				
381D	IN>2 k (RI)				
381E	IN>2 IDG Time				
381F	IN>2 Reset Char				
382	IN>2 tRESET				
3825	IN>3 Status				
3826	IN>3 Direction				
3827	IN>3 Current				
3828	IN>3 Time Delay				
382C	IN>4 Status				
382D	IN>4 Direction				
382E	IN>4 Current				
382F	IN>4 Time Delay				
3833	IN> Func Link				
3834	IN> DIRECTIONAL				
3835	IN> Char Angle				
3836	IN> Pol				
3837	IN> VNpol Set				
3838	IN> V2pol Set				
3839	IN> I2pol Set				
3841	Earth Fault 2				
3842	EF 2 Input				
3843	EF 2 Derived				
3844	EF 2 Measured				
3845	IN>1 Status				

3800	**EARTH FAULT**	**Group 1 settings**	**Group 1 settings**	**Group 1 settings**	**Group 1 settings**
Group 1 settings					
3846	IN>1 Char				
3847	IN>1 Direction				
3848	IN>1 Current				
3849	IN>1 IDG Is				
384A	IN>1 Time Delay				
384B	IN>1 TMS				
384C	IN>1 Time Dial				
384D	IN>1 k (RI)				
384E	IN>1 IDG Time				
384F	IN>1 Reset Char				
385	IN>1 tRESET				
3855	IN>2 Status				
3856	IN>2 Char				
3857	IN>2 Direction				
3858	IN>2 Current				
3859	IN>2 IDG Is				
385A	IN>2 Time Delay				
385B	IN>2 TMS				
385C	IN>2 Time Dial				
385D	IN>2 k (RI)				
385E	IN>2 IDG Time				
385F	IN>2 Reset Char				
386	IN>2 tRESET				
3865	IN>3 Status				
3866	IN>3 Direction				
3867	IN>3 Current				
3868	IN>3 Time Delay				
386C	IN>4 Status				
386D	IN>4 Direction				
386E	IN>4 Current				
386F	IN>4 Time Delay				
3873	IN> Func Link				
3874	IN> DIRECTIONAL				
3875	IN> Char Angle				
3876	IN> Pol				
3877	IN> VNpol Set				
3878	IN> V2pol Set				
3879	IN> I2pol Set				
3881	Earth Fault 3				
3882	EF 3 Input				
3883	EF 3 Derived				
3884	EF 3 Measured				
3885	IN>1 Status				

3800	EARTH FAULT	Group 1 settings	Group 1 settings	Group 1 settings	Group 1 settings
Group 1 settings					
3886	IN>1 Char				
3887	IN>1 Direction				
3888	IN>1 Current				
3889	IN>1 IDG Is				
388A	IN>1 Time Delay				
388B	IN>1 TMS				
388C	IN>1 Time Dial				
388D	IN>1 k (RI)				
388E	IN>1 IDG Time				
388F	IN>1 Reset Char				
389	IN>1 tRESET				
3895	IN>2 Status				
3896	IN>2 Char				
3897	IN>2 Direction				
3898	IN>2 Current				
3899	IN>2 IDG Is				
389A	IN>2 Time Delay				
389B	IN>2 TMS				
389C	IN>2 Time Dial				
389D	IN>2 k (RI)				
389E	IN>2 IDG Time				
389F	IN>2 Reset Char				
38A0	IN>2 tRESET				
38A5	IN>3 Status				
38A6	IN>3 Direction				
38A7	IN>3 Current				
38A8	IN>3 Time Delay				
38AC	IN>4 Status				
38AD	IN>4 Direction				
38AE	IN>4 Current				
38AF	IN>4 Time Delay				
38B3	IN> Func Link				
38B4	IN> DIRECTIONAL				
38B5	IN> Char Angle				
38B6	IN> Pol				
38B7	IN> VNpol Set				
38B8	IN> V2pol Set				
38B9	IN> I2pol Set				

10.29 3900 - Through Fault Monitoring

3900	THROUGH FAULT MONITORING	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
3901	Through Fault				
3902	Monitored Input				
3903	TF I> Trigger				
3904	TF I2t> Alarm				

10.30 3B00 - Residual O/V NVD

3B00	RESIDUAL O/V NVD	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
3B14	VN>1 Function				
3B16	VN>1 Voltage Set				
3B18	VN>1 Time Delay				
3B1A	VN>1 TMS				
3B1C	VN>1 tReset				
3B20	VN>2 Status				
3B26	VN>2 Voltage Set				
3B28	VN>2 Time Delay				

10.31 3D00 - Overfluxing (V/Hz)

3D00	OVERFLUXING (V/Hz)	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
3D01	Volts/Hz W1				
3D02	V/Hz Alm Status				
3D03	V/Hz Alm Set				
3D04	V/Hz Alarm Delay				
3D10	V/Hz>1 Status				
3D13	V/Hz>1 Function				
3D16	V/Hz>1 Trip Set				
3D19	V/Hz>1 Trip TMS				
3D1A	V/Hz>1 Delay				
3D1B	V/Hz>1 tReset				
3D20	V/Hz>2 Status				
3D25	V/Hz>2 Trip Set				
3D2A	V/Hz>2 Delay				
3D30	V/Hz>3 Status				
3D35	V/Hz>3 Trip Set				
3D3A	V/Hz>3 Delay				
3D40	V/Hz>4 Status				
3D45	V/Hz>4 Trip Set				
3D4A	V/Hz>4 Delay				

3D00	OVERFLUXING (V/Hz)	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
3D4F	TPre-trip Alarm				
3D50	Volts/Hz W2				
3D51	V/Hz Alm Status				
3D52	V/Hz Alm Set				
3D53	V/Hz Alarm Delay				
3D60	V/Hz>1 Status				
3D63	V/Hz>1 Function				
3D66	V/Hz>1 Trip Set				
3D69	V/Hz>1 Trip TMS				
3D6A	V/Hz>1 Delay				
3D6B	V/Hz>1 tReset				
3D70	V/Hz>2 Status				
3D75	V/Hz>2 Trip Set				
3D7A	V/Hz>2 Delay				
3D80	V/Hz>3 Status				
3D85	V/Hz>3 Trip Set				
3D8A	V/Hz>3 Delay				
3D90	V/Hz>4 Status				
3D95	V/Hz>4 Trip Set				
3D9A	V/Hz>4 Delay				
3D9F	TPre-trip alarm				

10.32 4200 - Volt Protection

4200	VOLT PROTECTION	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
4201	UNDERVOLTAGE				
4202	V< Measur’t Mode				
4203	V< Operate Mode				
4204	V<1 Function				
4205	V<1 Voltage Set				
4206	V<1 Time Delay				
4207	V<1 TMS				
4208	V<1 Poledead Inhibit				
4209	V<2 Status				
420A	V<2 Voltage Set				
420B	V<2 Time Delay				
420C	V<2 Poledead Inhibit				
4220	OVERVOLTAGE				
4221	V> Measur’t Mode				
4222	V> Operate Mode				
4223	V>1 Function				
4224	V>1 Voltage Set				

4200	VOLT PROTECTION	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
4225	V>1 Time Delay				
4226	V>1 TMS				
4227	V>2 Status				
4228	V>2 Voltage Set				
4229	V>2 Time Delay				
4240	NPS O/V				
4241	V2> Status				
4242	V2> Voltage Set				
4243	V2> Time Delay				

10.33 4300 - Freq Protection

4300	FREQ PROTECTION	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
4301	Under Frequency				
4302	F<1 Status				
4303	F<1 Setting				
4304	F<1 Time Delay				
4305	F<2 Status				
4306	F<2 Setting				
4307	F<2 Time Delay				
4308	F<3 Status				
4309	F<3 Setting				
430A	F<3 Time Delay				
430B	F<4 Status				
430C	F<4 Setting				
430D	F<4 Time Delay				
430F	Over Frequency				
4310	F>1 Status				
4311	F>1 Setting				
4312	F>1 Time Delay				
4313	F>2 Status				
4314	F>2 Setting				
4315	F>2 Time Delay				

10.34 4400 - RTD Protection

4400	RTD PROTECTION	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
4401	Select RTD				
4402	RTD1 PROTECTION				
4403	RTD Alarm Set				

4400	**RTD PROTECTION**	**Group 1 settings**	**Group 2 settings**	**Group 3 settings**	**Group 4 settings**
Group 1 settings					
4404	RTD Alarm Dly				
4405	RTD Trip Set				
4406	RTD Trip Dly				
4407	RTD2 PROTECTION				
4408	RTD Alarm Set				
4409	RTD Alarm Dly				
440A	RTD Trip Set				
440B	RTD Trip Dly				
440C	RTD3 PROTECTION				
440D	RTD Alarm Set				
440E	RTD Alarm Dly				
440F	RTD Trip Set				
4410	RTD Trip Dly				
4411	RTD4 PROTECTION				
4412	RTD Alarm Set				
4413	RTD Alarm Dly				
4414	RTD Trip Set				
4415	RTD Trip Dly				
4416	RTD5 PROTECTION				
4417	RTD Alarm Set				
4418	RTD Alarm Dly				
4419	RTD Trip Set				
441A	RTD Trip Dly				
441B	RTD6 PROTECTION				
441C	RTD Alarm Set				
441D	RTD Alarm Dly				
441E	RTD Trip Set				
441F	RTD Trip Dly				
4420	RTD7 PROTECTION				
4421	RTD Alarm Set				
4422	RTD Alarm Dly				
4423	RTD Trip Set				
4424	RTD Trip Dly				
4425	RTD8 PROTECTION				
4426	RTD Alarm Set				
4427	RTD Alarm Dly				
4428	RTD Trip Set				
4429	RTD Trip Dly				
442A	RTD9 PROTECTION				
442B	RTD Alarm Set				
442C	RTD Alarm Dly				
442D	RTD Trip Set				
442E	RTD Trip Dly				

4400	RTD PROTECTION	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
442F	RTD 10 PROTECTION				
4430	RTD Alarm Set				
4431	RTD Alarm Dly				
4432	RTD Trip Set				
4433	RTD Trip Dly				

10.35 4500 - CB Fail

4500	CB Fail	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 Settings					
4501	T1 CBF Status				
4502	I< Current Set				
4503	IN< Status				
4504	IN< Input				
4505	IN< Terminal				
4506	IN< Current Set				
4507	CB Fail 1 Status				
4508	CB Fail 1 Timer				
4509	CB Fail 2 Status				
450A	CB Fail 2 Timer				
450C	CBF Non I Reset				
450D	CBF Ext Reset				
4511	T2 CBF Status				
4512	I< Current Set				
4513	IN< Status				
4514	IN< Input				
4515	IN< Terminal				
4516	IN< Current Set				
4517	CB Fail 1 Status				
4518	CB Fail 1 Timer				
4519	CB Fail 2 Status				
451A	CB Fail 2 Timer				
451C	CBF Non I Reset				
451D	CBF Ext Reset				
4521	T3 CBF Status				
4522	I< Current Set				
4523	IN< Status				
4524	IN< Input				
4525	IN< Terminal				
4526	IN< Current Set				
4527	CB Fail 1 Status				
4528	CB Fail 1 Timer				
4529	CB Fail 2 Status				

4500	CB Fail	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 Settings					
452A	CB Fail 2 Timer				
452C	CBF Non I Reset				
452D	CBF Ext Reset				
4531	T4 CBF Status				
4532	I< Current Set				
4533	IN< Status				
4534	IN< Input				
4535	IN< Terminal				
4536	IN< Current Set				
4537	CB Fail 1 Status				
4538	CB Fail 1 Timer				
4539	CB Fail 2 Status				
453A	CB Fail 2 Timer				
453C	CBF Non I Reset				
453D	CBF Ext Reset				
4541	T5 CBF Status				
4542	I< Current Set				
4543	IN< Status				
4544	IN< Input				
4545	IN< Terminal				
4546	IN< Current Set				
4547	CB Fail 1 Status				
4548	CB Fail 1 Timer				
4549	CB Fail 2 Status				
454A	CB Fail 2 Timer				
454C	CBF Non I Reset				
454D	CBF Ext Reset				

10.36 4600 - Supervision

4600	SUPERVISION	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
4601	VT SUPERVISION				
4602	VTS Status				
4603	VTS Reset Mode				
4604	VTS Time Delay				
4605	VTS I> Inhibit				
4606	VTS I2> Inhibit				
4620	CT SUPERVISION				
4621	Diff CTS				
4622	CTS Status				
4623	CTS Tdelay				
4624	CTS I1				

4600	**SUPERVISION**	**Group 1 settings**	**Group 2 settings**	**Group 3 settings**	**Group 4 settings**
Group 1 settings					
4625	CTS I2/I1>1				
4626	CTS I2/I1>2				

10.37 4A00 - Input Labels

4A00	**INPUT LABELS**	**Group 1 Settings**	**Group 2 Settings**	**Group 3 Settings**	**Group 4 Settings**
Group 1 Settings					
4A01	Opto Input 1				
4A02	Opto Input 2				
4A03	Opto Input 3				
4A04	Opto Input 4				
4A05	Opto Input 5				
4A06	Opto Input 6				
4A07	Opto Input 7				
4A08	Opto Input 8				
4A09	Opto Input 9				
4A0A	Opto Input 10				
4A0B	Opto Input 11				
4A0C	Opto Input 12				
4A0D	Opto Input 13				
4A0E	Opto Input 14				
4A0F	Opto Input 15				
4A10	Opto Input 16				
4A11	Opto Input 17				
4A12	Opto Input 18				
4A13	Opto Input 19				
4A14	Opto Input 20				
4A15	Opto Input 21				
4A16	Opto Input 22				
4A17	Opto Input 23				
4A18	Opto Input 24				
4A19	Opto Input 25				
4A1A	Opto Input 26				
4A1B	Opto Input 27				
4A1C	Opto Input 28				
4A1D	Opto Input 29				
4A1E	Opto Input 30				
4A1F	Opto Input 31				
4A20	Opto Input 32				

10.38 4B00 - Output Labels

4B00	OUTPUT LABELS	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
4B01	Relay 1				
4B02	Relay 2				
4B03	Relay 3				
4B04	Relay 4				
4B05	Relay 5				
4B06	Relay 6				
4B07	Relay 7				
4B08	Relay 8				
4B09	Relay 9				
4B0A	Relay 10				
4B0B	Relay 11				
4B0C	Relay 12				
4B0D	Relay 13				
4B0E	Relay 14				
4B0F	Relay 15				
4B10	Relay 16				
4B11	Relay 17				
4B12	Relay 18				
4B13	Relay 19				
4B14	Relay 20				
4B15	Relay 21				
4B16	Relay 22				
4B17	Relay 23				
4B18	Relay 24				
4B19	Relay 25				
4B1A	Relay 26				
4B1B	Relay 27				
4B1C	Relay 28				
4B1D	Relay 29				
4B1E	Relay 30				
4B1F	Relay 31				
4B20	Relay 32				

10.39 4C00 - RTD Labels

4C00	RTD LABELS	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
4C01	RTD 1				
4C02	RTD 2				
4C03	RTD 3				
4C04	RTD 4				

4C00	RTD LABELS	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
4C05	RTD 5				
4C06	RTD 6				
4C07	RTD 7				
4C08	RTD 8				
4C09	RTD 9				
4C0A	RTD 10				

10.40 4D00 - CLIO Protection

4D00	CLIO Protection	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
4D01	CLI1 PROTECTION				
4D02	CLI Input Status				
4D04	CLI Input Type				
4D06	CLI Input Label				
4D08	CLI Minimum				
4D0A	CLI Maximum				
4D0C	CLI Alarm				
4D0E	CLI Alarm Fn				
4D10	CLI Alarm Set				
4D12	CLI Alarm Delay				
4D14	CLI Trip				
4D16	CLI Trip Fn				
4D18	CLI Trip Set				
4D1A	CLI Trip Delay				
4D1C	CLI I< Alarm				
4D1E	CLI I< Alm Set				
4D21	CLI2 PROTECTION				
4D22	CLI Input Status				
4D24	CLI Input Type				
4D26	CLI Input Label				
4D28	CLI Minimum				
4D2A	CLI Maximum				
4D2C	CLI Alarm				
4D2E	CLI Alarm Fn				
4D30	CLI Alarm Set				
4D32	CLI Alarm Delay				
4D34	CLI Trip				
4D36	CLI Trip Fn				
4D38	CLI Trip Set				
4D3A	CLI Trip Delay				
4D3C	CLI I< Alarm				
4D3E	CLI I< Alm Set				

4D00	CLIO Protection	Group 1 settings	Group 2 settings	Group 3 settings	Group 4 settings
Group 1 settings					
4D41	CLI3 PROTECTION				
4D42	CLI Input Status				
4D44	CLI Input Type				
4D46	CLI Input Label				
4D48	CLI Minimum				
4D4A	CLI Maximum				
4D4C	CLI Alarm				
4D4E	CLI Alarm Fn				
4D50	CLI Alarm Set				
4D52	CLI Alarm Delay				
4D54	CLI Trip				
4D56	CLI Trip Fn				
4D58	CLI Trip Set				
4D5A	CLI Trip Delay				
4D5C	CLI I< Alarm				
4D5E	CLI I< Alm Set				
4D61	CLI4 PROTECTION				
4D62	CLI Input Status				
4D64	CLI Input Type				
4D66	CLI Input Label				
4D68	CLI Minimum				
4D6A	CLI Maximum				
4D6C	CLI Alarm				
4D6E	CLI Alarm Fn				
4D70	CLI Alarm Set				
4D72	CLI Alarm Delay				
4D74	CLI Trip				
4D76	CLI Trip Fn				
4D78	CLI Trip Set				
4D7A	CLI Trip Delay				
4D7C	CLI I< Alarm				
4D7E	CLI I< Alm Set				
4D9F	CLO OUTPUT 1				
4DA0	CLO Status				
4DA2	CLO Type				
4DA4	CLO Set Values				
4DA6	CLO Parameter				
4DA8	CLO Minimum				
4DAA	CLO Maximum				
4DAF	CLO OUTPUT 2				
4DB0	CLO Status				
4DB2	CLO Type				
4DB4	CLO Set Values				

4D00	**CLIO Protection**	**Group 1 settings**	**Group 2 settings**	**Group 3 settings**	**Group 4 settings**
Group 1 settings					
4DB6	CLO Parameter				
4DB8	CLO Minimum				
4DBA	CLO Maximum				
4DBF	CLO OUTPUT 3				
4DC0	CLO Status				
4DC2	CLO Type				
4DC4	CLO Set Values				
4DC6	CLO Parameter				
4DC8	CLO Minimum				
4DCA	CLO Maximum				
4DCF	CLO OUTPUT 4				
4DD0	CLO Status				
4DD2	CLO Type				
4DD4	CLO Set Values				
4DD6	CLO Parameter				
4DD8	CLO Minimum				
4DDA	CLO Maximum				

Commissioning Engineer	Customer Witness
Date:	Date:

MAINTENANCE

CHAPTER 11

Date:	12/2013	
Products covered by this chapter:	P14x (P141, P142, P143, P144 & P145), P445, P44x (P441/P442 & P444), P44y (P443 and P446), P547, P54x (P543, P544, P545 & P546), P64x (P642, P643 & P645), P841, P842, P846 and P849	
Hardware suffix:	P14x (P141, P142, P143, P144 & P145) P445 P44x (P441/P442 & P444) P44y (P443 and P446) P547 P54x (P543, P544, P545 & P546) P642 P643 P645 P841 P842 P846 P849	J J J & K K K K J K K K B J K
Software version:	P14x (P141, P142, P143, P144 & P145) P445 P44x (P441/P442 & P444) P44y (P443 and P446) P547 P54x (P543, P544, P545 & P546) P64x (P642, P643 & P645) P841 P842 P846 P849	43 35 & 36 C7.x, D4.x, D5.x & D6.x 55 57 45 & 55 04 45 & 55 04 30 A0
Connection diagrams:	P14x (P141, P142, P143, P144 & P145): 10P141/2/3/4/5xx (xx = 01 to 07) P445: 10P445xx (xx = 01 to 04) P44y: 10P44303 (SH 01 and 03) 10P44304 (SH 01 and 03) 10P44305 (SH 01 and 03) 10P44306 (SH 01 and 03) 10P44600 10P44601 (SH 1 to 2) 10P44602 (SH 1 to 2) 10P44603 (SH 1 to 2) P54x (P543, P544, P545 & P546): 10P54302xx (xx = 01 to 02) 10P54303xx (xx = 01 to 02) 10P54400 10P54402xx (xx = 01 to 02) 10P54403xx (xx = 01 to 02) 10P54502xx (xx = 01 to 02) 10P54503xx (xx = 01 to 02) 10P54600 10P54602xx (xx = 01 to 02) 10P54603xx (xx = 01 to 02)	P547: 10P54702xx (xx = 01 to 02) 10P54703xx (xx = 01 to 02) 10P54704xx (xx = 01 to 02) 10P54705xx (xx = 01 to 02) P64x (P642, P643 & P645): 10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 6) 10P644xx (xx = 01 to 9) P841: 10P84100 10P84101 (SH 1 to 2) 10P84102 (SH 1 to 2) 10P84103 (SH 1 to 2) 10P84104 (SH 1 to 2) 10P84105 (SH 1 to 2) P842: 10P842xx (xx = 01 to 02) P846: 10P846xx (xx = 01 to 07) P849: 10P849xx (xx = 01 to 06)

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1 MAINTENANCE PERIOD

It is recommended that products supplied by Schneider Electric receive periodic monitoring after installation. In view of the critical nature of protective and control equipment, and their infrequent operation, it is desirable to confirm that they are operating correctly at regular intervals.

Schneider Electric protection and control equipment is designed for a life in excess of 20 years.

MiCOM relays are self-supervizing and so require less maintenance than earlier designs. Most problems will result in an alarm so that remedial action can be taken. However, some periodic tests should be done to ensure that the equipment is functioning correctly and the external wiring is intact.

If the customer's organization has a preventative maintenance policy, the recommended product checks should be included in the regular program. Maintenance periods depend on many factors, such as:

- The operating environment
- The accessibility of the site
- The amount of available manpower
- The importance of the installation in the power system
- The consequences of failure

2 MAINTENANCE CHECKS

Although some functionality checks can be performed from a remote location by using the communications ability of the equipment, these are predominantly restricted to checking that the equipment, is measuring the applied currents and voltages accurately, and checking the circuit breaker maintenance counters. Therefore it is recommended that maintenance checks are performed locally (i.e. at the equipment itself).

Warning **Before carrying out any work on the equipment, the user should be familiar with the contents of the Safety Guide or the Technical Data chapter of this Technical Manual and also the ratings on the equipment's rating label.**

2.1 Alarms

The alarm status LED should first be checked to identify if any alarm conditions exist. If so, press the read key (📖) repeatedly to step through the alarms.

Clear the alarms to extinguish the LED.

2.2 Opto-Isolators

The opto-isolated inputs can be checked to ensure that the equipment responds to energization by repeating the commissioning test detailed in the Commissioning chapter.

2.3 Output Relays

The output relays can be checked to ensure that they operate by repeating the commissioning test detailed in the Commissioning chapter.

2.4 Measurement Accuracy

If the power system is energized, the values measured by the equipment can be compared with known system values to check that they are in the approximate range that is expected. If they are, the analog/digital conversion and calculations are being performed correctly by the relay. Suitable test methods can be found in the Commissioning chapter.

Alternatively, the values measured by the equipment can be checked against known values injected via the test block, if fitted, or injected directly into the equipment terminals. Suitable test methods can be found in the Commissioning chapter. These tests will prove the calibration accuracy is being maintained.

3 METHOD OF REPAIR

If the equipment should develop a fault whilst in service, depending on the nature of the fault, the watchdog contacts will change state and an alarm condition will be flagged. Due to the extensive use of surface-mount components, faulty Printed Circuit Boards (PCBs) should be replaced, as it is not possible to perform repairs on damaged PCBs. Therefore either the complete equipment module or just the faulty PCB (as identified by the in-built diagnostic software), can be replaced. Advice about identifying the faulty PCB can be found in the Troubleshooting chapter.

The preferred method is to replace the complete equipment module as it ensures that the internal circuitry is protected against electrostatic discharge and physical damage at all times and overcomes the possibility of incompatibility between replacement PCBs. However, it may be difficult to remove installed equipment due to limited access in the back of the cubicle and the rigidity of the scheme wiring.

Replacing PCBs can reduce transport costs but requires clean, dry conditions on site and higher skills from the person performing the repair. If the repair is not performed by an approved service center, the warranty will be invalidated.

Warning **Before carrying out any work on the equipment, the user should be familiar with the contents of the Safety Guide or the Technical Data chapter of this Technical Manual and also the ratings on the equipment's rating label.**

This should ensure that no damage is caused by incorrect handling of the electronic components.

3.1 Replacing the Complete Equipment IED/Relay

The case and rear terminal blocks have been designed to facilitate removal of the IED/relay should replacement or repair become necessary without having to disconnect the scheme wiring.

Warning **Before working at the rear of the equipment, isolate all voltage and current supplies to the equipment.**

Note *The MiCOM range has integral current transformer shorting switches which will close when the heavy duty terminal block is removed.*

1. Disconnect the equipment's earth, IRIG-B and fiber optic connections, as appropriate, from the rear of the device.

   There are two types of terminal block used on the equipment, medium and heavy duty, which are fastened to the rear panel using crosshead screws. The P64x range also includes an RTD/CLIO terminal block option. These block types are shown in the Commissioning chapter.

   Important *The use of a magnetic bladed screwdriver is recommended to minimize the risk of the screws being left in the terminal block or lost.*

2. Without exerting excessive force or damaging the scheme wiring, pull the terminal blocks away from their internal connectors.
3. Remove the screws used to fasten the equipment to the panel, rack, etc. These are the screws with the larger diameter heads that are accessible when the access covers are fitted and open.

   Warning **If the top and bottom access covers have been removed, do not remove the screws with the smaller diameter heads which are accessible. These screws secure the front panel to the equipment.**

4. Withdraw the equipment carefully from the panel, rack, etc. because it will be heavy due to the internal transformers.

To reinstall the repaired or replacement equipment, follow the above instructions in reverse, ensuring that each terminal block is relocated in the correct position and the case earth, IRIG-B and fiber optic connections are replaced. To facilitate easy identification of each terminal block, they are labeled alphabetically with 'A' on the left-hand side when viewed from the rear.

Once reinstallation is complete, the equipment should be re-commissioned using the instructions in the Commissioning chapter.

3.2 Replacing a PCB

Replacing PCBs and other internal components must be undertaken only by Service Centers approved by Schneider Electric. Failure to obtain the authorization of Schneider Electric after sales engineers prior to commencing work may invalidate the product warranty.

Warning **Before removing the front panel to replace a PCB, remove the auxiliary supply and wait at least 30 seconds for the capacitors to discharge.**
We strongly recommend that the voltage and current transformer connections and trip circuit are isolated.

Schneider Electric support teams are available world-wide. We strongly recommend that any repairs be entrusted to those trained personnel. For this reason, details on product disassembly and re-assembly are not included here.

4 RE-CALIBRATION

Re-calibration is not required when a PCB is replaced **unless it happens to be one of the boards in the input module;** the replacement of either directly affects the calibration.

Warning **Although it is possible to carry out re-calibration on site, this requires test equipment with suitable accuracy and a special calibration program to run on a PC. It is therefore recommended that the work be carried out by the manufacturer, or entrusted to an approved service center.**

5 CHANGING THE BATTERY

Each relay/IED has a battery to maintain status data and the correct time when the auxiliary supply voltage fails. The data maintained includes event, fault and disturbance records and the thermal state at the time of failure.

This battery will periodically need changing, although an alarm will be given as part of the relay's/IED's continuous self-monitoring in the event of a low battery condition.

If the battery-backed facilities are not required to be maintained during an interruption of the auxiliary supply, the steps below can be followed to remove the battery, but do not replace with a new battery.

Warning **Before carrying out any work on the equipment, the user should be familiar with the contents of the Safety Guide or the Technical Data chapter of this Technical Manual and also the ratings on the equipment's rating label.**

5.1 Instructions for Replacing the Battery

1. Open the bottom access cover on the front of the equipment.
2. Gently extract the battery from its socket. If necessary, use a small, insulated screwdriver to prize the battery free.
3. Ensure that the metal terminals in the battery socket are free from corrosion, grease and dust.
4. The replacement battery should be removed from its packaging and placed into the battery holder, taking care to ensure that the polarity markings on the battery agree with those adjacent to the socket.

Note *Only use a type ½AA Lithium battery with a nominal voltage of 3.6 V and safety approvals such as UL (Underwriters Laboratory), CSA (Canadian Standards Association) or VDE (Vereinigung Deutscher Elektrizitätswerke).*

5. Ensure that the battery is securely held in its socket and that the battery terminals are making good contact with the metal terminals of the socket.
6. Close the bottom access cover.

5.2 Post Modification Tests

To ensure that the replacement battery will maintain the time and status data if the auxiliary supply fails, check cell [0806: DATE and TIME, Battery Status] reads 'Healthy'.

If further confirmation that the replacement battery is installed correctly is required, the commissioning test is described in the Commissioning chapter, 'Date and Time', can be performed.

5.3 Battery Disposal

The battery that has been removed should be disposed of in accordance with the disposal procedure for Lithium batteries in the country in which the equipment is installed.

6 CLEANING

Warning **Before cleaning the equipment ensure that all ac and dc supplies, current transformer and voltage transformer connections are isolated to prevent any chance of an electric shock whilst cleaning.**

The equipment may be cleaned using a lint-free cloth moistened with clean water. The use of detergents, solvents or abrasive cleaners is not recommended as they may damage the relay's surface and leave a conductive residue.

TROUBLESHOOTING

CHAPTER 12

Date:	07/2013		
Hardware Suffix:	P14x (P141, P142, P143, P144 & P145)	J	
	P24x (P241, P242 & P243)	J (P241) & K (P242/P243)	
	P341	J	
	P34x (P342, P343, P344, P345 & P346)	J (P342) K (P343/P344/P345/P346) A (P391)	
	P391	A	
	P44y (P443 and P446)	K	
	P445	J	
	P54x (P543, P544, P545 & P546)	K	
	P547	K	
	P64x (P642, P643 & P645):	J (P642) & K (P643/645)	
	P841	K	
	P842	B	
	P846	J	
	P849	K	
Software Version:	P14x (P141, P142, P143, P144 & P145)	43	
	P24x (P241, P242 & P243)	57	
	P341	36 & 71 (with DLR)	
	P34x (P342, P343, P344, P345 & P346)	36	
	P391	36	
	P44y (P443 and P446)	0550	
	P445	35 & 36	
	P54x (P543, P544, P545 & P546)	45 & 55	
	P547	57	
	P64x (P642, P643 & P645):	04	
	P841	45 & 55	
	P842	04	
	P846	30	
	P849	A0	
Connection Diagrams:	P14 (P141, P142, P143, P144 & P145): 10P141/2/3/4/5xx (xx = 01 to 07) P24x (P241, P242 & P243): 10P241xx (xx = 01 to 02) 10P24201 10P24301 P341: 10P341xx (xx = 01 to 12) P34x (P342, P343, P344, P345 & P346): 10P342xx (xx = 01 to 17) 10P343xx (xx = 01 to 19) 10P344xx (xx = 01 to 12) 10P345xx (xx = 01 to 07) 10P346xx (xx = 01 to 19) 10P391xx (xx = 01 to 02) P44y: 10P44303 (SH 01 and 03) 10P44304 (SH 01 and 03) 10P44305 (SH 01 and 03) 10P44306 (SH 01 and 03) 10P44600 10P44601 (SH 1 to 2) 10P44602 (SH 1 to 2) 10P44603 (SH 1 to 2)	P445: 10P445xx (xx = 01 to 04) P54x: 10P54302 (SH 1 to 2) 10P54303 (SH 1 to 2) 10P54400 10P54404 (SH 1 to 2) 10P54405 (SH 1 to 2) 10P54502 (SH 1 to 2) 10P54503 (SH 1 to 2) 10P54600 10P54604 (SH 1 to 2) 10P54605 (SH 1 to 2) 10P54606 (SH 1 to 2) P547: 10P54702xx (xx = 01 to 02) 10P54703xx (xx = 01 to 02) 10P54704xx (xx = 01 to 02) 10P54705xx (xx = 01 to 02) P64x: 10P642xx (xx = 01 to 10) 10P643xx (xx = 01 to 06) 10P645xx (xx = 01 to 09)	P841: 10P841xx (xx = 01 to 02) 10P84100 10P841xx (xx = 01 to 03) P842: 10P842xx (xx = 01 to 02) P846: 10P846xx (xx = 01 to 07) P849: 10P849xx (xx = 01 to 06)

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- 7.3 Incorrect Analog Signals 12
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  - 7.4.1 Diagram Reconstruction after Recover from Relay 12
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Notes:

1 INTRODUCTION

Warning **Before carrying out any work on the equipment, the user should be familiar with the contents of the Safety Guide or the Technical Data chapter of this Technical Manual and also the ratings on the equipment's rating label.**

The purpose of this chapter of the service manual is to allow an error condition on the relay to be identified so that appropriate corrective action can be taken.

If the relay has developed a fault, it should be possible in most cases to identify which relay module requires attention. The *Maintenance* chapter advises on the recommended method of repair where faulty modules need replacing. It is not possible to perform an on-site repair to a faulted module.

In cases where a faulty relay/module is being returned to the manufacturer or one of their approved service centers, completed copy of the Repair/Modification Return Authorization Form located at the end of this chapter should be included.

2 INITIAL PROBLEM IDENTIFICATION

Consult Table 1 to find the description that best matches the problem experienced, then consult the section referenced to perform a more detailed analysis of the problem.

Symptom	Refer To
Relay fails to power up	Section 3
Relay powers up - but indicates error and halts during power-up sequence	Section 4
Relay Powers up but Out of Service LED is illuminated	Section 5
Error during normal operation	Section 6
Mal-operation of the relay during testing	Section 7

Table 1 - Problem identification

3 POWER UP ERRORS

If the relay does not appear to power up then the following procedure can be used to determine whether the fault is in the external wiring, auxiliary fuse, power supply module of the relay or the relay front panel.

Test	Check	Action
1	Measure auxiliary voltage on terminals 1 and 2; verify voltage level and polarity against rating the label on front. Terminal 1 is –dc, 2 is +dc	If auxiliary voltage is present and correct, then proceed to test 2. Otherwise the wiring/fuses in auxiliary supply should be checked.
2	Do LEDs/and LCD backlight illuminate on power-up, also check the N/O watchdog contact for closing.	If they illuminate or the contact closes and no error code is displayed then error is probably in the main processor board (front panel). If they do not illuminate and the contact does not close then proceed to test 3.
3	Check Field voltage output (nominally 48V DC)	If field voltage is not present then the fault is probably in the relay power supply module.

Table 2 - Failure of relay to power up

4 ERROR MESSAGE/CODE ON POWER-UP

During the power-up sequence of the relay self-testing is performed as indicated by the messages displayed on the LCD. If an error is detected by the relay during these self-tests, an error message will be displayed and the power-up sequence will be halted. If the error occurs when the relay application software is executing, a maintenance record will be created and the relay will reboot.

Test	Check	Action
1	Is an error message or code permanently displayed during power up?	If relay locks up and displays an error code permanently then proceed to test 2. If the relay prompts for input by the user proceed to test 4. If the relay re-boots automatically then proceed to test 5.
2	Record displayed error, then remove and re-apply relay auxiliary supply.	Record whether the same error code is displayed when the relay is rebooted. If no error code is displayed then contact the local service center stating the error code and relay information. If the same code is displayed proceed to test 3.
3	Error code Identification Following text messages (in English) will be displayed if a fundamental problem is detected preventing the system from booting: Bus Fail address lines SRAM Fail data lines FLASH Fail format error FLASH Fail checksum Code Verify Fail These hex error codes relate to errors detected in specific relay modules:	These messages indicate that a problem has been detected on the main processor board of the relay (located in the front panel).
	0c140005/0c0d0000	Input Module (inc. Opto-isolated inputs)
	0c140006/0c0e0000	Output Relay Cards
	Last 4 digits provide details on the actual error.	Other error codes relate to problems within the main processor board hardware or software. It will be necessary to contact Schneider Electric with details of the problem for a full analysis.
4	Relay displays message for corrupt settings and prompts for restoration of defaults to the affected settings.	The power up tests have detected corrupted relay settings, it is possible to restore defaults to allow the power-up to be completed. It will then be necessary to re-apply the application-specific settings.
5	Relay resets on completion of power up - record error code displayed	Error 0x0E080000, Programmable Scheme Logic (PSL) error due to excessive execution time. Restore default settings by performing a power up with ◁ and ▷ keys depressed, confirm restoration of defaults at prompt using (↵) key. If relay powers up successfully, check PSL for feedback paths. Other error codes will relate to software errors on the main processor board, contact Schneider Electric.

Table 3 - Power-up self-test error

5 OUT OF SERVICE LED ILLUMINATED ON POWER UP

Test	Check	Action	
1	Using the relay menu confirm whether the Commission Test/Test Mode setting is Enabled. Otherwise proceed to test 2.	If the setting is Enabled then disable the test mode and, verify that the Out of Service LED is extinguished.	
2	Select and view the last maintenance record from the menu (in the View Records).	Check for H/W Verify Fail this indicates a discrepancy between the relay model number and the hardware; examine the "**Maint. Data**", this indicates the causes of the failure using bit fields:	
		Bit	**Meaning**
		0	The application type field in the model number does not match the software ID
		1	The application field in the model number does not match the software ID
		2	The variant 1 field in the model number does not match the software ID
		3	The variant 2 field in the model number does not match the software ID
		4	The protocol field in the model number does not match the software ID
		5	The language field in the model number does not match the software ID
		6	The VT type field in the model number is incorrect (110V VTs fitted)
		7	The VT type field in the model number is incorrect (440V VTs fitted)
		8	The VT type field in the model number is incorrect (no VTs fitted)

Table 4 - Out of service LED illuminated

6 ERROR CODE DURING OPERATION

The relay performs continuous self-checking, if an error is detected then an error message will be displayed, a maintenance record will be logged and the relay will reset (after a 1.6 second delay). A permanent problem (for example due to a hardware fault) will generally be detected on the power up sequence, following which the relay will display an error code and halt. If the problem was transient in nature then the relay should reboot correctly and continue in operation. The nature of the detected fault can be determined by examination of the maintenance record logged.

There are also two cases where a maintenance record will be logged due to a detected error where the relay will not reset. These are detection of a failure of either the field voltage or the lithium battery, in these cases the failure is indicated by an alarm message, however the relay will continue to operate.

If the field voltage is detected to have failed (the voltage level has dropped below threshold), then a scheme logic signal is also set. This allows the scheme logic to be adapted in the case of this failure (for example if a blocking scheme is being used).

In the case of a battery failure it is possible to prevent the relay from issuing an alarm using the setting under the Date and Time section of the menu. This setting ‘**Battery Alarm**’ can be set to '**Disabled**' to allow the relay to be used without a battery, without an alarm message being displayed.

In the case of an RTD board failure, an alarm "RTD board fail" message is displayed, the RTD protection is disabled, but the operation of the rest of the relay functionality is unaffected.

7 MAL-OPERATION OF THE RELAY DURING TESTING

7.1 Failure of Output Contacts

An apparent failure of the relay output contacts may be caused by the relay configuration; the following tests should be performed to identify the real cause of the failure.

Note *The relay self-tests verify that the coil of the contact has been energized, an error will be displayed if there is a fault in the output relay board.*

Test	Check	Action
1	Is the Out of Service LED illuminated?	Illumination of this LED may indicate that the relay is in test mode or that the protection has been disabled due to a hardware verify error (see Table 4).
2	Examine the Contact status in the Commissioning section of the menu.	If the relevant bits of the contact status are operated, proceed to test 4, if not proceed to test 3.
3	Verify by examination of the fault record or by using the test port whether the protection element is operating correctly.	If the protection element does not operate verify whether the test is being correctly applied. If the protection element does operate, it will be necessary to check the PSL to ensure that the mapping of the protection element to the contacts is correct.
4	Using the Commissioning/Test mode function apply a test pattern to the relevant relay output contacts and verify whether they operate (note the correct external connection diagram should be consulted). A continuity tester can be used at the rear of the relay for this purpose.	If the output relay does operate, the problem must be in the external wiring to the relay. If the output relay does not operate this could indicate a failure of the output relay contacts (note that the self-tests verify that the relay coil is being energized). Ensure that the closed resistance is not too high for the continuity tester to detect.

Table 5 - Failure of output contacts

7.2 Failure of Opto-Isolated Inputs

The opto-isolated inputs are mapped onto the relay internal signals using the PSL. If an input does not appear to be recognized by the relay scheme logic the Commission Tests/Opto Status menu option can be used to verify whether the problem is in the opto-isolated input itself or the mapping of its signal to the scheme logic functions. If the opto-isolated input does appear to be read correctly then it will be necessary to examine its mapping within the PSL.

Ensure the voltage rating for the opto inputs has been configured correctly with applied voltage. If the opto-isolated input state is not being correctly read by the relay the applied signal should be tested. Verify the connections to the opto-isolated input using the correct wiring diagram and the correct nominal voltage settings in any standard or custom menu settings. Next, using a voltmeter verify that 80% opto setting voltage is present on the terminals of the opto-isolated input in the energized state. If the signal is being correctly applied to the relay then the failure may be on the input card itself. Depending on which opto-isolated input has failed this may require replacement of either the complete analog input module (the board within this module cannot be individually replaced without re-calibration of the relay) or a separate opto board.

7.3 Incorrect Analog Signals

The measurements may be configured in primary or secondary to assist. If it is suspected that the analog quantities being measured by the relay are not correct then the measurement function of the relay can be used to verify the nature of the problem. The measured values displayed by the relay should be compared with the actual magnitudes at the relay terminals. Verify that the correct terminals are being used (in particular the dual rated CT inputs) and that the CT and VT ratios set on the relay are correct. The correct 120 degree displacement of the phase measurements should be used to confirm that the inputs have been correctly connected.

7.4 PSL Editor Troubleshooting

A failure to open a connection could be because of one or more of the following:

- The relay address is not valid (note: this address is always 1 for the front port).
- Password is not valid
- Communication Set-up - COM port, Baud rate, or Framing - is not correct
- Transaction values are not suitable for the relay and/or the type of connection
- Modem configuration is not valid. Changes may be necessary when using a modem
- The connection cable is not wired correctly or broken. See MiCOM S1 connection configurations
- The option switches on any KITZ101/102 that is in use may be incorrectly set

7.4.1 Diagram Reconstruction after Recover from Relay

Although the extraction of a scheme from a relay is supported, the facility is provided as a way of recovering a scheme in the event that the original file is unobtainable.

The recovered scheme will be logically correct, but much of the original graphical information is lost. Many signals will be drawn in a vertical line down the left side of the canvas. Links are drawn orthogonally using the shortest path from A to B.

Any annotation added to the original diagram (titles, notes, etc.) are lost.

Sometimes a gate type may not be what was expected, e.g. a 1-input AND gate in the original scheme will appear as an OR gate when uploaded. Programmable gates with an inputs-to-trigger value of 1 will also appear as OR gates.

7.4.2 PSL Version Check

The PSL is saved with a version reference, time stamp and CRC check. This gives a visual check whether the default PSL is in place or whether a new application has been downloaded.

8 REPAIR AND MODIFICATION PROCEDURE

Please follow these steps to return an Automation product to us:

1. Get the Repair and Modification Authorization Form (RMA).

   A copy of the RMA form is shown at the end of this section.

2. Fill in the RMA form.

   Fill in only the white part of the form.

   Please ensure that all fields marked **(M)** are completed such as:

   Equipment model

   Model No. and Serial No.

   Description of failure or modification required (please be specific)

   Value for customs (in case the product requires export)

   Delivery and invoice addresses

   Contact details

3. Receive from local service contact, the information required to ship the product.

   Your local service contact will provide you with all the information:

   Pricing details

   RMA No

   Repair center address

   If required, an acceptance of the quote must be delivered before going to next stage.

4. Send the product to the repair center.

   Address the shipment to the repair center specified by your local contact.

   Ensure all items are protected by appropriate packaging: anti-static bag and foam protection.

   Ensure a copy of the import invoice is attached with the unit being returned.

   Ensure a copy of the RMA form is attached with the unit being returned.

   E-mail or fax a copy of the import invoice and airway bill document to your local contact.

Notes:

Schneider Electric

REPAIR/MODIFICATION RETURN AUTHORIZATION FORM

FIELDS IN GREY TO BE FILLED IN BY SCHNEIDER ELECTRIC PERSONNEL ONLY

Reference **RMA:** _____		Date:
Repair Center Address (for shipping)	**Service Type** ☐ Retrofit ☐ Warranty ☐ Paid service ☐ Under repair contract ☐ Wrong supply	LSC PO No.:
Schneider Electric - Local Contact Details Name: Telephone No.: Fax No.: E-mail:		

IDENTIFICATION OF UNIT

Fields marked (M) are mandatory, delays in return will occur if not completed.

Model No./Part No.: **(M)**	Site Name/Project:
Manufacturer Reference: **(M)**	Commissioning Date:
Serial No.: **(M)**	Under Warranty: ☐ Yes ☐ No
Software Version:	Additional Information:
Quantity:	Customer P.O (if paid):

FAULT INFORMATION

Type of Failure	**Found Defective**
Hardware fail ☐	During FAT/inspection ☐
Mechanical fail/visible defect ☐	On receipt ☐
Software fail ☐	During installation/commissioning ☐
Other:	During operation ☐
	Other:
Fault Reproducibility	
Fault persists after removing, checking on test bench ☐	
Fault persists after re-energization ☐	
Intermittent fault ☐	

Description of Failure Observed or Modification Required - *Please be specific* **(M)**

FOR REPAIRS ONLY

Would you like us to install an updated firmware version after repair?	☐	Yes	☐	No

CUSTOMS & INVOICING INFORMATION

Required to allow return of repaired items

Value for Customs (M)	
Customer Invoice Address ((M) if paid)	**Customer Return Delivery Address (full street address) (M)** Part shipment accepted ☐ Yes ☐ No **OR** Full shipment required ☐ Yes ☐ No
Contact Name: Telephone No.: Fax No.: E-mail:	Contact Name: Telephone No.: Fax No.: E-mail:

REPAIR TERMS

1. **Please ensure that a copy of the import invoice is attached with the returned unit, together with the airway bill document.** Please fax/e-mail a copy of the appropriate documentation **(M)**.
2. Please ensure the Purchase Order is released, for paid service, to allow the unit to be shipped.
3. Submission of equipment to Schneider Electric is deemed as authorization to repair and acceptance of quote.
4. Please ensure all items returned are marked as Returned for ‘Repair/Modification’ and **protected by appropriate packaging** (anti-static bag for each board and foam protection).

SCADA COMMUNICATIONS

CHAPTER NO 13

Date:	12/2013
Hardware Suffix:	J (P642) K (P643/P645)
Software Version:	04
Connection Diagrams:	10P642xx (xx = 1 to 10) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9)

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1 INTRODUCTION

This chapter describes the remote interfaces of the MiCOM relay in enough detail to allow integration in a substation communication network. As has been outlined in earlier chapters, the relay supports a choice of one of four protocols through the rear communication interface, selected using the model number when ordering. This is in addition to the front serial interface and second rear communications port, which supports the Courier protocol only.

The rear EIA(RS)-485 interface is isolated and is suitable for permanent connection whichever protocol is selected. The advantage of this type of connection is that up to 32 relays can be daisy-chained together using a simple twisted-pair electrical connection.

For each of the protocol options, the supported functions and commands are listed with the database definition. The operation of standard procedures such as extraction of event, fault and disturbance records, or setting changes is also described.

The descriptions in this chapter do not aim to fully describe the protocol in detail. Refer to the relevant documentation protocol for this information. This chapter describes the specific implementation of the protocol in the relay.

2 REAR PORT CONNECTION - EIA(RS)-485 PROTOCOLS

2.1 Rear Communication Port EIA(RS)-485 Interface

The rear EIA(RS)-485 communication port is provided by a 3-terminal screw connector on the back of the relay. See the Installation chapter for details of the connection terminals. The rear port provides K-Bus/EIA(RS)-485 serial data communication and is intended for use with a permanently-wired connection to a remote control center. Of the three connections, two are for the signal connection, and the other is for the earth shield of the cable. When the K-Bus option is selected for the rear port, the two signal connections are not polarity conscious, however for MODBUS, IEC60870-5-103 and DNP3.0 care must be taken to observe the correct polarity.

The protocol provided by the relay is indicated in the relay menu in the **Communications** column. Using the keypad and LCD, first check that the **Comms. settings** cell in the **Configuration** column is set to **Visible**, then move to the **Communications** column. The first cell down the column shows the communication protocol that is being used by the rear port.

2.2 EIA(RS)-485 Bus

The EIA(RS)-485 two-wire connection provides a half-duplex fully isolated serial connection to the product. The connection is polarized and while the product's connection diagrams show the polarization of the connection terminals, there is no agreed definition of which terminal is which. If the master is unable to communicate with the product and the communication parameters match, make sure the two-wire connection is not reversed.

EIA(RS)-485 provides the capability to connect multiple devices to the same two-wire bus. MODBUS is a master-slave protocol, so one device is the master, and the remaining devices are slaves. It is not possible to connect two masters to the same bus, unless they negotiate bus access.

2.2.1 Bus Termination

The EIA(RS)-485 bus must have 120 Ω (Ohm) ½ Watt terminating resistors fitted at either end across the signal wires, see Figure 1. Some devices may be able to provide the bus terminating resistors by different connection or configuration arrangements, in which case separate external components are not needed. However, this product does not provide such a facility, so if it is located at the bus terminus, an external termination resistor is needed.

2.2.2 Bus Connections & Topologies

The EIA(RS)-485 standard requires each device to be directly connected to the physical cable that is the communications bus. Stubs and tees are expressly forbidden, as are star topologies. Loop bus topologies are not part of the EIA(RS)-485 standard and are forbidden by it.

Two-core screened cable is recommended. The specification of the cable depends on the application, although a multi-strand 0.5 mm^2 per core is normally adequate. Total cable length must not exceed 1000 m. The screen must be continuous and connected at one end, normally at the master connection point. It is important to avoid circulating currents, especially when the cable runs between buildings, for both safety and noise reasons.

This product does not provide a signal ground connection. If the bus cable has a signal ground connection, it must be ignored. However, the signal ground must have continuity for the benefit of other devices connected to the bus. For both safety and noise reasons, the signal ground must never be connected to the cable's screen or to the product's chassis.

2.2.3 Biasing

It may also be necessary to bias the signal wires to prevent jabber. Jabber occurs when the signal level has an indeterminate state because the bus is not being actively driven. This can occur when all the slaves are in receive mode and the master is slow to switch from receive mode to transmit mode. This may be because the master purposefully waits in receive mode, or even in a high impedance state, until it has something to transmit. Jabber causes the receiving device(s) to miss the first bits of the first character in the packet, which results in the slave rejecting the message and consequentially not responding. Symptoms of this are poor response times (due to retries), increasing message error counters, erratic communications, and even a complete failure to communicate.

Biasing requires that the signal lines are weakly pulled to a defined voltage level of about 1 V. There should only be one bias point on the bus, which is best situated at the master connection point. The DC source used for the bias must be clean, otherwise noise is injected. Some devices may (optionally) be able to provide the bus bias, in which case external components are not required.

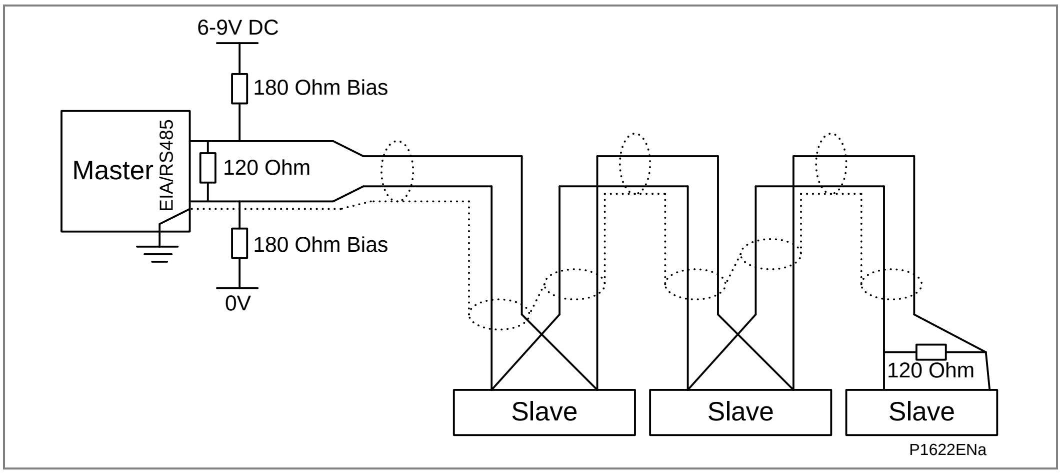


Figure 1 - EIA(RS)-485 bus connection arrangements

It is possible to use the product's field voltage output (48 V DC) to bias the bus using values of 2.2 k Ω (½W) as bias resistors instead of the 180 Ω resistors shown in Figure 1. Note the following warnings apply:

Warning	**It is extremely important that the 120 Ω termination resistors are fitted. Otherwise the bias voltage may be excessive and may damage the devices connected to the bus.**
Warning	**As the field voltage is much higher than that required, Schneider Electric cannot assume responsibility for any damage that may occur to a device connected to the network as a result of incorrect application of this voltage.**
Warning	**Ensure the field voltage is not used for other purposes, such as powering logic inputs, because noise may be passed to the communication network.**

2.2.4 Courier Communication

Courier is the communication language developed to allow remote interrogation of its range of protection relays. Courier uses a master and slave. EIA(RS)-232 on the front panel allows only one slave but EIA(RS)-485 on the back panel allows up to 32 daisy-chained slaves. Each slave unit has a database of information and responds with information from its database when requested by the master unit.

The relay is a slave unit that is designed to be used with a Courier master unit such as MiCOM S1 Studio, MiCOM S10, PAS&T or a SCADA system. MiCOM S1 Studio is compatible with Windows^{TM} 2000, XP or Vista and is specifically designed for setting changes with the relay.

To use the rear port to communicate with a PC-based master station using Courier, a KITZ K-Bus to EIA(RS)-232 protocol converter is needed. This unit is available from Schneider Electric. A typical connection arrangement is shown in Figure 2. For more detailed information on other possible connection arrangements, refer to the manual for the Courier master station software and the manual for the KITZ protocol converter. Each spur of the K-Bus twisted pair wiring can be up to 1000 m in length and have up to 32 relays connected to it.

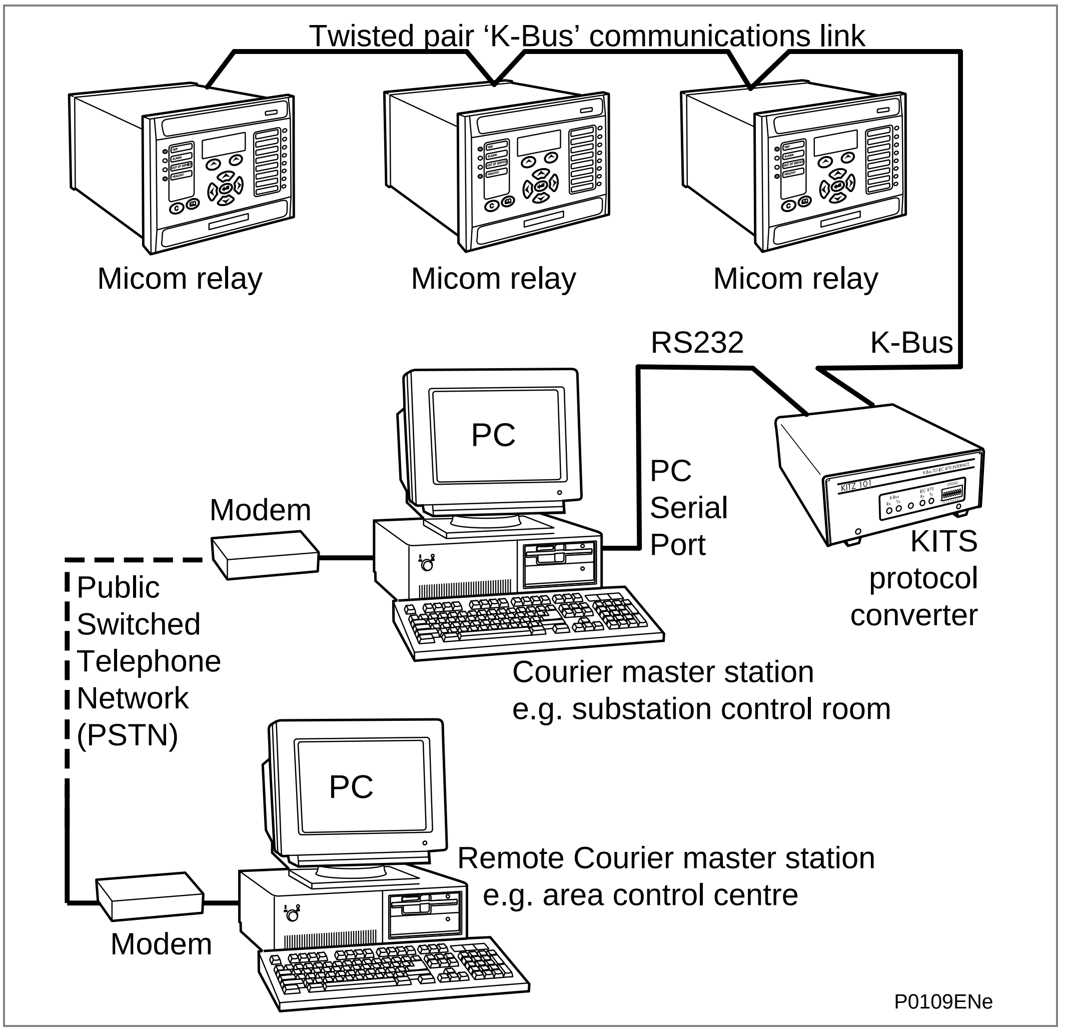

Twisted pair 'K-Bus' communications link
Micom relay
Micom relay
Micom relay
RS232
K-Bus
PC
PC
Serial
Port
Modem
KITS
protocol
converter
Public
Switched
Telephone
Network
(PSTN)
Courier master station
e.g. substation control room
PC
Remote Courier master station
e.g. area control centre
Modem
P0109ENe

Figure 2 - Remote communication connection arrangements

Once the physical connection is made to the relay, configure the relay's communication settings using the keypad and LCD user interface.

1. In the relay menu, select the **Configuration** column, then check that the **Comms. settings** cell is set to **Visible**.
2. Select the **Communications** column. Only two settings apply to the rear port using Courier, the relay’s address and the inactivity timer. Synchronous communication uses a fixed baud rate of 64 kbits/s.
3. Move down the **Communications** column from the column heading to the first cell down. This shows the communication protocol.

   ```
   RP1 Protocol
   Courier
   ```

4. The next cell down the column controls the address of the relay. As up to 32 relays can be connected to one K-Bus spur (see Figure 2), each relay must have a unique address so messages from the master control station are accepted by one relay only. Courier uses an integer (from 0 to 254) for the relay address that is set with this cell. Important: no two relays should have the same Courier address. The master station uses the Courier address to communicate with the relay.

   ```
   RP1 Address
   1
   ```

5. The next cell down controls the inactivity timer.

   ```
   RP1 Inactiv timer
   10.00 mins.
   ```

   The inactivity timer controls how long the relay waits without receiving any messages on the rear port before it reverts to its default state, including revoking any password access that was enabled. For the rear port this can be set between 1 and 30 minutes. The next cell down controls the physical media used for the communication.

   ```
   RP1 Physical link
   Copper
   ```

   The default setting is to select the copper electrical EIA(RS)-485 connection. If the optional fiber optic connectors are fitted to the relay, this setting can be changed to **Fiber optic**. This cell is also invisible if a second rear comms. port is fitted because it is mutually exclusive to the fiber optic connectors.

6. As an alternative to running Courier over K-Bus, Courier over EIA(RS)-485 can be selected. The next cell down indicates the status of the hardware.

   ```
   RP1 Card status
   EIA(RS)-232 OK
   ```

7. The next cell allows you to configure the port for EIA(RS)-485 or K-Bus.

   ```
   RP1 Port config.
   EIA(RS)-232
   ```

8. If using EIA(RS)-485, the next cell selects the communication mode. The choice is either IEC60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity.

   ```
   RP1 Comms. Mode
   IEC60870 FT1.2
   ```

9. If using EIA(RS)-485, the next cell down controls the baud rate. For K-Bus the baud rate is fixed at 64 kbits/second between the relay and the KITZ interface at the end of the relay spur. Courier communications is asynchronous. Three baud rates are supported by the relay, 9600 bits/s, 19200 bits/s and 38400 bits/s.

```
RP1 Baud rate
19200
```

If you modify protection and disturbance recorder settings using an on-line editor such as PAS&T, you must confirm them. To do this, from the **Configuration** column select the **Save changes** cell. Off-line editors such as MiCOM S1 Studio do not need this action for the setting changes to take effect.

2.2.5 MODBUS Communication

MODBUS is a master/slave communication protocol that can be used for network control. In a similar way to Courier, the master device initiates all actions and the slave devices (the relays) respond to the master by supplying the requested data or by taking the requested action. MODBUS communication uses a twisted pair connection to the rear port and can be used over a distance of 1000 m with up to 32 slave devices.

To use the rear port with MODBUS communication, configure the relay’s communication settings using the keypad and LCD user interface.

1. In the relay menu, select the **Configuration** column, then check that the **Comms. settings** cell is set to **Visible**.
2. Select the **Communications** column. Four settings apply to the rear port using MODBUS that are described below. Move down the **Communications** column from the column heading to the first cell down. This shows the communication protocol.

```
RP1 Protocol
MODBUS
```

3. The next cell down controls the MODBUS address of the relay.

```
RP1 MODBUS address
23
```

Up to 32 relays can be connected to one MODBUS spur, therefore it is necessary for each relay to have a unique address so that messages from the master control station are accepted by one relay only. MODBUS uses an integer between 1 and 247 for the relay address. It is important that no two relays have the same MODBUS address. The MODBUS address is then used by the master station to communicate with the relay.

4. The next cell down controls the inactivity timer.

```
RP1 Inactiv timer
10.00 mins.
```

The inactivity timer controls how long the relay waits without receiving any messages on the rear port before it reverts to its default state, including revoking any password access that was enabled. For the rear port this can be set between 1 and 30 minutes.

5. The next cell down the column controls the baud rate to be used.

```
RP1 Baud rate
9600 bits/s
```

MODBUS communication is asynchronous. Three baud rates are supported by the relay, 9600 bits/s, 19200 bits/s and 38400 bits/s. It is important that whatever baud rate is selected on the relay is the same as that set on the MODBUS master station.

6. The next cell down controls the parity format used in the data frames.

```
RP1 Parity
None
```

The parity can be set to be one of **None**, **Odd** or **Even**. It is important that whatever parity format is selected on the relay is the same as that set on the MODBUS master station.

7. The next cell down controls the physical media used for the communication.

```
RP1 Physical link
Copper
```

The default setting is to select the copper electrical EIA(RS)-485 connection. If the optional fiber optic connectors are fitted to the relay, this setting can be changed to **Fiber optic**. This cell is also invisible if a second rear comms. port is fitted because it is mutually exclusive to the fiber optic connectors.

8. The next cell down controls the format of the Date/Time (software 30 or later).

```
MODBUS
IEC time standard
```

The format can be selected as either **Standard** (as for IEC60870-5-4 ‘Binary Time 2a’) which is the default, or to **Reverse** for compatibility with MICOM Px20 and Px30 product ranges. For more information see *section 4.16*.

2.2.6 IEC 60870-5 CS 103 Communication

The IEC specification IEC 60870-5-103: Telecontrol Equipment and Systems, Part 5: Transmission Protocols Section 103 defines the use of standards IEC 60870-5-1 to IEC 60870-5-5 to perform communication with protection equipment. The standard configuration for the IEC 60870-5-103 protocol is to use a twisted pair connection over distances up to 1000 m. As an option for IEC 60870-5-103, the rear port can be specified to use a fiber optic connection for direct connection to a master station. The relay operates as a slave in the system, responding to commands from a master station. The method of communication uses standardized messages which are based on the VDEW communication protocol.

To use the rear port with IEC 60870-5-103 communication, configure the relay’s communication settings using the keypad and LCD user interface.

9. In the relay menu, select the **Configuration** column, then check that the **Comms. settings** cell is set to **Visible**.

10. Select the **Communications** column. Four settings apply to the rear port using IEC 60870-5-103 that are described below.

    Move down the **Communications** column from the column heading to the first cell down. This shows the communication protocol.

```
RP1 Protocol
IEC 60870-5-103
```

11. The next cell down controls the IEC 60870-5-103 address of the relay.

```
RP1 address
162
```

Up to 32 relays can be connected to one IEC 60870-5-103 spur, therefore it is necessary for each relay to have a unique address so that messages from the master control station are accepted by one relay only. IEC 60870-5-103 uses an integer number between 0 and 254 for the relay address. It is important that no two relays have the same IEC 60870-5-103 address. The IEC 60870-5-103 address is then used by the master station to communicate with the relay.

12. The next cell down the column controls the baud rate to be used.

```
RP1 Baud rate
9600 bits/s
```

IEC 60870-5-103 communication is asynchronous. Two baud rates are supported by the relay, ‘9600 bits/s’ and ‘19200 bits/s’. It is important that whatever baud rate is selected on the relay is the same as that set on the IEC 60870-5-103 master station.

13. The next cell down controls the period between IEC 60870-5-103 measurements.

```
RP1 Meas. Period
30.00 s
```

The IEC 60870-5-103 protocol allows the relay to supply measurements at regular intervals. The interval between measurements is controlled by this cell, and can be set between 1 and 60 seconds.

14. The following cell is not currently used but is available for future expansion.

```
RP1 Inactiv timer
```

15. The next cell down the column controls the physical media used for communication.

```
RP1 Physical link
Copper
```

The default setting is to select the copper electrical EIA(RS)-485 connection. If the optional fiber optic connectors are fitted to the relay, this setting can be changed to **Fiber optic**. This cell is also invisible if a second rear comms. port is fitted because it is mutually exclusive to the fiber optic connectors.

16. The next cell down can be used for monitor or command blocking.

```
RP1 CS103 Blcking
```

There are three settings associated with this cell; these are:

- Disabled

  No blocking selected.

- Monitor Blocking

  When the monitor blocking DDB Signal is active high, either by energizing an opto input or control input, reading of the status information and disturbance records is not permitted. When in this mode the relay returns a “Termination of general interrogation” message to the master station.

- Command Blocking

  When the command blocking DDB signal is active high, either by energizing an opto input or control input, all remote commands are ignored, such as CB Trip/Close or change setting group. When in this mode the relay returns a **negative acknowledgement of command** message to the master station.

2.2.7 DNP3.0 Communication

The DNP3.0 protocol is defined and administered by the DNP User Group. Information about the user group, DNP3.0 in general and protocol specifications can be found on their website: www.dnp.org

The relay operates as a DNP3.0 slave and supports subset level 2 of the protocol plus some of the features from level 3. DNP3.0 communication is achieved using a twisted pair connection to the rear port and can be used over a distance of 1000 m with up to 32 slave devices.

1. To use the rear port with DNP3.0 communication, configure the relay's communication settings using the keypad and LCD user interface.
2. In the relay menu, select the **Configuration** column, then check that the **Comms. settings** cell is set to **Visible**.
3. Four settings apply to the rear port using IEC 60870-5-103 that are described below.
4. Move down the **Communications** column from the column heading to the first cell down. This shows the communication protocol.

```
RP1 Protocol
DNP3.0
```

5. The next cell controls the DNP3.0 address of the relay.

```
RP1 Address
232
```

Up to 32 relays can be connected to one DNP3.0 spur, therefore it is necessary for each relay to have a unique address so that messages from the master control station are accepted by only one relay. DNP3.0 uses a decimal number between 1 and 65519 for the relay address. It is important that no two relays have the same DNP3.0 address. The DNP3.0 address is then used by the master station to communicate with the relay.

6. The next cell down the column controls the baud rate to be used.

```
RP1 Baud rate
9600 bits/s
```

DNP3.0 communication is asynchronous. Six baud rates are supported by the relay 1200bits/s, 2400bits/s, 4800bits/s, 9600bits/s, 19200bits/s and 38400bits/s. It is important that whatever baud rate is selected on the relay is the same as that set on the DNP3.0 master station.

7. The next cell down the column controls the parity format used in the data frames.

```
RP1 Parity
None
```

The parity can be set to be one of **None**, **Odd** or **Even.** It is important that whatever parity format is selected on the relay is the same as that set on the DNP3.0 master station.

8. The next cell down the column controls the physical media used for the communication.

```
RP1 Physical link
Copper
```

The default setting is to select the copper electrical EIA(RS)-485 connection. If the optional fiber optic connectors are fitted to the relay, this setting can be changed to

Fiber optic. This cell is also invisible if a second rear comms. port is fitted because it is mutually exclusive to the fiber optic connectors.

9. The next cell down the column sets the time synchronization request from the master by the relay.

```
RP1 Time sync.
Enabled
```

The time sync. can be set to either enabled or disabled. If enabled it allows the DNP3.0 master to synchronize the time.

2.3 Second Rear Communication Port

For relays with Courier, MODBUS, IEC60870-5-103 or DNP3.0 protocol on the first rear communications port there is the hardware option of a second rear communications port, which runs the Courier language. This can be used over one of three physical links: twisted pair K-Bus (non-polarity sensitive), twisted pair EIA(RS)-485 (connection polarity sensitive) or EIA(RS)-232. The settings for this port are immediately below those for the first port. See the *Installation* chapter *P64x/EN IT*.

1. Move down the settings until the following sub heading is displayed.

```
Rear port2
(RP2)
```

2. The next cell down indicates the language, which is fixed at Courier for RP2.

```
RP2 Protocol
Courier
```

3. The next cell down indicates the status of the hardware.

```
RP2 Card status
EIA(RS)-232 OK
```

4. The next cell allows port to be configured for EIA(RS)-232, EIA(RS)-485 or K-Bus.

```
RP2 Port config.
EIA(RS)-232
```

5. For EIA(RS)-232 and EIA(RS)-485, the next cell selects the communication mode.

   The choice is either IEC60870 FT1.2 for normal operation with 11-bit modems, or 10-bit no parity.

```
RP2 Comms. Mode
IEC60870 FT1.2
```

6. The next cell down controls the comms. port address.

```
RP2 Address
255
```

Since up to 32 relays can be connected to one K-Bus spur, as indicated in Figure 2 each relay must have a unique address so that messages from the master control station are accepted by one relay only. Courier uses an integer between 0 and 254 for the relay address that is set with this cell. It is important that no two relays have the same Courier address. The Courier address is then used by the master station to communicate with the relay.

7. The next cell down controls the inactivity timer.

```
RP2 Inactivity timer
15 mins.
```

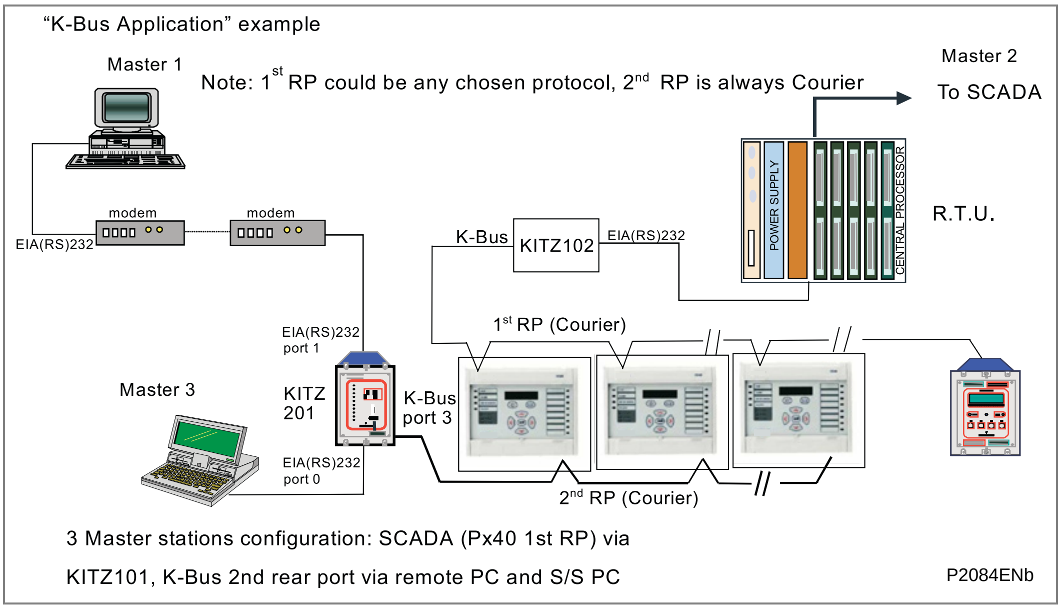
The inactivity timer controls how long the relay waits without receiving any messages on the rear port before it reverts to its default state, including revoking any password access that was enabled. For the rear port this can be set between 1 and 30 minutes.

8. For EIA(RS)-232 and EIA(RS)-485, the next cell down controls the baud rate.

   For K-Bus the baud rate is fixed at 64 kbit/second between the relay and the KITZ interface at the end of the relay spur.

```
RP2 Baud rate
19200
```

Courier communications is asynchronous. Three baud rates are supported by the relay, 9600 bits/s, 19200 bits/s and 38400 bits/s.


"K-Bus Application" example
Master 1
Master 2
To SCADA
R.T.U.
POWER SUPPLY
CENTRAL PROCESSOR
modem
modem
EIA(RS)232
K-Bus
KITZ102
EIA(RS)232
1st RP (Courier)
EIA(RS)232 port 1
Master 3
KITZ 201
K-Bus port 3
EIA(RS)232 port 0
2nd RP (Courier)
P2084ENb

Note: 1st RP could be any chosen protocol, 2nd RP is always Courier

3 Master stations configuration: SCADA (Px40 1st RP) via KITZ101, K-Bus 2nd rear port via remote PC and S/S PC

Figure 3 - Second rear port K-Bus application

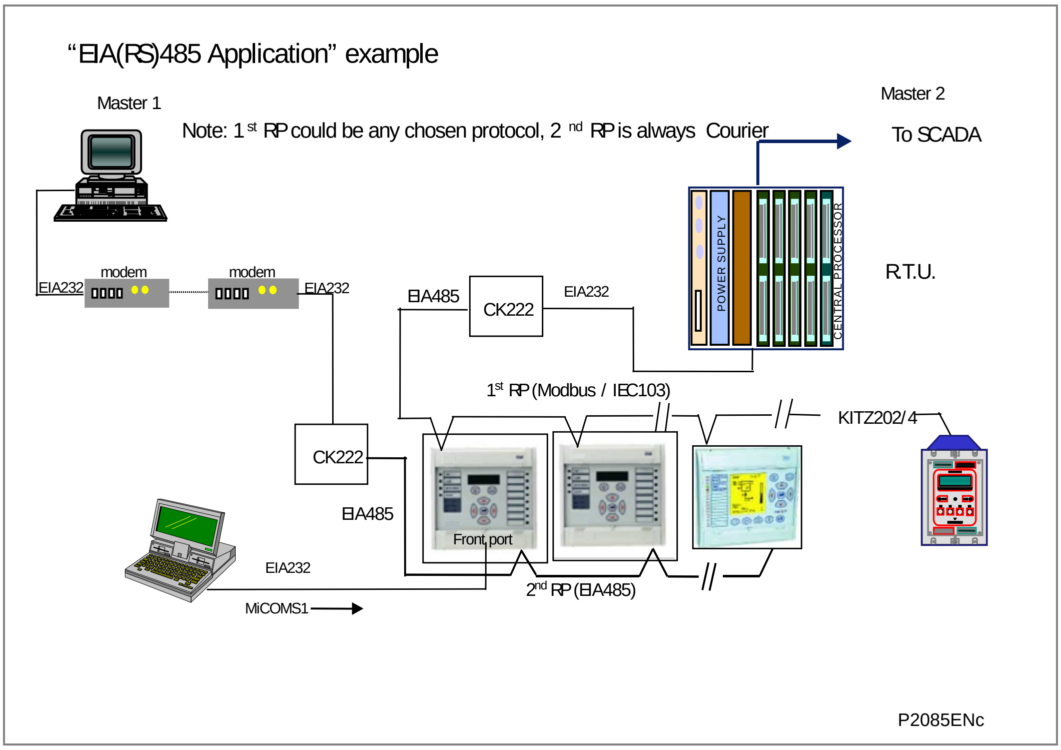
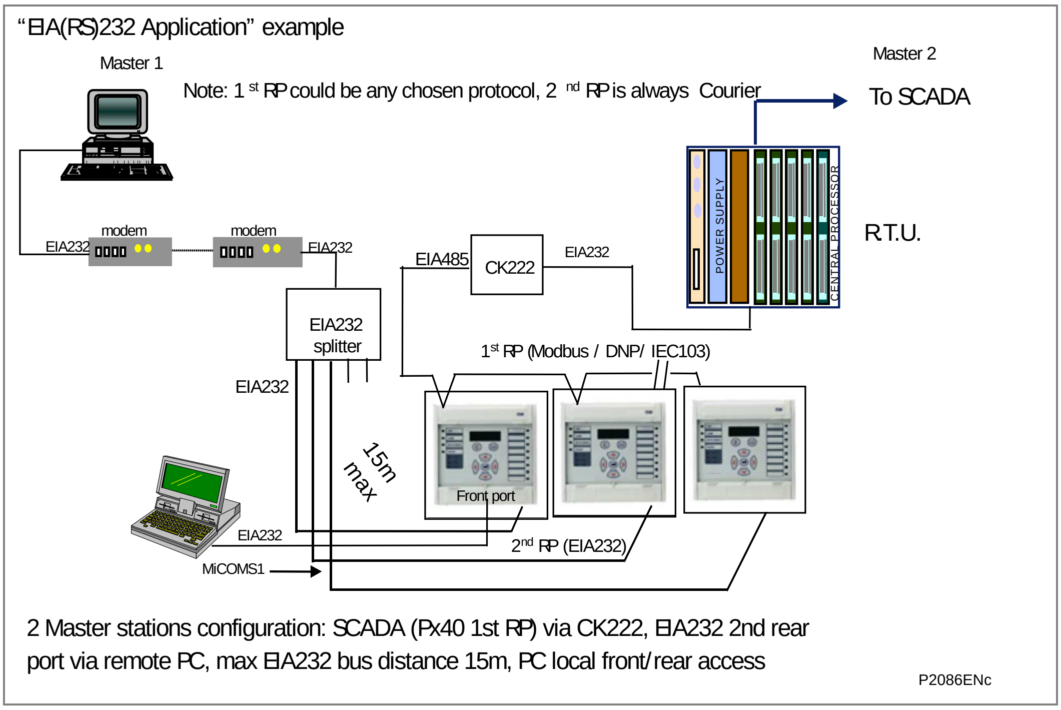

"EIA(RS)485 Application" example
Master 1
Master 2
Note: 1 st RP could be any chosen protocol, 2 nd RP is always Courier
To SCADA
POWER SUPPLY
CENTRAL PROCESSOR
R.T.U.
modem
modem
EIA232
EIA232
EIA485
CK222
EIA232
1st RP (Modbus / IEC103)
KITZ202/4
CK222
EIA485
Front port
EIA232
MiCOMS1
2nd RP (EIA485)
P2085ENc

Figure 4 - Second rear port EIA(RS)-485 example


"EIA(RS)232 Application" example
Master 1
Master 2
Note: 1 st RP could be any chosen protocol, 2 nd RP is always Courier
To SCADA
POWER SUPPLY
CENTRAL PROCESSOR
R.T.U.
modem
modem
EIA232
EIA232
EIA485
CK222
EIA232
EIA232 splitter
1st RP (Modbus / DNP/ IEC103)
EIA232
15m max
Front port
EIA232
MiCOMS1
2nd RP (EIA232)
P2086ENc

2 Master stations configuration: SCADA (Px40 1st RP) via CK222, EIA232 2nd rear port via remote PC, max EIA232 bus distance 15m, PC local front/rear access

Figure 5 - Second rear port EIA(RS)-232 example

3 COURIER INTERFACE

3.1 Courier Protocol

Courier is a Schneider Electric communication protocol. The concept of the protocol is that a standard set of commands is used to access a database of settings and data in the relay. This allows a generic master to be able to communicate with different slave devices. The application-specific aspects are contained in the database rather than the commands used to interrogate it, so the master station does not need to be preconfigured.

The same protocol can be used through two physical links K-Bus or EIA(RS)-232.

K-Bus is based on EIA(RS)-485 voltage levels with HDLC FM0 encoded synchronous signaling and its own frame format. The K-Bus twisted pair connection is unpolarized, whereas the EIA(RS)-485 and EIA(RS)-232 interfaces are polarized.

The EIA(RS)-232 interface uses the IEC60870-5 FT1.2 frame format.

The relay supports an IEC60870-5 FT1.2 connection on the front-port. This is intended for temporary local connection and is not suitable for permanent connection. This interface uses a fixed baud rate, 11-bit frame, and a fixed device address.

The rear interface is used to provide a permanent connection for K-Bus and allows multi-drop connection. Although K-Bus is based on EIA(RS)-485 voltage levels, it is a synchronous HDLC protocol using FM0 encoding. It is not possible to use a standard EIA(RS)-232 to EIA(RS)-485 converter to convert IEC60870-5 FT1.2 frames to K-Bus. Also it is not possible to connect K-Bus to an EIA(RS)-485 computer port. A protocol converter, such as the KITZ101, should be used for this purpose.

For a detailed description of the Courier protocol, command-set and link description, see the following documentation:

R6509	K-Bus Interface Guide
R6510	IEC60870 Interface Guide
R6511	Courier Protocol
R6512	Courier User Guide

3.2 Front Courier Port

The front EIA(RS)-232 9 pin port supports the Courier protocol for one-to-one communication. This port complies with EIA(RS)-574; the 9-pin version of EIA(RS)-232, see www.tiaonline.org. It is designed for use during installation and commissioning/maintenance and is not suitable for permanent connection. Since this interface is not used to link the relay to a substation communication system, some of the features of Courier are not implemented. These are as follows:

- Automatic extraction of Event Records:
  - Courier Status byte does not support the Event flag.
  - Send Event/Accept Event commands are not implemented.
- Automatic extraction of Disturbance records:
  - Courier Status byte does not support the Disturbance flag.
- Busy Response Layer:
  - Courier Status byte does not support the Busy flag, the only response to a request is the final data.

- Fixed Address:
  - The address of the front Courier port is always 1; the Change Device address command is not supported.
- Fixed Baud Rate:
  - 19200 bps.
  - Although automatic extraction of event and disturbance records is not supported, it is possible to manually access this data through the front port.

3.3 Supported Command Set

The following Courier commands are supported by the relay:

- Protocol Layer:

  Reset Remote Link
  Poll Status
  Poll Buffer*

- Low Level Commands:

  Send Event*
  Accept Event*
  Send Block
  Store Block Identifier
  Store Block Footer

- Menu Browsing:

  Get Column Headings
  Get Column Text
  Get Column Values
  Get Strings
  Get Text
  Get Value
  Get Column Setting Limits

- Setting Changes:

  Enter Setting Mode
  Preload Setting
  Abort Setting
  Execute Setting
  Reset Menu Cell
  Set Value

- Control Commands:

  Select Setting Group
  Change Device Address*
  Set Real Time

Note	*Commands marked with an asterisk (*) are not supported through the front Courier port.*

3.4 Relay Courier Database

The Courier database is two-dimensional. Each cell in the database is referenced by a row and column address. Both the column and the row can take a range from 0 to 255. Addresses in the database are specified as hexadecimal values, for example, 0A02 is column 0A (10 decimal) row 02. Associated settings or data are part of the same column. Row zero of the column has a text string to identify the contents of the column and to act as a column heading.

The *Relay Menu Database document P64x/EN MD* contains the complete database definition for the relay. For each cell location the following information is stated:

- Cell Text
- Cell Data type
- Cell value
- Whether the cell is settable, if so
- Minimum value
- Maximum value
- Step size
- Password Level required to allow setting changes
- String information (for Indexed String or Binary flag cells)

3.5 Setting Changes

(See R6512, Courier User Guide - Chapter 9)

Courier provides two mechanisms for making setting changes, both of these are supported by the relay. Either method can be used for editing any of the settings in the relay database.

3.5.1 Method 1

This uses a combination of three commands to perform a settings change:

Enter Setting Mode	Checks that the cell is settable and returns the limits.
Preload Setting	Places a new value to the cell. This value is echoed to ensure that setting corruption has not taken place. The validity of the setting is not checked by this action.
Execute Setting	Confirms the setting change. If the change is valid, a positive response is returned. If the setting change fails, an error response is returned.
Abort Setting	This command can be used to abandon the setting change.

This is the most secure method. It is ideally suited to on-line editors because the setting limits are taken from the relay before the setting change is made. However, this method can be slow if many settings are being changed because three commands are required for each change.

3.5.2 Method 2

The **Set Value** command can be used to directly change a setting, the response to this command is either a positive confirm or an error code to indicate the nature of a failure. This command can be used to implement a setting more rapidly than the previous method, however the limits are not extracted from the relay. This method is most suitable for off-line setting editors such as MiCOM S1 Studio, or for issuing preconfigured (SCADA) control commands.

3.5.3 Relay Settings

There are three categories of settings in the relay database:

- Control and support
- Disturbance recorder
- Protection settings group

Setting changes made to the control and support settings are implemented immediately and stored in non-volatile memory. Changes made to either the Disturbance recorder settings or the Protection Settings Groups are stored in a ‘scratchpad’ memory and are not immediately implemented by the relay.

To action setting changes stored in the scratchpad the Save **Changes cell** in the **Configuration** column must be written to. This allows the changes to either be confirmed and stored in non-volatile memory, or the setting changes to be aborted.

3.5.4 Setting Transfer Mode

If it is necessary to transfer all of the relay settings to or from the relay, a cell in the **Communication System Data** column can be used. This cell (location BF03) when set to 1 makes all of the relay settings visible. Any setting changes made with the relay set in this mode are stored in scratchpad memory, including control and support settings. When the value of BF03 is set back to 0, any setting changes are verified and stored in non-volatile memory.

3.6 Event Extraction

Events can be extracted either automatically (rear port only) or manually (either Courier port). For automatic extraction all events are extracted in sequential order using the standard Courier event mechanism, this includes fault/maintenance data if appropriate. The manual approach allows the user to select events, faults, or maintenance data at random from the stored records.

3.6.1 Automatic Event Extraction

(See Chapter 7 Courier User Guide, publication R6512).

This method is intended for continuous extraction of event and fault information as it is produced. It is only supported through the rear Courier port.

When new event information is created, the Event bit is set in the Status byte. This indicates to the Master device that event information is available. The oldest, unextracted event can be extracted from the relay using the Send Event command. The relay responds with the event data, which is either a Courier Type 0 or Type 3 event. The Type 3 event is used for fault records and maintenance records.

Once an event has been extracted from the relay, the Accept Event can be used to confirm that the event has been successfully extracted. If all events have been extracted, the event bit is reset. If there are more events still to be extracted, the next event can be accessed using the **Send Event** command as before.

3.6.2 Event Types

Events are created by the relay under these circumstances:

- Change of state of output contact
- Change of state of opto input
- Protection element operation
- Alarm condition
- Setting change
- Password entered/timed-out
- Fault record (Type 3 Courier Event)
- Maintenance record (Type 3 Courier Event)

3.6.3 Event Format

The Send Event command results in these fields being returned by the relay:

- Cell reference
- Time stamp
- Cell text
- Cell value

The *Relay Menu Database document, P64x/EN MD,* contains a table of the events created by the relay and indicates how the contents of the above fields are interpreted. Fault records and Maintenance records return a Courier Type 3 event, which contains the above fields with two additional fields:

- Event extraction column
- Event number

These events contain additional information that is extracted from the relay using the referenced extraction column. Row 01 of the extraction column contains a setting that allows the fault/maintenance record to be selected. This setting should be set to the event number value returned in the record. The extended data can be extracted from the relay by uploading the text and data from the column.

3.6.4 Manual Event Record Extraction

Column 01 of the database can be used for manual viewing of event, fault, and maintenance records. The contents of this column depend on the nature of the record selected. It is possible to select events by event number and to directly select a fault record or maintenance record by number.

Event Record selection (Row 01)

This cell can be set to a value between 0 to 249 to select from 250 stored events. 0 selects the most recent record and 249 the oldest stored record. For simple event records, (Type 0) cells 0102 to 0105 contain the event details. A single cell is used to represent each of the event fields. If the event selected is a fault or maintenance record (Type 3), the remainder of the column contains the additional information.

Fault Record Selection (Row 05)

This cell can be used to select a fault record directly, using a value between 0 and 4 to select one of up to five stored fault records. (0 is the most recent fault and 4 is the oldest). The column then contains the details of the fault record selected.

Maintenance Record Selection (Row F0)

This cell can be used to select a maintenance record using a value between 0 and 4. This cell operates in a similar way to the fault record selection.

If this column is used to extract event information from the relay, the number associated with a particular record changes when a new event or fault occurs.

3.7 Disturbance Record Extraction

The stored disturbance records in the relay are accessible in a compressed format through the Courier interface. The records are extracted using column B4. Cells required for extraction of uncompressed disturbance records are not supported.

Select Record Number (Row 01)

This cell can be used to select the record to be extracted. Record 0 is the oldest unextracted record, already extracted older records are assigned positive values, and negative values are used for more recent records. To help automatic extraction through the rear port, the Disturbance bit of the Status byte is set by the relay whenever there are unextracted disturbance records.

Once a record has been selected, using the above cell, the time and date of the record can be read from cell 02. The disturbance record can be extracted using the block transfer mechanism from cell B00B. The file extracted from the relay is in a compressed format. Use MiCOM S1 Studio to decompress this file and save the disturbance record in the COMTRADE format.

As has been stated, the rear Courier port can be used to extract disturbance records automatically as they occur. This operates using the standard Courier mechanism, see *Chapter 8 of the Courier User Guide*. The front Courier port does not support automatic extraction although disturbance record data can be extracted manually from this port.

3.8 Programmable Scheme Logic (PSL) Settings

The Programmable Scheme Logic (PSL) settings can be uploaded from and downloaded to the relay using the block transfer mechanism defined in Chapter 12 of the Courier User Guide.

These cells are used to perform the extraction:

- B204 Domain Used to select either PSL settings (upload or download) or PSL configuration data (upload only)
- B208 Sub-Domain Used to select the Protection Setting Group to be uploaded or downloaded.
- B20C Version Used on a download to check the compatibility of the file to be downloaded with the relay.
- B21C Transfer Mode Used to set up the transfer process.
- B120 Data Transfer Cell Used to perform upload or download.

The PSL settings can be uploaded and downloaded to and from the relay using this mechanism. If it is necessary to edit the settings, MiCOM S1 Studio must be used because the data is compressed. MiCOM S1 Studio also performs checks on the validity of the settings before they are downloaded to the relay.

4 MODBUS INTERFACE

The MODBUS interface is a master/slave protocol and is defined by:

www.modbus.org

MODBUS Serial Protocol Reference Guide: PI-MBUS-300 Rev. E

4.1 Serial Interface

The MODBUS interface uses the first rear EIA(RS)-485 (RS485) two-wire port “RP1”. The port is designated “EIA(RS)-485/K-Bus Port” on the external connection diagrams.

The interface uses the MODBUS RTU communication mode rather than the ASCII mode since it provides for more efficient use of the communication bandwidth and is in widespread use. This communication mode is defined by the MODBUS standard.

4.1.1 Character Framing

The character framing is 1 start bit, 8 data bits, either 1 parity bit and 1 stop bit, or two stop bits. This gives 11 bits per character.

4.1.2 Maximum MODBUS Query and Response Frame Size

The maximum query and response frame size is limited to 260 bytes in total. (This includes the frame header and CRC footer, as defined by the MODBUS protocol.).

4.1.3 User Configurable Communications Parameters

The following parameters can be configured for this port using the product’s front panel user interface (in the communications sub-menu):

Baud rate:	9600, 19200, 38400 bps
Device address:	1 - 247
Parity:	Odd, even, none.
Inactivity time:	1 - 30 minutes

Note *The inactivity timer is started (or restarted) whenever the active password level is reduced when a valid password is entered, or when a change is made to the setting scratchpad. When the timer expires, the password level is restored to its default level and any pending (uncommitted) setting changes on the scratch pad are discarded. The inactivity timer is disabled when the password level is at its default value and there are no settings pending on the scratchpad. See section 4.13.*

The MODBUS interface communication parameters are not part of the product’s setting file and cannot be configured with MiCOM S1 Studio.

4.2 Supported MODBUS Query Functions

The MODBUS protocol provides numerous query functions, of which the product supports the subset in Table 1. The product responds with exception code 01 if any other query function is received by it.

Query function code	MODBUS query name	Application
01	Read Coil Status	Read status of output contacts (0x addresses)
02	Read Input Status	Read status of opto-isolated status inputs (1x addresses)
03	Read Holding Registers	Read setting values (4x addresses)
04	Read Input Registers	Read measurement values (3x addresses)
06	Preset Single Register	Write single setting value (4x addresses)
07	Read Exception Status	Read relay status, same value as register 3x1
08	Diagnostics	Application defined by the MODBUS protocol specification
11	Fetch Communication Event Counter	
12	Fetch Communication Event Log	
16	Preset Multiple Registers	Write multiple setting values (4x addresses)

Table 1 - MODBUS query functions supported by the product

4.3 MODBUS Response Code Interpretation

Code	MODBUS response name	Product interpretation
01	Illegal Function Code	The function code transmitted is not supported.
02	Illegal Data Address	The start data address in the request is not an allowable value. If any of the addresses in the range cannot be accessed due to password protection, all changes in the request are discarded and this error response is returned. Note If the start address is correct but the range includes non-implemented addresses, this response is not produced.
03	Illegal Value	A value referenced in the data field transmitted by the master is not in range. Other values transmitted in the same packet are executed if they are in the range.
04	Slave Device Failure	An exception arose during the processing of the received query that is not covered by any of the other exception codes in this table.
05	Acknowledge	Not used.
06	Slave Device Busy	The write command cannot be implemented due to the product’s internal database being locked by another interface. This response is also produced if the product is busy executing a previous request.

Table 2 - MODBUS response code interpretation

4.4 Maximum Query and Response Parameters

Table 3 shows the maximum amount of data that the product can process for each of the supported query functions (see section 4.2) and the maximum amount of data that can be sent in a corresponding response frame. The principal constraint is the maximum query and response frame size, as noted in section 4.1.2. Maximum MODBUS query and response frame size.

Query function code	MODBUS query name	Maximum query data request size	Maximum response data size
01	Read Coil Status	32 coils	32 coils
02	Read Input Status	32 inputs	32 inputs
03	Read Holding Registers	127 registers	127 registers
04	Read Input Registers	127 registers	127 registers
06	Preset Single Register	1 register	1 register
07	Read Exception Status	-	8 coils
08	Diagnostics	-	-
11	Fetch Communication Event Counter	-	-
12	Fetch Communication Event Log	-	70 bytes
16	Preset Multiple Registers	127 registers	127 registers

Table 3 - Maximum query and response parameters for supported queries

4.5 Register Mapping

4.5.1 Conventions

4.5.1.1 Memory Pages

The MODBUS specification associates a specific register address space to each query that has a data address field. The address spaces are often called memory pages because they are analogous to separate memory devices. A simplistic view of the queries in MODBUS is that a specified location in a specified memory device is being read from or written to. However, the product’s implementation of such queries is not as a memory access but as a translation to an internal database query (see Note).

Note *One consequence of this is that the granularity of the register address space (in the 3x and 4x memory pages) is governed by the size of the data item being requested from the internal database. Since this is often more than the 16 bits of an individual register, not all register addresses are valid. See section 4.14 for more details.*

Each MODBUS memory page has a name and an ID. Table 4 provides a summary of the memory pages, their Ids, and their application in the product.

It is common practice to prefix a decimal register address with the page ID and generally this is the style used in this document.

Memory page ID	MODBUS memory page name	Product application
0x	Coil Status	Read and write access of the Output Relays.
1x	Input Status	Read only access of the Opto-Isolated Status Inputs.
3x	Input Registers	Read-only data access, such as measurements and records.
4x	Holding Registers	Read and write data access, such as product configurations settings and control commands.
6x	Extended Memory File	Not used or supported.

Table 4 - MODBUS "memory" pages reference and application

4.5.1.2 MODBUS Register Identification

The MODBUS convention is to document register identifiers with ordinal values (first, second, third…) whereas the actual protocol uses memory-page based register addresses that begin with address zero. Therefore the first register in a memory page is register address zero, the second register is register address 1 and so on. In general, one must be subtracted from a register's identifier to find its equivalent address. The page number notation is not part of the address.

Example:

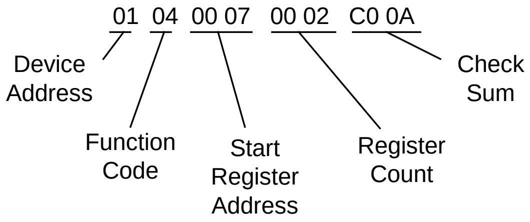
Task:

Obtain the status of the output contacts from the Schneider Electric P643 device at address 1.

The output contact status is a 32-bit binary string held in input registers 3x8 and 3x9 (see section 4.8).

Select MODBUS function code 4 "Read input registers" and request two registers starting at input register address 7. Note the register address is one less than the required register ordinal.

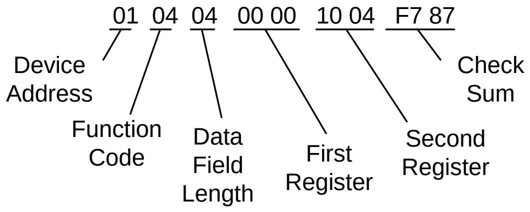
The MODBUS query frame is:



Note that the following frame data is shown in hexadecimal 8-bit bytes.

The frame is transmitted from left to right by the master device. The start register address, register count and check sum are all 16-bit numbers that are transmitted in a high byte - low byte order.

The query may elicit the following response: [4]



The frame was transmitted from left to right by the slave device. The response frame is valid because the eighth bit of the function code field is not set. The data field length is 4 bytes since the query was a read from two 16-bit registers. The data field consists of two pairs of bytes in a high byte - low byte order with the first requested register's data coming first. Therefore the request for the 32-bit output contact status starting at register 3x8 is 00001004h (1000000000100b), which shows that outputs 3 and 13 are energized and the remaining outputs are de-energized.

4.6 Register Map

For a complete map of the MODBUS addresses supported by the product, see the *Relay Menu Database document, P64x/EN MD*.

The register map tables in this document include an Equivalent Courier Cell column. The cell identifiers relate to the product's internal Courier database and may be used in cross-reference with the Courier Protocol documentation or the product's front panel user interface documentation.

The Data Format column specifies the format of the data presented by the associated MODBUS register or registers. *Section 4.14* describes the formats used.

The right-hand columns in the tables show whether the register is used in a particular product model. An asterisk indicates that the model uses the register.

4.7 Measurement Values

This table presents all of the product’s available measurements: analog values and counters. An asterisk indicates that the model uses the register. Their values are refreshed approximately every second.

Measurement name	Measurement unit	Equivalent courier cell		Start register	End register	Data format	Data size registers	Cell type	P642	P643	P645
Measurements 1		02	00								
IA-1 Magnitude	Amps	02	01	3x11200	3x11201	G24	2	Data	*	*	*
IA-1 Phase Angle	Degrees	02	02	3x11202		G30	1	Data	*	*	*
IB-1 Magnitude	Amps	02	03	3x11203	3x11204	G24	2	Data	*	*	*
IB-1 Phase Angle	Degrees	02	04	3x11205		G30	1	Data	*	*	*
IC-1 Magnitude	Amps	02	05	3x11206	3x11207	G24	2	Data	*	*	*
IC-1 Phase Angle	Degrees	02	06	3x11208		G30	1	Data	*	*	*
IA-2 Magnitude	Amps	02	07	3x11209	3x11210	G24	2	Data	*	*	*
IA-2 Phase Angle	Degrees	02	08	3x11211		G30	1	Data	*	*	*
IB-2 Magnitude	Amps	02	09	3x11212	3x11213	G24	2	Data	*	*	*
IB-2 Phase Angle	Degrees	02	0A	3x11214		G30	1	Data	*	*	*
IC-2 Magnitude	Amps	02	0B	3x11215	3x11216	G24	2	Data	*	*	*
IC-2 Phase Angle	Degrees	02	0C	3x11217		G30	1	Data	*	*	*
IA-3 Magnitude	Amps	02	0D	3x11218	3x11219	G24	2	Data		*	*
IA-3 Phase Angle	Degrees	02	0E	3x11220		G30	1	Data		*	*
IB-3 Magnitude	Amps	02	0F	3x11221	3x11222	G24	2	Data		*	*
IB-3 Phase Angle	Degrees	02	10	3x11223		G30	1	Data		*	*
IC-3 Magnitude	Amps	02	11	3x11224	3x11225	G24	2	Data		*	*
IC-3 Phase Angle	Degrees	02	12	3x11226		G30	1	Data		*	*
IA-4 Magnitude	Amps	02	13	3x11227	3x11228	G24	2	Data			*
IA-4 Phase Angle	Degrees	02	14	3x11229		G30	1	Data			*
IB-4 Magnitude	Amps	02	15	3x11230	3x11231	G24	2	Data			*
IB-4 Phase Angle	Degrees	02	16	3x11232		G30	1	Data			*
IC-4 Magnitude	Amps	02	17	3x11233	3x11234	G24	2	Data			*
IC-4 Phase Angle	Degrees	02	18	3x11235		G30	1	Data			*
IA-5 Magnitude	Amps	02	19	3x11236	3x11237	G24	2	Data			*
IA-5 Phase Angle	Degrees	02	1A	3x11238		G30	1	Data			*
IB-5 Magnitude	Amps	02	1B	3x11239	3x11240	G24	2	Data			*
IB-5 Phase Angle	Degrees	02	1C	3x11241		G30	1	Data			*
IC-5 Magnitude	Amps	02	1D	3x11242	3x11243	G24	2	Data			*
IC-5 Phase Angle	Degrees	02	1E	3x11244		G30	1	Data			*
IA-HV Magnitude	Amps	02	50	3x11308	3x11309	G24	2	Data	*	*	*
IA-HV Phase Ang	Degrees	02	51	3x11310		G30	1	Data	*	*	*
IB-HV Magnitude	Amps	02	52	3x11311	3x11312	G24	2	Data	*	*	*
IB-HV Phase Ang	Degrees	02	53	3x11313		G30	1	Data	*	*	*
IC-HV Magnitude	Amps	02	54	3x11314	3x11315	G24	2	Data	*	*	*
IC-HV Phase Ang	Degrees	02	55	3x11316		G30	1	Data	*	*	*
IA-LV Magnitude	Amps	02	56	3x11317	3x11318	G24	2	Data	*	*	*
IA-LV Phase Ang	Degrees	02	57	3x11319		G30	1	Data	*	*	*

Measurement name	Measurement unit	Equivalent courier cell		Start register	End register	Data format	Data size registers	Cell type	P642	P643	P645
IB-LV Magnitude	Amps	02	58	3x11320	3x11321	G24	2	Data	*	*	*
IB-LV Phase Ang	Degrees	02	59	3x11322		G30	1	Data	*	*	*
IC-LV Magnitude	Amps	02	5A	3x11323	3x11324	G24	2	Data	*	*	*
IC-LV Phase Ang	Degrees	02	5B	3x11325		G30	1	Data	*	*	*
IA-TV Magnitude	Amps	02	5C	3x11326	3x11327	G24	2	Data		*	*
IA-TV Phase Ang	Degrees	02	5D	3x11328		G30	1	Data		*	*
IB-TV Magnitude	Amps	02	5E	3x11329	3x11330	G24	2	Data		*	*
IB-TV Phase Ang	Degrees	02	5F	3x11331		G30	1	Data		*	*
IC-TV Magnitude	Amps	02	60	3x11332	3x11333	G24	2	Data		*	*
IC-TV Phase Ang	Degrees	02	61	3x11334		G30	1	Data		*	*
I0-1 Magnitude	Amps	02	62	3x11335	3x11336	G24	2	Data	*	*	*
I1-1 Magnitude	Amps	02	63	3x11337	3x11338	G24	2	Data	*	*	*
I2-1 Magnitude	Amps	02	64	3x11339	3x11340	G24	2	Data	*	*	*
IN-HV Mea Mag	Amps	02	65	3x11341	3x11342	G24	2	Data	*	*	*
IN-HV Mea Ang	Degrees	02	66	3x11343		G30	1	Data	*	*	*
IN-HV Deriv Mag IN-1 Derived Mag	Amps	02	67	3x11344	3x11345	G24	2	Data	*	*	*
IN-HV Deriv Ang IN-1 Derived Ang	Degrees	02	68	3x11346		G30	1	Data	*	*	*
I0-2 Magnitude	Amps	02	69	3x11347	3x11348	G24	2	Data	*	*	*
I1-2 Magnitude	Amps	02	6A	3x11349	3x11350	G24	2	Data	*	*	*
I2-2 Magnitude	Amps	02	6B	3x11351	3x11352	G24	2	Data	*	*	*
IN-LV Mea Mag	Amps	02	6C	3x11353	3x11354	G24	2	Data	*	*	*
IN-LV Mea Ang	Degrees	02	6D	3x11355		G30	1	Data	*	*	*
IN-LV Deriv Mag IN-2 Derived Mag	Amps	02	6E	3x11356	3x11357	G24	2	Data	*	*	*
IN-LV Deriv Ang IN-2 Derived Ang	Degrees	02	6F	3x11358		G30	1	Data	*	*	*
I0-3 Magnitude	Amps	02	70	3x11359	3x11360	G24	2	Data		*	*
I1-3 Magnitude	Amps	02	71	3x11361	3x11362	G24	2	Data		*	*
I2-3 Magnitude	Amps	02	72	3x11363	3x11364	G24	2	Data		*	*
IN-TV Mea Mag	Amps	02	73	3x11365	3x11366	G24	2	Data		*	*
IN-TV Mea Ang	Degrees	02	74	3x11367		G30	1	Data		*	*
IN-TV Deriv Mag IN-3 Derived Mag	Amps	02	75	3x11368	3x11369	G24	2	Data		*	*
IN-TV Deriv Ang IN-3 Derived Ang	Degrees	02	76	3x11370		G30	1	Data		*	*
I0-4 Magnitude	Amps	02	77	3x11371	3x11372	G24	2	Data			*
I1-4 Magnitude	Amps	02	78	3x11373	3x11374	G24	2	Data			*
I2-4 Magnitude	Amps	02	79	3x11375	3x11376	G24	2	Data			*
I0-5 Magnitude	Amps	02	7C	3x11380	3x11381	G24	2	Data			*
I1-5 Magnitude	Amps	02	7D	3x11382	3x11383	G24	2	Data			*
I2-5 Magnitude	Amps	02	7E	3x11384	3x11385	G24	2	Data			*
IA-HV RMS	Amps	02	86	3x11398	3x11399	G24	2	Data	*	*	*
IB-HV RMS	Amps	02	87	3x11400	3x11401	G24	2	Data	*	*	*

Measurement name	Measurement unit	Equivalent courier cell		Start register	End register	Data format	Data size registers	Cell type	P642	P643	P645
IC-HV RMS	Amps	02	88	3x11402	3x11403	G24	2	Data	*	*	*
IA-LV RMS	Amps	02	89	3x11404	3x11405	G24	2	Data	*	*	*
IB-LV RMS	Amps	02	8A	3x11406	3x11407	G24	2	Data	*	*	*
IC-LV RMS	Amps	02	8B	3x11408	3x11409	G24	2	Data	*	*	*
IA-TV RMS	Amps	02	8C	3x11410	3x11411	G24	2	Data		*	*
IB-TV RMS	Amps	02	8D	3x11412	3x11413	G24	2	Data		*	*
IC-TV RMS	Amps	02	8E	3x11414	3x11415	G24	2	Data		*	*
VAN Magnitude	Volts	02	8F	3x11416	3x11417	G24	2	Data		*	*
VAN Phase Angle	Degrees	02	90	3x11418		G30	1	Data		*	*
VBN Magnitude	Volts	02	91	3x11419	3x11420	G24	2	Data		*	*
VBN Phase Angle	Degrees	02	92	3x11421		G30	1	Data		*	*
VCN Magnitude	Volts	02	93	3x11422	3x11423	G24	2	Data		*	*
VCN Phase Angle	Degrees	02	94	3x11424		G30	1	Data		*	*
Vx Magnitude	Volts	02	95	3x11425	3x11426	G24	2	Data	*	*	*
Vx Phase Angle	Degrees	02	96	3x11427		G30	1	Data	*	*	*
V1 Magnitude	Volts	02	97	3x11428	3x11429	G24	2	Data		*	*
V2 Magnitude	Volts	02	98	3x11430	3x11431	G24	2	Data		*	*
V0 Magnitude	Volts	02	99	3x11432	3x11433	G24	2	Data		*	*
VN Derived Mag	Volts	02	9A	3x11434	3x11435	G24	2	Data		*	*
VN Derived Angle	Degrees	02	9B	3x11436		G30	1	Data		*	*
VAB Magnitude	Volts	02	9C	3x11437	3x11438	G24	2	Data		*	*
VAB Phase Angle	Degrees	02	9D	3x11439		G30	1	Data		*	*
VBC Magnitude	Volts	02	9E	3x11440	3x11441	G24	2	Data		*	*
VBC Phase Angle	Degrees	02	9F	3x11442		G30	1	Data		*	*
VCA Magnitude	Volts	02	A0	3x11443	3x11444	G24	2	Data		*	*
VCA Phase Angle	Degrees	02	A1	3x11445		G30	1	Data		*	*
VAN RMS	Volts	02	A2	3x11446	3x11447	G24	2	Data		*	*
VBN RMS	Volts	02	A3	3x11448	3x11449	G24	2	Data		*	*
VCN RMS	Volts	02	A4	3x11450	3x11451	G24	2	Data		*	*
Frequency	Hz	02	AA	3x11452		G30	1	Data	*	*	*
A Phase Watts	Watts	03	01	3x11500	3x11502	G29	3	Data		*	*
A Phase Watts	Watts	03	02	3x11503	3x11505	G29	3	Data		*	*
A Phase Watts	Watts	03	03	3x11506	3x11508	G29	3	Data		*	*
B Phase Watts	Watts	03	04	3x11509	3x11511	G29	3	Data		*	*
B Phase Watts	Watts	03	05	3x11512	3x11514	G29	3	Data		*	*
B Phase Watts	Watts	03	06	3x11515	3x11517	G29	3	Data		*	*
C Phase Watts	Watts	03	07	3x11518	3x11520	G29	3	Data		*	*
C Phase Watts	Watts	03	08	3x11521	3x11523	G29	3	Data		*	*
C Phase Watts	Watts	03	09	3x11524	3x11526	G29	3	Data		*	*
A Phase VArs	VAr	03	0A	3x11527	3x11529	G29	3	Data		*	*
A Phase VArs	VAr	03	0B	3x11530	3x11532	G29	3	Data		*	*
A Phase VArs	VAr	03	0C	3x11533	3x11535	G29	3	Data		*	*
B Phase VArs	VAr	03	0D	3x11536	3x11538	G29	3	Data		*	*

Measurement name	Measurement unit	Equivalent courier cell		Start register	End register	Data format	Data size registers	Cell type	P642	P643	P645
B Phase VArs	VAr	03	0E	3x11539	3x11541	G29	3	Data		*	*
B Phase VArs	VAr	03	0F	3x11542	3x11544	G29	3	Data		*	*
C Phase VArs	VAr	03	10	3x11545	3x11547	G29	3	Data		*	*
C Phase VArs	VAr	03	11	3x11548	3x11550	G29	3	Data		*	*
C Phase VArs	VAr	03	12	3x11551	3x11553	G29	3	Data		*	*
A Phase VA	VA	03	13	3x11554	3x11556	G29	3	Data		*	*
A Phase VA	VA	03	14	3x11557	3x11559	G29	3	Data		*	*
A Phase VA	VA	03	15	3x11560	3x11562	G29	3	Data		*	*
B Phase VA	VA	03	16	3x11563	3x11565	G29	3	Data		*	*
B Phase VA	VA	03	17	3x11566	3x11568	G29	3	Data		*	*
B Phase VA	VA	03	18	3x11569	3x11571	G29	3	Data		*	*
C Phase VA	VA	03	19	3x11572	3x11574	G29	3	Data		*	*
C Phase VA	VA	03	1A	3x11575	3x11577	G29	3	Data		*	*
C Phase VA	VA	03	1B	3x11578	3x11580	G29	3	Data		*	*
3 Phase Watts	Watts	03	1C	3x11581	3x11583	G29	3	Data		*	*
3 Phase Watts	Watts	03	1D	3x11584	3x11586	G29	3	Data		*	*
3 Phase Watts	Watts	03	1E	3x11587	3x11589	G29	3	Data		*	*
3 Phase VArs	VAr	03	1F	3x11590	3x11592	G29	3	Data		*	*
3 Phase VArs	VAr	03	20	3x11593	3x11595	G29	3	Data		*	*
3 Phase VArs	VAr	03	21	3x11596	3x11598	G29	3	Data		*	*
3 Phase VA	VA	03	22	3x11599	3x11601	G29	3	Data		*	*
3 Phase VA	VA	03	23	3x11602	3x11604	G29	3	Data		*	*
3 Phase VA	VA	03	24	3x11605	3x11607	G29	3	Data		*	*
3Ph Power Factor	% pf	03	25	3x11608		G30	1	Data		*	*
APh Power Factor	% pf	03	26	3x11609		G30	1	Data		*	*
BPh Power Factor	% pf	03	27	3x11610		G30	1	Data		*	*
CPh Power Factor	% pf	03	28	3x11611		G30	1	Data		*	*
3Ph WHours Fwd	Wh	03	29	3x11612	3x11614	G29	3	Data		*	*
3Ph WHours Rev	Wh	03	2A	3x11615	3x11617	G29	3	Data		*	*
3Ph VArHours Fwd	VArh	03	2B	3x11618	3x11620	G29	3	Data		*	*
3Ph VArHours Rev	VArh	03	2C	3x11621	3x11623	G29	3	Data		*	*
3Ph W Fix Demand	Watts	03	2D	3x11624	3x11626	G29	3	Data		*	*
3Ph VArs Fix Demand	VArs	03	2E	3x11627	3x11629	G29	3	Data		*	*
3 Ph W Roll Dem	Watts	03	2F	3x11630	3x11632	G29	3	Data		*	*
3 Ph VArs Roll Dem	VAr	03	30	3x11633	3x11635	G29	3	Data		*	*
3Ph W Peak Dem	Watts	03	31	3x11636	3x11638	G29	3	Data		*	*
3Ph VAr Peak Dem	VAr	03	32	3x11639	3x11641	G29	3	Data		*	*
Reset Demand	Indexed String	03	50	4x00103		G11	1	Data		*	*
IA Differential IA Z1 Diff	Amps	04	01	3x11750	3x11751	G24	2	Data	*	*	*
IB Differential IB Z1 Diff	Amps	04	02	3x11752	3x11753	G24	2	Data	*	*	*
IC Differential IC Z1 Diff	Amps	04	03	3x11754	3x11755	G24	2	Data	*	*	*

Measurement name	Measurement unit	Equivalent courier cell		Start register	End register	Data format	Data size registers	Cell type	P642	P643	P645
IA Bias IA Z1 Bias	Amps	04	04	3x11756	3x11757	G24	2	Data	*	*	*
IB Bias IB Z1 Bias	Amps	04	05	3x11758	3x11759	G24	2	Data	*	*	*
IC Bias IC Z1 Bias	Amps	04	06	3x11760	3x11761	G24	2	Data	*	*	*
IA Diff 2H IA Z1 Diff 2H	Amps	04	07	3x11762	3x11763	G24	2	Data	*	*	*
IB Diff 2H IB Z1 Diff 2H	Amps	04	08	3x11764	3x11765	G24	2	Data	*	*	*
IC Diff 2H IC Z1 Diff 2H	Amps	04	09	3x11766	3x11767	G24	2	Data	*	*	*
IA Diff 5H IA Z2 Diff	Amps	04	0A	3x11768	3x11769	G24	2	Data	*	*	*
IB Diff 5H IB Z2 Diff	Amps	04	0B	3x11770	3x11771	G24	2	Data	*	*	*
IC Diff 5H IC Z2 Diff	Amps	04	0C	3x11772	3x11773	G24	2	Data	*	*	*
IREF HV LoZ Diff IA Z2 Bias	Amps	04	0D	3x11774	3x11775	G24	2	Data	*	*	*
IREF HV LoZ Bias IB Z2 Bias	Amps	04	0E	3x11776	3x11777	G24	2	Data	*	*	*
IREF LV LoZ Diff	Amps	04	0F	3x11778	3x11779	G24	2	Data	*	*	*
IREF LV LoZ Bias IA Z2 Diff 2H	Amps	04	10	3x11780	3x11781	G24	2	Data	*	*	*
IREF TV LoZ Diff IB Z2 Diff 2H	Amps	04	11	3x11782	3x11783	G24	2	Data		*	*
IREF TV LoZ Bias IC Z2 Diff 2H	Amps	04	12	3x11784	3x11785	G24	2	Data		*	*
Hot Spot T	°C	04	28	3x11798		G10	1	Data	*	*	*
Top Oil T	°C	04	2A	3x11799		G10	1	Data	*	*	*
Ambient T	°C	04	2C	3x11800		G10	1	Data	*	*	*
TOL Pretrip left	Courier Number (decimal)	04	2D	3x11801	3x11802	G24	2	Data	*	*	*
LOL status	Courier Number (decimal)	04	2F	3x11803	3x11804	G27	2	Data	*	*	*
Rate of LOL	Courier Number (decimal)	04	31	3x11805		G24	2	Data	*	*	*
LOL Aging Factor	Courier Number (decimal)	04	32	3x11807	3x11808	G27	2	Data	*	*	*
Lres at designed	Courier Number (decimal)	04	33	3x11809	3x11810	G27	2	Data	*	*	*
FAA,m	Courier Number (decimal)	04	34	3x11811	3x11812	G27	2	Data	*	*	*
Lres at FAA,m	Courier Number (decimal)	04	35	3x11813	3x11814	G24	2	Data	*	*	*
Volts/Hz	(Sub Heading)	04	38						*	*	*
Volts/Hz W1	Volts/Hz	04	39	3x11815		G24	2	Data		*	*

Measurement name	Measurement unit	Equivalent courier cell		Start register	End register	Data format	Data size registers	Cell type	P642	P643	P645
V/Hz W1 tPretrip	Courier Number (time)	04	3A	3x11817	3x11818	G24	2	Data		*	*
V/Hz W1 Thermal	Courier Number (time)	04	3B	3x11819	3x11820	G24	2	Data		*	*
Volts/Hz W2	Volts/Hz	04	3D	3x11821		G24	2	Data	*	*	*
V/Hz W2 tPretrip	Courier Number (time)	04	3E	3x11823	3x11824	G24	2	Data	*	*	*
V/Hz W2 Thermal	Courier Number (time)	04	3F	3x11825	3x11826	G24	2	Data	*	*	*
RTD 1 label	Courier Number (decimal)	04	60	3x11827		G10	1	Data	*	*	*
RTD 2 label	Courier Number (decimal)	04	61	3x11828		G10	1	Data	*	*	*
RTD 3 label	Courier Number (decimal)	04	62	3x11829		G10	1	Data	*	*	*
RTD 4 label	Courier Number (decimal)	04	63	3x11830		G10	1	Data	*	*	*
RTD 5 label	Courier Number (decimal)	04	64	3x11831		G10	1	Data	*	*	*
RTD 6 label	Courier Number (decimal)	04	65	3x11832		G10	1	Data	*	*	*
RTD 7 label	Courier Number (decimal)	04	66	3x11833		G10	1	Data	*	*	*
RTD 8 label	Courier Number (decimal)	04	67	3x11834		G10	1	Data	*	*	*
RTD 9 label	Courier Number (decimal)	04	68	3x11835		G10	1	Data	*	*	*
RTD 10 label	Courier Number (decimal)	04	69	3x11836		G10	1	Data	*	*	*
RTD Open Cct	Binary Flag (10 bits)	04	6A	3x11837		G108	1	Data	*	*	*
RTD Short Cct	Binary Flag (10 bits)	04	6B	3x11838		G109	1	Data	*	*	*
RTD Data Error	Binary Flag (10 bits)	04	6C	3x11839		G110	1	Data	*	*	*
CLIO Input 1	Courier Number (Decimal)	04	70	3x11840	3x11841	G125	2	Data	*	*	*
CLIO Input 2	Courier Number (Decimal)	04	71	3x11842	3x11843	G125	2	Data	*	*	*
CLIO Input 3	Courier Number (Decimal)	04	72	3x11844	3x11845	G125	2	Data	*	*	*
CLIO Input 4	Courier Number (Decimal)	04	73	3x11846	3x11847	G125	2	Data	*	*	*

Table 5 - Measurement data available in the P64x product range

4.8 Binary Status Information

Binary status information is available for the product’s optically-isolated status inputs (optos), relay contact outputs, alarm flags, control inputs, internal Digital Data Bus (DDB), and the front panel 25-pin test port (see Note).

Note	*The test port allows the product to be configured to map up to eight of its DDB signals (see the Relay Menu Database document, P64x/EN MD) to eight output pins. The usual application is to control test equipment. However, since the test port output status is available on the MODBUS interface, it could be used to efficiently collect up to eight DDB signals.*

The product’s internal DDB consists of 1023 binary-status flags. The allocation of the points in the DDB are largely product and version specific. See the *Relay Menu Database document, P64x/EN MD*, for a definition of the product’s DDB.

The relay-contact status information is available from the 0x “Coil Status” MODBUS page and from the 3x “Input Register” MODBUS page. For legacy reasons the information is duplicated in the 3x page with explicit registers (8 & 9) and in the DDB status register area (723 & 724).

The current state of the optically isolated status inputs is available from the 1x “Input Status” MODBUS page and from the 3x “Input Register” MODBUS page. The principal 3x registers are part of the DDB status register area (725 & 726). For legacy reasons, a single register at 3x00007 provides the status of the first 16 inputs.

The 0x “Coil Status” and 1x “Input Status” pages allow individual or blocks of binary status flags to be read. The resultant data is left aligned and transmitted in a big-endian (high-order to low-order) format in the response frame. Relay contact 1 is mapped to coil 1, contact 2 to coil 2 and so on. Similarly, opto input 1 is mapped to input 1, opto input 2 to input 2 and so on.

Table 7 shows the available 3x and 4x binary status information.

Name	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	P642	P643	P645
Opto I/P Status	0030	3x11027	3x11028	G8	2	*	*	*
Relay O/P Status	0040	3x00008	3x00009	G9	2	*	*	*
Alarm Status 1	0050	3x00011	3x00012	G96	2	*	*	*
Alarm Status 2	0051	3x00013	3x00014	G128	2	*	*	*
Alarm Status 3	0052	3x00015	3x00016	G228	2	*	*	*
Ctrl I/P Status	1201	4x00950	4x00951	G202	2	*	*	*
Relay Test Port Status	0F03	3x00722		G1	1	*	*	*
DDB 31 - 0	0F20	3x11023	3x11024	G27	2	*	*	*
DDB 63 - 32	0F21	3x11025	3x11026	G27	2	*	*	*
DDB 95 - 64	0F22	3x11027	3x11028	G27	2	*	*	*
DDB 127 - 96	0F23	3x11029	3x11030	G27	2	*	*	*
DDB 159 - 128	0F24	3x11031	3x11032	G27	2	*	*	*
DDB 191 - 160	0F25	3x11033	3x11034	G27	2	*	*	*
DDB 223 - 192	0F26	3x11035	3x11036	G27	2	*	*	*
DDB 255 - 224	0F27	3x11037	3x11038	G27	2	*	*	*
DDB 287 - 256	0F28	3x11039	3x11040	G27	2	*	*	*
DDB 319 - 288	0F29	3x11041	3x11042	G27	2	*	*	*
DDB 351 - 320	0F2A	3x11043	3x11044	G27	2	*	*	*
DDB 383 - 352	0F2B	3x11045	3x11046	G27	2	*	*	*
DDB 415 - 384	0F2C	3x11047	3x11048	G27	2	*	*	*

Name	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	P642	P643	P645
DDB 447 - 416	0F2D	3x11049	3x11050	G27	2	*	*	*
DDB 479 - 448	0F2E	3x11051	3x11052	G27	2	*	*	*
DDB 511 - 480	0F2F	3x11053	3x11054	G27	2	*	*	*
DDB 543 - 512	0F30	3x11055	3x11056	G27	2	*	*	*
DDB 575 - 544	0F31	3x11057	3x11058	G27	2	*	*	*
DDB 607 - 576	0F32	3x11059	3x11060	G27	2	*	*	*
DDB 639 - 608	0F33	3x11061	3x11062	G27	2	*	*	*
DDB 671 - 640	0F34	3x11063	3x11064	G27	2	*	*	*
DDB 703 - 672	0F35	3x11065	3x11066	G27	2	*	*	*
DDB 735 - 704	0F36	3x11067	3x11068	G27	2	*	*	*
DDB 767 - 736	0F37	3x11069	3x11070	G27	2	*	*	*
DDB 799 - 768	0F38	3x11071	3x11072	G27	2	*	*	*
DDB 831 - 800	0F39	3x11073	3x11074	G27	2	*	*	*
DDB 863 - 832	0F3A	3x11075	3x11076	G27	2	*	*	*
DDB 895 - 864	0F3B	3x11077	3x11078	G27	2	*	*	*
DDB 927 - 896	0F3C	3x11079	3x11080	G27	2	*	*	*
DDB 959 - 928	0F3D	3x11081	3x11082	G27	2	*	*	*
DDB 991 - 960	0F3E	3x11083	3x11084	G27	2	*	*	*
DDB 1023 - 992	0F3F	3x11085	3x11086	G27	2	*	*	*
DDB 1055-1024	0F40	3x11087	3x11088	G27	2	*	*	*
DDB 1087-1056	0F41	3x11089	3x11090	G27	2	*	*	*
DDB 1119-1088	0F42	3x11091	3x11092	G27	2	*	*	*
DDB 1151-1120	0F43	3x11093	3x11094	G27	2	*	*	*
DDB 1183-1152	0F44	3x11095	3x11096	G27	2	*	*	*
DDB 1215-1184	0F45	3x11097	3x11098	G27	2	*	*	*
DDB 1247-1216	0F46	3x11099	3x11100	G27	2	*	*	*
DDB 1279-1248	0F47	3x11101	3x11102	G27	2	*	*	*
DDB 1311-1280	0F48	3x11103	3x11104	G27	2	*	*	*
DDB 1343-1312	0F49	3x11105	3x11106	G27	2	*	*	*
DDB 1375-1344	0F4A	3x11107	3x11108	G27	2	*	*	*
DDB 1407-1376	0F4B	3x11109	3x11110	G27	2	*	*	*
DDB 1439-1408	0F4C	4x10493	4x10494	G27	2	*	*	*
DDB 1471-1440	0F4D	4x10493	4x10494	G27	2	*	*	*
DDB 1503-1472	0F4E	4x10493	4x10494	G27	2	*	*	*
DDB 1535-1504	0F4F	4x10493	4x10494	G27	2	*	*	*
DDB 1567-1536	0F50	4x10493	4x10494	G27	2	*	*	*
DDB 1599-1568	0F51	4x10493	4x10494	G27	2	*	*	*
DDB 1631-1600	0F52	4x10493	4x10494	G27	2	*	*	*
DDB 1663-1632	0F53	4x10493	4x10494	G27	2	*	*	*
DDB 1695-1664	0F54	4x10493	4x10494	G27	2	*	*	*
DDB 1727-1696	0F55	4x10493	4x10494	G27	2	*	*	*
DDB 1759-1728	0F56	4x10493	4x10494	G27	2	*	*	*
DDB 1791-1760	0F57	4x10493	4x10494	G27	2	*	*	*
DDB 1823-1792	0F58	4x10493	4x10494	G27	2	*	*	*
DDB 1855-1824	0F59	4x10493	4x10494	G27	2	*	*	*
DDB 1887-1856	0F5A	4x10493	4x10494	G27	2	*	*	*
DDB 1919-1888	0F5B	4x10493	4x10494	G27	2	*	*	*

Name	Equivalent courier cell	Start register	End register	Data format	Data size (registers)	P642	P643	P645
DDB 1951-1920	0F5C	4x10493	4x10494	G27	2	*	*	*
DDB 1983-1952	0F5D	4x10493	4x10494	G27	2	*	*	*
DDB 2015-1984	0F5E	4x10493	4x10494	G27	2	*	*	*
DDB 2047-2016	0F5F	4x10493	4x10494	G27	2	*	*	*

Table 6 - Binary status information available in the P64x product range

4.9 Measurement and Binary Status 3x Register Sets

The data available from the 3x input registers is arranged into register sets. A register set is a fixed collection of values in a contiguous block of register addresses. The advantage of this is that multiple values may be read with a single MODBUS query, function code 4 “Read Input Registers”, up to the maximum data limits of the query, *see section 4.4*.

The definition of a register-set is specified by the selection of a start and end address, which can span multiple contiguous values in the 3x Register, see the *Relay Menu Database document, P64x/EN MD*. The only rule is that a register set must not result in an attempt to read only part of a multi-register data type, see *section 4.14*. A register set can span unused register locations, in which case a value of zero is returned for each such register location.

Some examples of useful register sets are:

- 3x701 to 3x786 provide a selection of measurement and binary-status values. Some of these registers are duplicates of other register values.
- 3x723 to 3x786 provide the DDB status.
- 3x391 to 3x408 provide the per phase power measurements in floating point format.
- 3x409 to 3x414 provide the three-phase power measurements in floating point format.
- 3x184 to 3x193 provide the ten RTD measurement values (P642/P643 only).

There are many other possibilities depending on your application and an appraisal of the 3x Register Map in the *Relay Menu Database document, P64x/EN MD.* The capabilities of the MODBUS master device, performance targets, and communications latencies may also influence the degree to which multiple values are read as register sets, as opposed to individually.

4.10 Controls

The following table presents MODBUS 4x “Holding Registers” that allow the external system to control aspects of the product’s behavior, configuration, records, or items of plant connected to the product such as circuit breakers.

The **Command or setting** column indicates whether the control is a self-resetting “Command” or a state based “Setting”.

“Command” controls automatically return to their default value when the control action has been completed. This may cause problems with masters that try to verify write requests by reading back the value that was written.

“Setting” controls maintain the written value, assuming that it was accepted. For example, the **Active Settings** register reports the current active group on reads. The Active Setting Group register also accepts writes with a valid setting group number to change the active group to the one specified. This assumes that the setting group selection by optically isolated status inputs has not been enabled and that the specified group is enabled.

Entries without a defined setting range, as for the **min.**, **max.** and **step** columns, are binary-string values whose pattern is defined by its stated data type.

4.11 Event Extraction

The product can store up to 512 event records in battery backed-up memory. An event record consists of a time stamp, a record type, and a set of information fields. The record type and the information fields record the event that occurred at the time captured by the time stamp.

The product has several classes of event record:

- Alarm events
- Opto-isolated status input events
- Relay contact output events
- Protection/DDB operation events
- Fault data capture events
- General events

The *Relay Menu Database document, P64x/EN MD* specifies the available events. The product provides an “event filtering” feature that may be used to prevent specific events from being logged. The event filter is configured in the **Record Control** section of the product’s menu database in the MiCOM S1 Studio configuration tool.

The product supports two methods of event extraction providing either automatic or manual extraction of the stored event, fault, and maintenance records.

The product stores event, fault, and maintenance records in three separate queues. As entries are added to the fault and maintenance queues, a corresponding event is added to the event queue. Each queue is of different length and each queue may be individually cleared, *see section 4.11.4*. It is therefore possible to have a fault event or a maintenance event entry in the event queue with no corresponding entry in the associated queue because it has been overwritten or deleted.

The manual extraction procedure (see *section 4.11.1*) allows each of these three queues to be read independently.

The automatic extraction procedure (see *section 4.11.2*) reads records from the event queue. If the event record is a fault or a maintenance record, the record’s extended data is read also, if it is available from their queues.

Note	*Version 31 of the product introduced a new set of 3x registers for the presentation of the event and fault record data. These registers are used throughout the text of the following sub-sections. For legacy compatibility, the original registers are still provided. These are described as previous MODBUS addresses in the Relay Menu Database document, P64x/EN MD. They should not be used for new installations. See section 4.11.5 for additional information.*

4.11.1 Manual Extraction Procedure

There are three registers used to manually select stored records. For each of these registers, zero represents the most-recent stored record. For example:

- 4x00100 - Select Event, 0 to 511.
  511 was 249 in P640 software revisions 01, 02, 03, 04, 05, 06, & 07, since they only stored 250 event records.
- 4x00101 - Select Fault, 0 to 4
- 4x00102 - Select Maintenance Record, 0 to 4

There are also three read-only registers used to determine the number of various types of stored records. For example:

- 3x10000 - Number of stored event records
- 3x10001 - Number of stored fault records
- 3x10002 - Number of stored maintenance records

Each fault or maintenance record logged causes an event record to be created by the product. If this event record is selected, the additional registers showing the fault or maintenance record details are also populated.

4.11.2 Automatic Extraction Procedure

Automatic event-record extraction allows records to be extracted as they occur. Event records are extracted in sequential order, including any fault or maintenance data that may be associated with an event.

The MODBUS master can determine whether the product has any events stored that have not yet been extracted. This is done by reading the product’s status register 3x00001 (G26 data type). If the event bit of this register is set, the product contains event records that have not yet been extracted.

To select the next event for sequential extraction, the master station writes a value of one to the record selection register 4x00400 (G18 data type). The event data, plus any fault or maintenance data, can be read from the registers specified in *section 4.11.3*. Once the data has been read, the event record is marked. This is done by writing a value of 2 to register 4x00400. The G18 data type consists of bit fields. Therefore it is also possible to both mark the current record as read and automatically select the next unread record. This is done by writing a value of 3 to the register.

When the last (most recent) record is accepted, the event flag in the status register (3x00001) resets. If the last record is accepted by writing a value of 3 to the record selection register (4x00400), a dummy record appears in the event-record registers with an “Event Type” value of 255. Selecting another record when none are available gives a MODBUS exception code 3, “Invalid value” (see *section 4.3*).

One possible event record extraction procedure is shown in Figure 6.

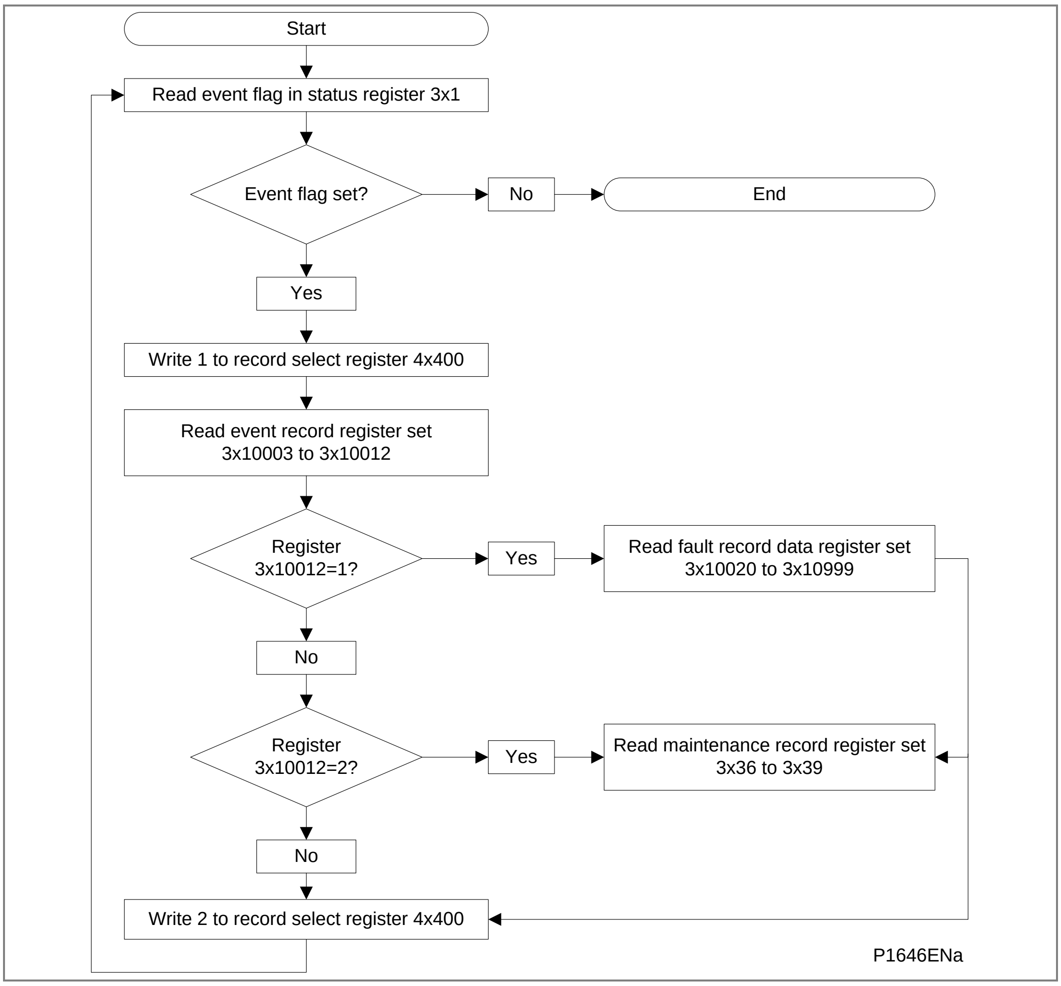

Start
Read event flag in status register 3x1
Event flag set?
No
End
Yes
Write 1 to record select register 4x400
Read event record register set 3x10003 to 3x10012
Register 3x10012=1?
Yes
Read fault record data register set 3x10020 to 3x10999
No
Register 3x10012=2?
Yes
Read maintenance record register set 3x36 to 3x39
No
Write 2 to record select register 4x400
P1646ENa

Figure 6 - Automatic event extraction procedure

4.11.3 Record Data

The location and format of the registers used to access the record data is the same whether they have been selected using manual or automatic extraction mechanisms, see *sections 4.11.1 and 4.11.2*.

Description	Register	Length (registers)	Comments
Time Stamp	3x10003	4	See G12 data type in the Relay Menu Database document, P64x/EN MD.
Event Type	3x10007	1	Indicates the type of the event record. See G13 data type in the Relay Menu Database document, P64x/EN MD (a value of 255 indicates that the end of the event log has been reached).
Event Value	3x10008	2	Contains the associated status register value as a string of binary flags for relay-contact, opto-input, alarm, and protection events. Otherwise it has a value of zero. When a status value is supplied, the value represents the recorded value of the event types associated register pair, as indicated by the Event Origin value (see Note 1).

Description	Register	Length (registers)	Comments
Event Origin	3x10010	1	The Event Original value indicates the MODBUS Register pair where the change occurred (see Note 2). Possible values are: 30011: Alarm Status 1 event 30013: Alarm Status 2 event 30015: Alarm Status 3 event 30723: Relay contact event (2 registers: DDB 0-31 status) 30725: Status input event (2 registers: DDB 32-63 status) 30727 to 30785: Protection events (Indicates the 32-bit DDB status word that was the origin of the event) For General events, Fault events, and Maintenance events, a value of zero is returned.
Event Index	3x10011	1	The Event Index value is used to distinguish between events with the same Event Type and Event Origin. The registers value depends on the type of the event: For protection events, the value is the ID of the DDB that caused the event. For alarm events, the value is the ID of the alarm that caused the event. In both cases, the value includes the direction of the state transition in the Most Significant Bit. This direction bit is 1 for a 0-1 (low to high) change, and 0 for a 1-0 (high to low) change. For all other types of events, it has a value of zero.
Additional Data Present	3x10012	1	Indicates whether the record has additional data. 0: Indicates that there is no additional data. 1: Indicates that fault record data can be read from 3x10020 to 3x10999 (see Note 3). 2: Indicates that maintenance record data can be read from registers 3x36 to 3x39.

Note 1 *The protection-event status information is the value of the DDB status word that contains the protection DDB that caused the event.*

Note 2 *Subtracting 3000 from the Event Origin value results in the MODBUS 3x memory-page register ID, subtracting one from this results in the MODBUS register address - see section 4.5.1.2. The resultant register address can be used in a function code 4 MODBUS query.*

Note 3 *The exact number of fault record registers depends on the individual product - see Relay Menu Database, P64x/EN GC.*

Table 7 - Event record extraction registers

If a fault record or maintenance record is directly selected using the manual mechanism, the data can be read from the fault or maintenance data register ranges specified in Table 8. The event record data in registers 3x10003 to 3x10012 is not valid.

See the *Relay Menu Database document, P64x/EN MD* for the record values for each event.

The general procedure for decoding an event record is to use the value of the **Event Type** field combined with the value of the **Event Index** field to uniquely identify the event. The exceptions to this are event types 4, 5, 7, 8, & 9.

Event types 4 **Relay Contact Output Events** and 5 **Opto-Isolated Status Input Events** only provide the value of the input or output status register (as indicated by the Event Origin value) when the event occurred. If event transition information for each input or output is required, it must be deduced by comparing the event value with the previous event value (for identically-typed events records).

Event type 7 **General Event** events are solely identified by their **Event Value**.

Event types 8 **Fault Record** and 9 **Maintenance Record** require additional registers to be read when the associated additional data is available (see Note). The Fault record registers in the range 3x10020 to 3x10999 (the exact number of registers depends on the individual product) are documented in the 3x register-map in the *Relay Menu Database document, P64x/EN MD*. The two additional 32-bit maintenance record register-pairs consist of a maintenance record type (register pair 3x36/7) and a type-specific error code (register pair 3x38/9). Table 8 lists the different types of maintenance record available from the product.

Note	*As noted at the beginning of section 4.11, it should not be assumed that the additional data is available for fault and maintenance record events.*

Maintenance record	Front panel text	Record type 3x00036
Power on test errors (non-fatal)		
Watchdog 1 failure (fast)	Fast W'Dog Error	0
Battery fail	Battery Failure	1
Battery-backed RAM failure	BBRAM Failure	2
Field voltage failure	Field Volt Fail	3
Ribbon bus check failure	Bus Reset Error	4
Watchdog 2 failure (slow)	Slow W'Dog Error	5
Continuous self-test errors		
SRAM bus failure	SRAM Failure Bus	6
SRAM cell failure	SRAM Failure Blk.	7
Flash EPROM checksum failure	FLASH Failure	8
Program code verify failure	Code Verify Fail	9
Battery-backed RAM failure	BBRAM Failure	10
Battery fail	Battery Failure	11
Field Voltage failure	Field Volt Fail	12
EEPROM failure	EEPROM Failure	13
Fatal software exception	Software Failure	14
Incorrect hardware configuration	H/W Verify Fail	15
Software exception (typically non-fatal)	Non Standard	16
Analog module failure	Ana. Sample Fail	17
Ethernet card error	NIC Soft Error	18

Table 8 - Maintenance record types

4.11.4 Event Record Deletion

It is possible to independently delete (“clear”) the stored event, fault, and maintenance record queues. This is done by writing a value of 1, 2, or 3 to register 4x401 (G6 data type), respectively.

Register 4x401 also provides an option to reset the product’s front panel indications, which has the same effect as pressing the front panel “Clear” key when viewing alarm indications using the front panel user interface. This is done by writing a value of 4 to register 4x401.

See also section 4.12.4 for details about deleting disturbance records.

4.11.5 Legacy Event Record Support

Version 31 of the P64x product introduced a new set of 3x registers for the presentation of the event and fault record data. For legacy compatibility, the original registers are supported and are described in this section. They should not be used for new installations and they are correspondingly described as previous MODBUS address in the 3x-register table in the *Relay Menu Database document, P64x/EN MD*.

Table 9 provides a mapping between the obsolete event record 3x-registers and the registers used in the event record discussions in the previous sub-sections.

The obsolete fault record data between registers 3x113 and 3x199, and 3x490 and 3x499, now exists between registers 3x10020 and 3x10999. In comparison with the obsolete fault record data, the data between registers 3x10020 and 3x10999 is ordered slightly differently and it contains new data values. These new values since version 31 of the product are not available in the obsolete fault-record register sets.

The maintenance-record registers 3x36 to 3x39 remain unaffected by this evolution.

Description	Obsolete register	Length (registers)	Corresponds to register
Number of stored event records	3x00100	1	3x10000
Number of stored fault records	3x00101	1	3x10001
Number of stored maintenance records	3x00102	1	3x10002
Time Stamp	3x00103	4	3x10003
Event Type	3x00107	1	3x10007
Event Value	3x00108	2	3x10008
Event Origin	3x00110	1	3x10010
Event Index	3x00111	1	3x10011
Additional Data Present	3x00112	1	3x10012

Table 9 - Correspondence of obsolete event record 3x registers with their counterparts

4.12 Disturbance Record Extraction

The product provides facilities for both manual and automatic extraction of disturbance records. The two methods differ only in the mechanism for selecting a disturbance record; the method for extracting the data and the format of the data are identical.

Records extracted are presented in IEEE COMTRADE format. This involves extracting two files: an ASCII text configuration file, and a binary data file.

Each file is extracted by repeatedly reading a data-page until all of the file's data has been transferred. The data-page is made up of 127 registers; providing a maximum of 254 bytes for each register block request.

4.12.1 Interface Registers

The following set of registers is presented to the master station to support the extraction of uncompressed disturbance records:

Register	Name	Description
3x00001	Status register	Provides the status of the product as bit flags: b0 Out of service b1 Minor self test failure b2 Event b3 Time synchronization b4 Disturbance b5 Fault b6 Trip b7 Alarm b8 to b15 Unused A ‘1’ in bit “b4” indicates the presence of one or more disturbance records.

Register	Name	Description
3x00800	Number of stored disturbances	Indicates the total number of disturbance records currently stored in the product, both extracted and unextracted.
3x00801	Unique identifier of the oldest disturbance record	Indicates the unique identifier value for the oldest disturbance record stored in the product. This is an integer value used with the **Number of stored disturbances** value to calculate a value for manually selecting records.
4x00250	Manual disturbance record selection register	This register is used to manually select disturbance records. The values written to this cell are an offset of the unique identifier value for the oldest record. The offset value, which ranges from 0 to the N^o of stored disturbances - 1, is added to the identifier of the oldest record to generate the identifier of the required record.
4x00400	Record selection command register	This register is used during the extraction process and has several commands. These are: b0 Select next event b1 Accept event b2 Select next disturbance record b3 Accept disturbance record b4 Select next page of disturbance data b5 Select data file
3x00930 to 3x00933	Record time stamp	These registers return the timestamp of the disturbance record.
3x00802	Number of registers in data page	This register informs the master station of the number of registers in the data page that are populated.
3x00803 to 3x00929	Data page registers	These 127 registers are used to transfer data from the product to the master station.
3x00934	Disturbance record status register	The disturbance record status register is used during the extraction process to indicate to the master station when data is ready for extraction. See Table 13.
4x00251	Data file format selection	This is used to select the required data file format. This is reserved for future use.

Table 10 - Disturbance record extraction registers

The Disturbance Record status register reports one of these values:

State		Description
Idle		This is the state reported when no record is selected; such as after power-on or after a record has been marked as extracted.
Busy		The product is currently processing data.
Page ready		The data page has been populated and the master can now safely read the data.
Configuration complete		All of the configuration data has been read without error.
Record complete	4	All of the disturbance data has been extracted.
Disturbance overwritten	5	An error occurred during the extraction process where the disturbance being extracted was overwritten by a new record.
No unextracted disturbances	6	An attempt was made by the master station to automatically select the next oldest unextracted disturbance when all records have been extracted.
Not a valid disturbance	7	An attempt was made by the master station to manually select a record that did not exist in the product.

State		Description
Command out of sequence	8	The master station issued a command to the product that was not expected during the extraction process.

Table 11 - Disturbance record status register (3x934) values

4.12.2 Extraction Procedure

The following procedure must be used to extract disturbance records from the product. The procedure is split into four sections:

1. Selection of a disturbance, either manually or automatically.
2. Extraction of the configuration file.
3. Extraction of the data file.
4. Accepting the extracted record (automatic extraction only).

4.12.2.1 Manual Extraction Procedure

The procedure used to extract a disturbance manually is shown in Figure 7. The manual method of extraction does not allow for the acceptance of disturbance records.

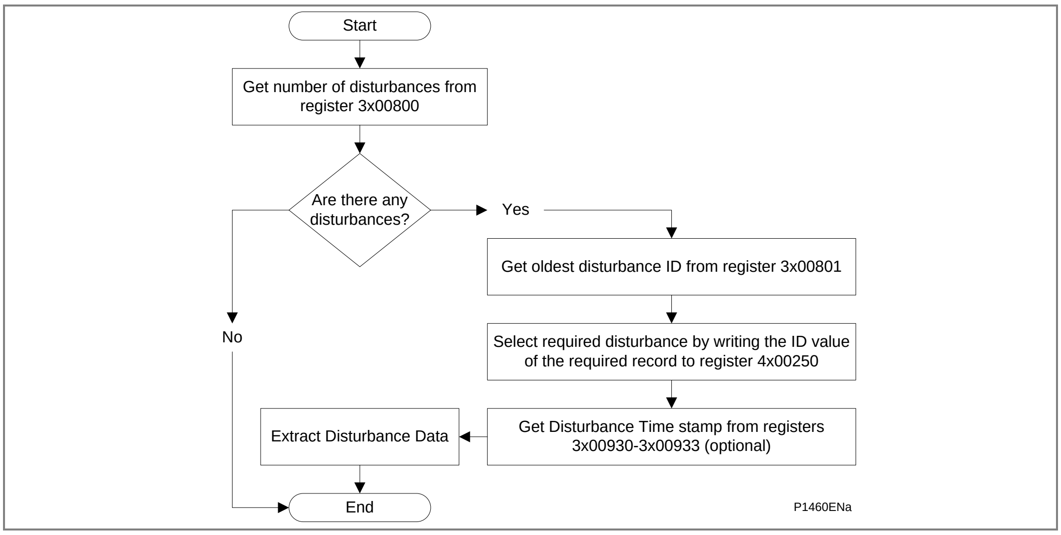

Start
Get number of disturbances from register 3x00800
Are there any disturbances?
Yes
No
Get oldest disturbance ID from register 3x00801
Select required disturbance by writing the ID value of the required record to register 4x00250
Get Disturbance Time stamp from registers 3x00930-3x00933 (optional)
Extract Disturbance Data
End
P1460ENa

Figure 7 - Manual selection of a disturbance record

4.12.2.2 Automatic Extraction Procedure - Option 1

There are two methods that can be used for automatically extracting disturbances. The procedure for the first method is shown in Figure 8. This also shows the acceptance of the disturbance record once the extraction is complete.

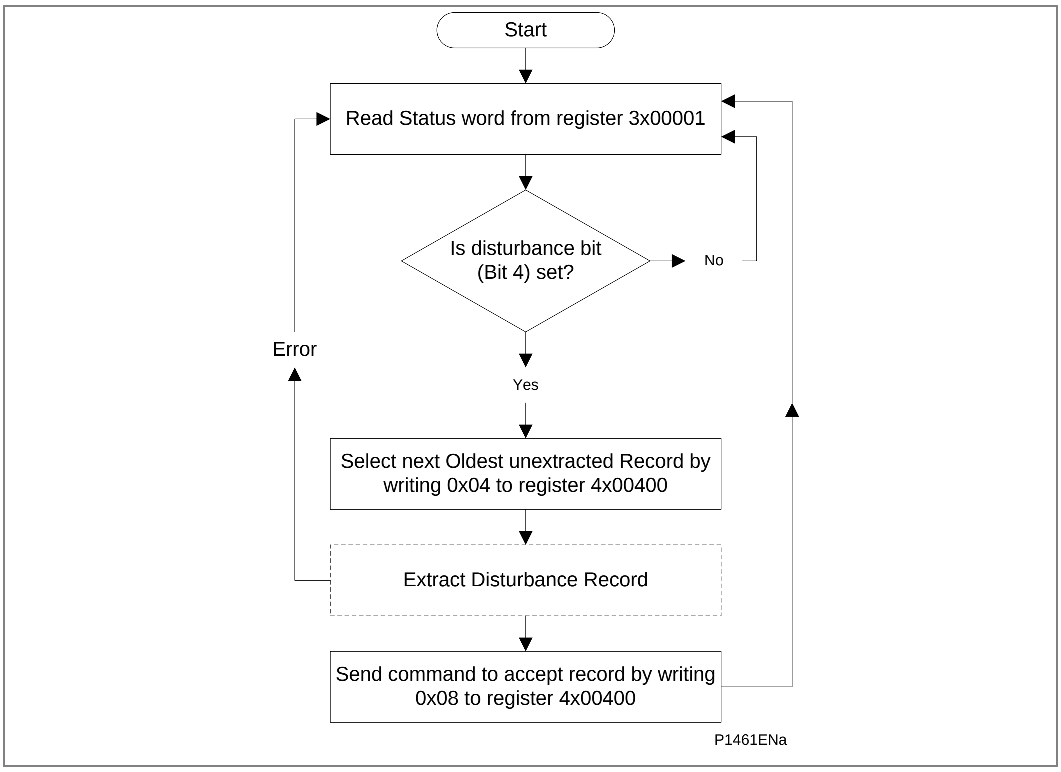

Start
Read Status word from register 3x00001
Is disturbance bit (Bit 4) set?
No
Yes
Error
Select next Oldest unextracted Record by writing 0x04 to register 4x00400
Extract Disturbance Record
Send command to accept record by writing 0x08 to register 4x00400
P1461ENa

Figure 8 - Automatic selection of a disturbance - option 1

4.12.2.3 Automatic Extraction Procedure - Option 2

The second method that can be used for automatic extraction is shown in Figure 9. This also shows the acceptance of the disturbance record once the extraction is complete.

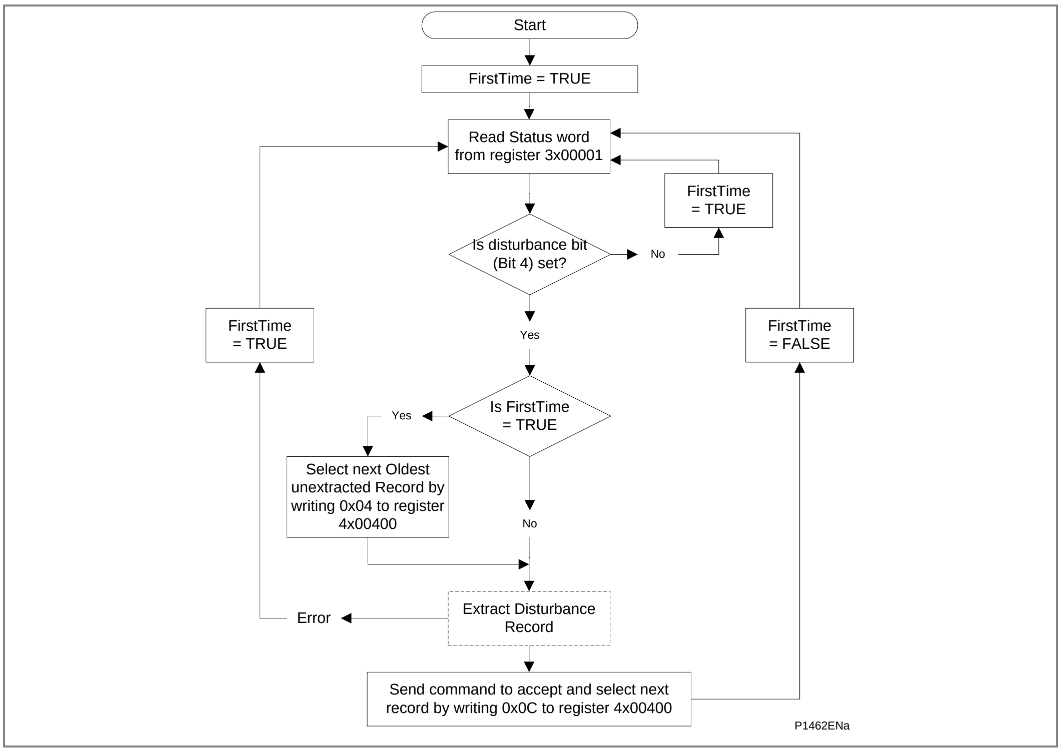

Start
FirstTime = TRUE
Read Status word from register 3x00001
FirstTime = TRUE
Is disturbance bit (Bit 4) set?
No
Yes
FirstTime = TRUE
FirstTime = FALSE
Is FirstTime = TRUE
Yes
Select next Oldest unextracted Record by writing 0x04 to register 4x00400
No
Error
Extract Disturbance Record
Send command to accept and select next record by writing 0x0C to register 4x00400
P1462ENa

Figure 9 - Automatic selection of a disturbance - option 2

4.12.2.4 Extracting the Disturbance Data

Extraction of a selected disturbance record is a two-stage process. This involves first reading the configuration file, then the data file. Figure 10 shows how the configuration file is read and Figure 11 shows how the data file is extracted.

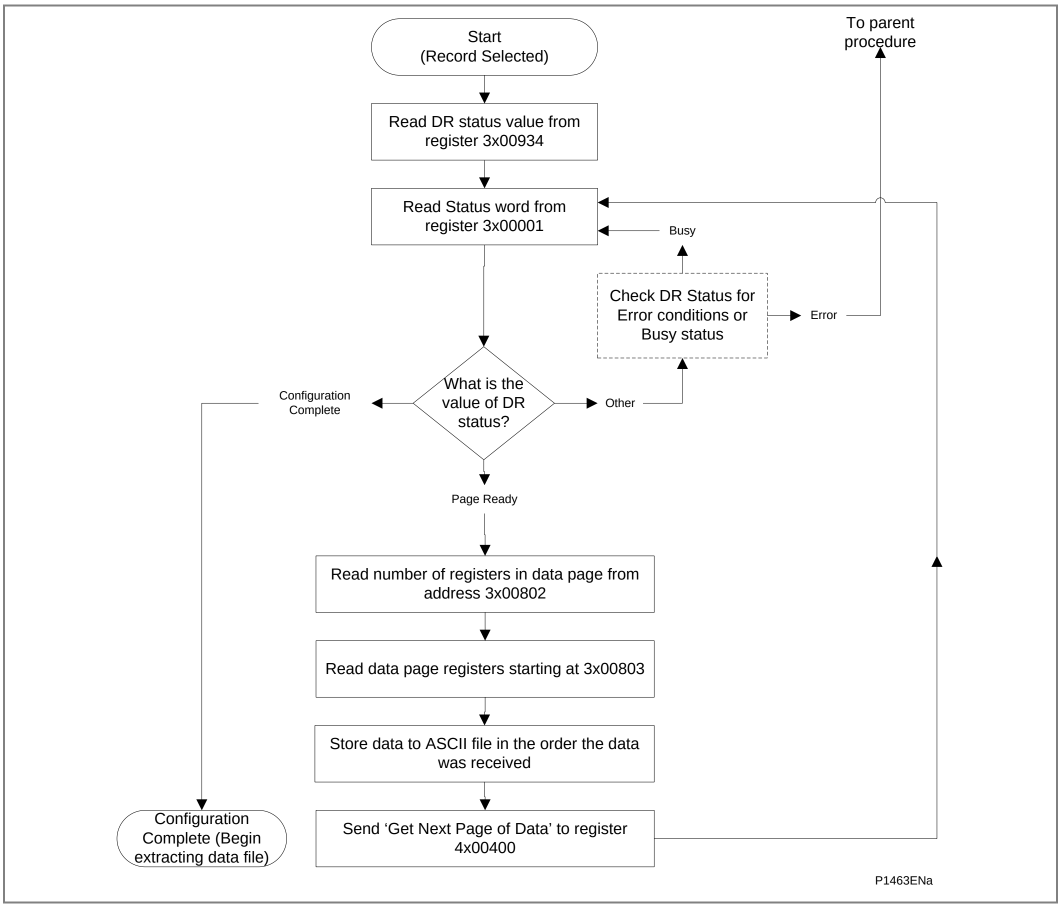

Start
(Record Selected)
To parent procedure
Read DR status value from register 3x00934
Read Status word from register 3x00001
Busy
Check DR Status for Error conditions or Busy status
Error
Configuration Complete
What is the value of DR status?
Other
Page Ready
Read number of registers in data page from address 3x00802
Read data page registers starting at 3x00803
Store data to ASCII file in the order the data was received
Configuration Complete (Begin extracting data file)
Send ‘Get Next Page of Data’ to register 4x00400
P1463ENa

Figure 10 - Extracting the COMTRADE configuration file

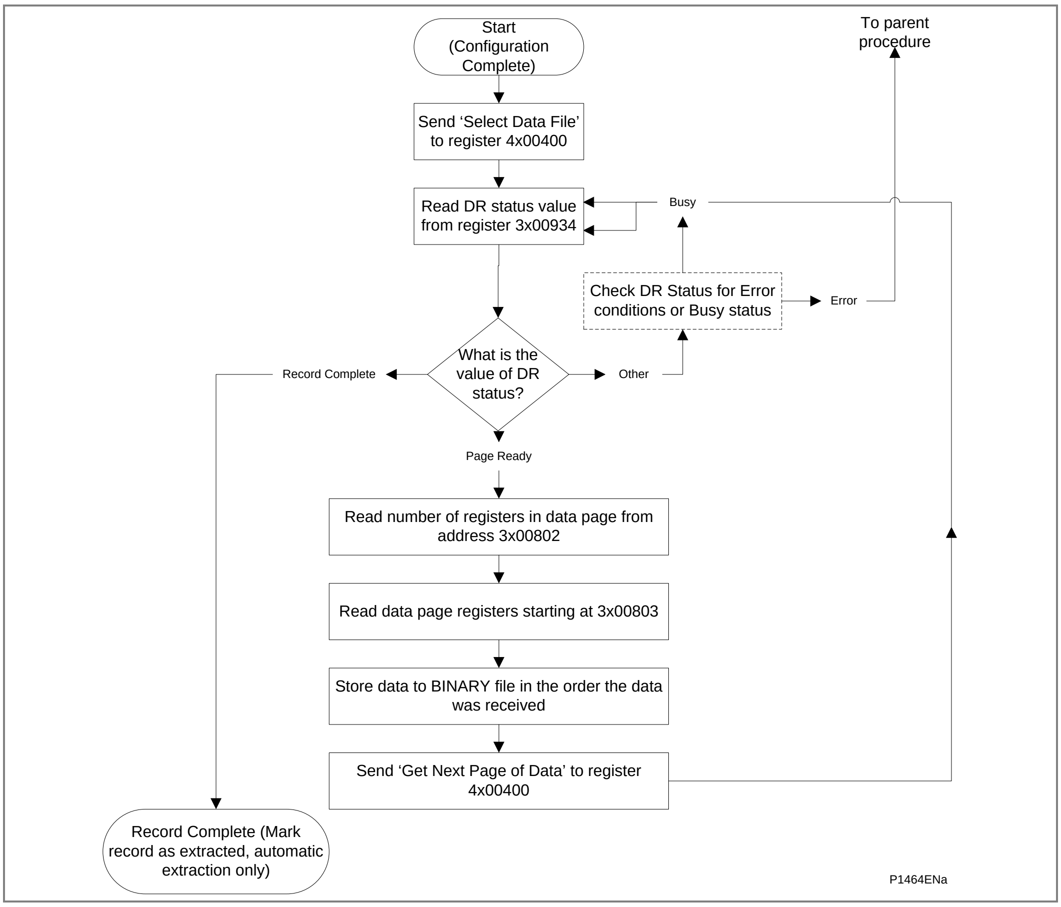

Start (Configuration Complete)
To parent procedure
Send 'Select Data File' to register 4x00400
Read DR status value from register 3x00934
Busy
Check DR Status for Error conditions or Busy status
Error
What is the value of DR status?
Record Complete
Other
Page Ready
Read number of registers in data page from address 3x00802
Read data page registers starting at 3x00803
Store data to BINARY file in the order the data was received
Send 'Get Next Page of Data' to register 4x00400
Record Complete (Mark record as extracted, automatic extraction only)
P1464ENa

Figure 11 - Extracting the COMTRADE binary data file

During the extraction of a COMTRADE file, an error may occur that is reported in the disturbance record status register, 3x934. This can be caused by the product overwriting the record that is being extracted. It can also be caused by the master issuing a command that is not in the bounds of the extraction procedure.

4.12.3 Storage of Extracted Data

The extracted data needs to be written to two separate files. The first is the configuration file, which is in ASCII text format, and the second is the data file, which is in a binary format.

4.12.3.1 Storing the Configuration File

As the configuration data is extracted from the product, it should be stored to an ASCII text file with a '.cfg' file extension. Each register in the page is a G1 format 16-bit unsigned integer that is transmitted in big-endian byte order. The master must write the configuration file page-data to the file in ascending register order with each register's high order byte written before its low order byte, until all the pages have been processed.

4.12.3.2 Storing the Binary Data File

As the binary data is extracted from the product, it should be stored to a binary file with the same name as the configuration file, but with a '.dat' file extension instead of the '.cfg' extension. Each register in the page is a G1-format 16-bit unsigned integer that is transmitted in big-endian byte order. The master must write the page data to a file in ascending register order with each register's high order byte written before its low order byte until all the pages have been processed.

4.12.4 Disturbance Record Deletion

All of the disturbance records stored in the product can be deleted (“cleared”) by writing 5 to the record control register 4x401 (G6 data type). See *section 4.11.4* for details on event record deletion.

4.13 Setting Changes

The product settings can be split into two categories:

- Control and support settings
- Disturbance record settings and protection setting groups

Changes to settings in the control and support area are executed immediately. Changes to the protection setting groups or the disturbance recorder settings are stored in a temporary ‘scratchpad’ area and must be confirmed before they are implemented. All the product settings are 4x page registers; see the *Relay Menu Database document, P64x/EN MD*. The following points should be noted when changing settings:

- Settings implemented using multiple registers must be written to using a multi-register write operation. The product does not support write access to sub-parts of multi-register data types.
- The first address for a multi-register write must be a valid address. If there are unmapped addresses in the range that is written to, the data associated with these addresses are discarded.
- If a write operation is performed with values that are out of range, an “illegal data” response code is produced. Valid setting values in the same write operation are executed.
- If a write operation is performed attempting to change registers that require a higher level of password access than is currently enabled, all setting changes in the write operation are discarded.

4.13.1 Password Protection

The product’s settings can be subject to Password protection. The level of password protection required to change a setting is indicated in the 4x register-map table in the *Relay Menu Database document, P64x/EN MD*. Level 2 is the highest level of password access, level 0 indicates that no password is required.

The following registers are available to control Password protection:

4x00001 & 4x00002	Password Entry
4x00022	Default Password Level
4x00023 & 4x00024	Setting to Change Password Level 1
4x00025 & 4x00026	Setting to Change Password Level 2
3x00010	Current Access Level (read only)

4.13.2 Control and Support Settings

Control and support settings are committed immediately when a value is written to such a register. The MODBUS registers in this category are:

- 4x00000-4x00599
- 4x00700-4x00999
- 4x02049 to 4x02052

- 4x10000-4x10999

4.13.2.1 Time Synchronization

The value of the product’s real time clock can be set by writing the desired time (see section 4.16) to registers 4x02049 through 4x02052. These registers are standard to Schneider Electric MiCOM products, which makes it easier to broadcast a time synchronization packet, being a block write to the time setting registers sent to slave address zero.

When the product’s time has been set using these registers, the Time Synchronized flag in the MODBUS Status Register (3x1: type G26) is set. The product automatically clears this flag if more than five minutes has elapsed since these registers were last written to.

A “Time synchronization” event is logged if the new time value is more than two seconds different to the current value.

4.13.3 Disturbance Recorder Configuration Settings

Disturbance recorder configuration-settings are written to a scratchpad memory area. A confirmation procedure is required to commit the contents of the scratchpad to the disturbance recorder's set-up, which ensures that the recorders configuration is consistent at all times. The contents of the scratchpad memory can be discarded with the abort procedure. The scratchpad confirmation and abort procedures are described in *section 4.13.5*.

The disturbance recorder configuration registers are in the range:

- 4x00600-4x00699

4.13.4 Protection Settings

Protection configuration-settings are written to a scratchpad memory area. A confirmation procedure is required to commit the contents of the scratchpad to the product’s protection functions, which ensures that their configuration is consistent at all times. The contents of the scratchpad memory can be discarded with the abort procedure. The scratchpad confirmation and abort procedures are described in *section 4.13.5*.

The product supports four groups of protection settings. One protection-group is active and the other three are either dormant or disabled. The active protection-group can be selected by writing to register 4x00404. An illegal data response is returned if an attempt is made to set the active group to one that has been disabled.

The MODBUS registers for each of the four groups are repeated in the following ranges:

Group 1	4x01000-4x02999, (see note) 4x11000-4x12999
Group 2	4x03000-4x04999, 4x13000-4x14999
Group 3	4x05000-4x06999, 4x15000-4x16999
Group 4	4x07000-4x08999, 4x17000-4x18999

Note *Registers 4x02049 to 4x02052 are not part of protection setting group #1 so they do not repeat nin any of the other protection setting groups. These registers are for time synchronization purposes and are standard for most Schneider Electric products. See section 4.13.2.1.*

4.13.5 Scratchpad Management

Register 4x00405 can be used to either confirm or abort the setting changes in the scratchpad area. In addition to the basic editing of the protection setting groups, these functions are provided:

- Default values can be restored to a setting group or to all of the product settings by writing to register 4x00402.
- It is possible to copy the contents of one setting group to another by writing the source group to register 4x00406 and the target group to 4x00407.
- The setting changes performed by either of these two operations are made to the scratchpad area. These changes must be confirmed by writing to register 4x00405.

4.14 Register Data Types

The product maps one or more MODBUS registers to data-typed information contained in an internal database. These data-types are referred to as G-Types since they have a 'G' prefixed identifier. The *Relay Menu Database document, P64x/EN MD* gives a complete definition of the all of the G-Types used in the product.

Generally the data types are transmitted in high byte to low byte order, also known as "Big Endian format". This may require the MODBUS master to reorder the received bytes into a format that complies with its byte order and register order (for multi-register G-Types) conventions. Most MODBUS masters provide byte-swap and register-swap device (or data point) configuration to cope with the wide range of implementations.

The product's data types cannot be broken into smaller parts. Therefore multi-register data types cannot be read from or written to on an individual register basis. All of the registers for a multi-register data-typed item must be read from or written to with a single block read or write command. The following subsections provide some additional notes for a few of the more complex G-Types.

4.15 Numeric Setting (Data Types G2 & G35)

Numeric settings are integer representations of real (non-integer) values. The register value is the number of setting increments (or steps) that the real value is away from the real minimum value. This is expressed by this formula:

$S_{real} = S_{min.} + (S_{inc.} \times S_{numeric})$

Where:

S_{real}	Setting real value
$S_{min.}$	Setting real minimum value
$S_{inc.}$	Setting real increment (step) value
$S_{numeric}$	Setting numeric (register) value

For example, a setting with a real value setting range of 0.01 to 10 in steps of 0.01 would have the following numeric setting values:

Real value (S_{real})	Numeric value ($S_{numeric}$)
0.01	0
0.02	1
1.00	99

Table 12 - Real and numeric values

The G2 numeric data type uses 1 register as an unsigned 16-bit integer, whereas the G35 numeric data type uses 2 registers as an unsigned 32-bit integer. The G2 data type therefore provides a maximum setting range of 2^{16} x S_{inc}. Similarly the G35 data type provides a maximum setting range of 2^{32} x S_{inc}.

4.16 Date and Time Format (Data Type G12)

The date-time data type G12 allows real date and time information to be conveyed down to a resolution of 1 ms. The data-type is used for record time-stamps and for time synchronization (see section 4.13.2.1).

The structure of the data type is shown in Table 13 and complies with the IEC60870-5-4 Binary Time 2a format.

Byte	**Bit Position**							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
1	m^7	m^6	m^5	m^4	m^3	m^2	m^1	m^0
2	m^{15}	m^{14}	m^{13}	m^{12}	m^{11}	m^{10}	m^9	m^8
3	IV	R	I^5	I^4	I^3	I^2	I^1	I^0
4	SU	R	R	H^4	H^3	H^2	H^1	H^0
5	W^2	W^1	W^0	D^4	D^3	D^2	D^1	D^0
6	R	R	R	R	M^3	M^2	M^1	M^0
7	R	Y^6	Y^5	Y^4	Y^3	Y^2	Y^1	Y^0

Where:
m = 0…59,999ms
I = 0…59 minutes
H = 0…23 Hours
W = 1…7 Day of week; Monday to Sunday, 0 for not calculated
D = 1…31 Day of Month
M = 1…12 Month of year; January to December
Y = 0…99 Years (year of century)
R = Reserved bit = 0
SU = Summertime: 0=standard time, 1=summer time
IV = Invalid value: 0=valid, 1=invalid
range = 0ms…99 years

Table 13 - G12 date & time data type structure

The seven bytes of the structure are packed into four 16-bit registers. Two packing formats are provided: standard and reverse. The prevailing format is selected by the G238 setting in the **Date and Time** menu column or by register 4x306 (Modbus IEC Time).

The standard packing format is the default and complies with the IEC60870-5-4 requirement that byte 1 is transmitted first. This is followed by byte 2 through to byte 7, followed by a null (zero) byte to make eight bytes in total. Since register data is usually transmitted in big-endian format (high-order byte followed by low-order byte), byte 1 is in the high-order byte position followed by byte 2 in the low-order position for the first register. The last register contains just byte 7 in the high-order position and the low-order byte has a value of zero.

The reverse packing format is the exact byte transmission order reverse of the standard format. The null (zero) byte is sent as the high-order byte of the first register and byte 7 as the register's low-order byte. The second register's high-order byte contains byte 6 and byte 5 in its low order byte.

Both packing formats are fully documented in the *Relay Menu Database document, P64x/EN MD* for the G12 type.

The principal application of the reverse format is for date-time packet format consistency when a mixture of MiCOM Px20, Px30, and Px40 series products are being used. This is especially true when there is a requirement for broadcast time synchronization with a mixture of such MiCOM products.

The data type provides only the value for the year of the century. The century must be deduced. The century could be imposed as 20 for applications not dealing with dates stored in this format from the previous (20th) century. Alternatively, the century can be calculated as the one that produces the nearest time value to the current date. For example: 30-12-99 is 30-12-1999 when received in 1999 & 2000, but is 30-12-2099 when received in 2050. This technique allows 2-digit years to be accurately converted to 4 digits in a ±50 year window around the current datum.

The invalid bit has two applications:

- It can indicate that the date-time information is considered inaccurate, but is the best information available.
- Date-time information is not available.

The summertime bit is used to indicate that summertime (day light saving) is being used and, more importantly, to resolve the alias and time discontinuity which occurs when summertime starts and ends. This is important for the correct time correlation of time stamped records. The value of the summertime bit does not affect the time displayed by the product.

The day of the week field is optional and if not calculated is set to zero.

This data type (and therefore the product) does not cater for time zones so the end user must determine the time zone used by the product. UTC (universal co-ordinated time) is commonly used and avoids the complications of daylight saving timestamps.

Power and energy measurement data formats (G29 & G125)

The power and energy measurements are available in two data formats, G29 integer format and G125 IEEE754 floating point format. The G125 format is preferred over the older G29 format.

4.16.1 Data Type G29

Data type G29 consists of three registers. The first register is the per-unit power or energy measurement and is of type G28, which is a signed 16-bit quantity. The second and third registers contain a multiplier to convert the per-unit value to a real value.

The multiplier is of type G27, which is an unsigned 32-bit quantity. Therefore the overall value conveyed by the G29 data type must be calculated as G29 = G28 × G27.

The product calculates the G28 per unit power or energy value as

G28 = ((measured secondary quantity) / (CT secondary) × (110 V / (VT secondary)).

Since data type G28 is a signed 16-bit integer, its dynamic range is constrained to ±32768. This limitation should be borne in mind for the energy measurements, as the G29 value saturates a long time before the equivalent G125.

The associated G27 multiplier is calculated as

G27 = (CT primary) × (VT primary / 110 V)
when primary value measurements are selected,
and as
G27 = (CT secondary) × (VT secondary / 110 V)
when secondary value measurements are selected.

Due to the required truncations from floating point values to integer values in the calculations of the G29 component parts and its limited dynamic range, the use of the G29 values is only recommended when the MODBUS master cannot deal with the G125 IEEE754 floating point equivalents.

Note *The G29 values must be read in whole multiples of three registers. It is not possible to read the G28 and G27 parts with separate read commands.*

Example:

For A-Phase Power (Watts) (registers 3x00300 - 3x00302) for a 110 V nominal, In = 1 A, VT ratio = 110 V:110 V and CT ratio = 1 A : 1 A.

Applying A-phase 1A @ 63.51V

A-phase Watts = ((63.51 V × 1 A) / In=1 A) × (110/Vn=110 V) = 63.51 Watts

The G28 part of the value is the truncated per unit quantity, which is equal to 64 (40h).

The multiplier is derived from the VT and CT ratios set in the product, with the equation ((CT Primary) × (VT Primary) / 110 V)). Therefore the G27 part of the value equals 1 and the overall value of the G29 register set is 64×1 = 64 W.

The registers would contain:

3x00300 - 0040h
3x00301 - 0000h
3x00302 - 0001h

Using the previous example with a VT ratio = 110,000 V:110 V and CT ratio = 10,000 A : 1 A the G27 multiplier would be 10,000 A × 110,000 V / 110 = 10,000,000. The overall value of the G29 register set is 64 × 10,000,000 = 640 MW. (Note that there is an actual error of 49 MW in this calculation due to loss of resolution).

The registers would contain:

3x00300 - 0040h
3x00301 - 0098h
3x00302 - 9680h

4.16.2 Data Type G125

Data type G125 is a short float IEEE754 floating point format, which occupies 32 bits in two consecutive registers. The most significant 16 bits of the format are in the first (low order) register and the least significant 16 bits in the second register.

The value of the G125 measurement is as accurate as the product's ability to resolve the measurement after it has applied the secondary or primary scaling factors as required. It does not suffer from the truncation errors or dynamic range limitations associated with the G29 data format.

5 IEC60870-5-103 INTERFACE

The IEC60870-5-103 interface is a master/slave interface with the relay as the slave device. The relay conforms to compatibility level 2; compatibility level 3 is not supported.

These IEC60870-5-103 facilities are supported by this interface:

- Initialization (Reset)
- Time Synchronization
- Event Record Extraction
- General Interrogation
- Cyclic Measurements
- General Commands
- Disturbance Record Extraction
- Private Codes

5.1 Physical Connection and Link Layer

Two connection options are available for IEC60870-5-103, either the rear EIA(RS)-485 port or an optional rear fiber optic port. If the fiber optic port is fitted, the active port can be selected using the front panel menu or the front Courier port. However the selection is only effective following the next relay power up.

For either of the two connection modes, both the relay address and baud rate can be selected using the front panel menu or the front Courier port. Following a change to either of these two settings a reset command is required to re-establish communications, see the description of the reset command in *section 5.2 Initialization*.

5.2 Initialization

Whenever the relay has been powered up, or if the communication parameters have been changed, a reset command is required to initialize the communications. The relay responds to either of the two reset commands (Reset CU or Reset FCB). However, the Reset CU clears any unsent messages in the relay’s transmit buffer.

The relay responds to the reset command with an identification message ASDU 5. The Cause Of Transmission (COT) of this response is either Reset CU or Reset FCB depending on the nature of the reset command. For information on the content of ASDU 5 see *section IEC60870-5-103 in the Relay Menu Database document, P64x/EN MD*.

In addition to the ASDU 5 identification message, if the relay has been powered up it also produces a power-up event.

5.3 Time Synchronization

The relay time and date can be set using the time synchronization feature of the IEC60870-5-103 protocol. The relay corrects for the transmission delay as specified in IEC60870-5-103. If the time synchronization message is sent as a send / confirm message, the relay responds with a confirm. Whether the time-synchronization message is sent as a send / confirm or a broadcast (send / no reply) message, a time synchronization Class 1 event is generated.

If the relay clock is synchronised using the IRIG-B input, it is not possible to set the relay time using the IEC60870-5-103 interface. If the time is set using the interface, the relay creates an event using the current date and time from the internal clock, which is synchronised to IRIG-B.

5.4 Spontaneous Events

Events are categorized using the following information:

- Function Type
- Information Number

The IEC60870-5-103 profile in the *Relay Menu Database document, P64x/EN MD*, contains a complete listing of all events produced by the relay.

5.5 General Interrogation

The GI request can be used to read the status of the relay, the function numbers, and information numbers that are returned during the GI cycle. See the IEC60870-5-103 profile in the *Relay Menu Database document, P64x/EN MD*.

5.6 Cyclic Measurements

The relay produces measured values using ASDU 9 cyclically. This can be read from the relay using a Class 2 poll (note ADSU 3 is not used). The rate at which the relay produces new measured values can be controlled using the Measurement Period setting. This setting can be edited from the front panel menu or the front Courier port and is active immediately following a change.

The measurands transmitted by the relay are sent as a proportion of 2.4 times the rated value of the analog value.

5.7 Commands

A list of the supported commands is contained in the *Relay Menu Database document, P64x/EN MD*. The relay responds to other commands with an ASDU 1, with a Cause of Transmission (COT) indicating ‘negative acknowledgement’.

5.8 Test Mode

Using either the front panel menu or the front Courier port, it is possible to disable the relay output contacts to allow secondary injection testing to be performed. This is interpreted as ‘test mode’ by the IEC60870-5-103 standard. An event is produced to indicate both entry to and exit from test mode. Spontaneous events and cyclic measured data transmitted while the relay is in test mode has a COT of ‘test mode’.

5.9 Disturbance Records

The disturbance records are stored in uncompressed format and can be extracted using the standard mechanisms described in IEC60870-5-103. Note IEC60870-5-103 only supports up to 8 records.

5.10 Blocking of Monitor Direction

The relay supports a facility to block messages in the Monitor direction and in the Command direction. Messages can be blocked in the Monitor and Command directions using the menu commands, Communications - CS103 Blocking -
Disabled / Monitor Blocking / Command Blocking or DDB signals Monitor Blocked and Command Blocked.

6 DNP3.0 INTERFACE

6.1 DNP3.0 Protocol

The DNP3.0 protocol is defined and administered by the DNP Users Group. For information on the user group, DNP3.0 in general and the protocol specifications, see www.dnp.org

The descriptions given here are intended to accompany the device profile document that is included in the *Relay Menu Database document, P64x/EN MD.* The DNP3.0 protocol is not described here, please refer to the documentation available from the user group. The device profile document specifies the full details of the DNP3.0 implementation for the relay. This is the standard format DNP3.0 document that specifies which objects; variations and qualifiers are supported. The device profile document also specifies what data is available from the relay using DNP3.0. The relay operates as a DNP3.0 slave and supports subset level 2 of the protocol, plus some of the features from level 3.

DNP3.0 communication uses the EIA(RS)-485 communication port at the rear of the relay. The data format is 1 start bit, 8 data bits, an optional parity bit and 1 stop bit. Parity is configurable (see menu settings below).

6.2 DNP3.0 Menu Setting

The following settings are in the DNP3.0 menu in the **Communications** column.

Setting	Range	Description
Remote Address	0 - 65534	DNP3.0 address of relay (decimal)
Baud Rate	1200, 2400, 4800, 9600, 19200, 38400	Selectable baud rate for DNP3.0 communication
Parity	None, Odd, Even	Parity setting
RP1 Physical Link	Copper or Fiber Optic	This cell defines whether an electrical EIA(RS)485 or fiber optic connection is being used for communication between the master station and relay. If **Fiber Optic** is selected, the optional fiber optic communications board is required.
Time Sync.	Enabled, Disabled	Enables or disables the relay requesting time sync. from the master using IIN bit 4 word 1
Meas Scaling	Primary, Secondary or Normalized	Setting to report analog values in terms of primary, secondary or normalized (with respect to the CT/VT ratio setting) values.
Message Gap	0 - 50 msec	Setting to allow the master station to have an interframe gap.
DNP Need Time	1 - 30 mins	The length of time waited before requesting another time sync from the master.
DNP App Fragment	1 - 2048 bytes	The maximum message length (application fragment size) transmitted by the relay.
DNP App Timeout	1 -120 s	The length of time waited after sending a message fragment and waiting for a confirmation from the master.
DNP SBO Timeout	1 - 10 s	The length of time waited after receiving a select command and waiting for an operate confirmation from the master.

Setting	Range	Description
DNP Link Timeout	0 - 120 s	The length of time the relay waits for a Data Link Confirm from the master. A value of 0 means data link support disabled and 1 to 120 seconds is the timeout setting.

Table 14 - DNP3.0 menu in the Communications column

If the DNP3.0 over Ethernet option is selected, further settings are presented, as shown in this table.

Setting	Range	Description
DNP Time Sync.	Disabled or Enabled	If set to Enabled the DNP3.0 master station can be used to synchronize the time on the relay. If set to Disabled, either the internal free running clock or the IRIG-B input are used.
Meas Scaling	Primary, Secondary or Normalized	Setting to report analog values in terms of primary, secondary or normalized values, with respect to the CT/VT ratio setting.
NIC Tunl Timeout	1 - 30 mins	Time waited before an inactive tunnel to a master station is reset.
NIC Link Report	Alarm, Event or None	Configures how a failed or unfitted network link (copper or fiber) is reported: Alarm - an alarm is raised for a failed link Event - an event is raised for a failed link None - nothing reported for a failed link
NIC Link Timeout	0.1 - 60 s	Time waited, after failed network link is detected, before communication by the alternative media interface is attempted.

Table 15 - DNP3.0 over Ethernet option settings

6.3 Object 1 Binary Inputs

Object 1, binary inputs, contains information describing the state of signals in the relay, which mostly form part of the digital data bus (DDB). In general these include the state of the output contacts and input optos, alarm signals and protection start and trip signals. The ‘DDB number’ column in the device profile document provides the DDB numbers for the DNP3.0 point data. These can be used to cross-reference to the DDB definition list. See the *Relay Menu Database document, P64x/EN MD*. The binary input points can also be read as change events using object 2 and object 60 for class 1-3 event data.

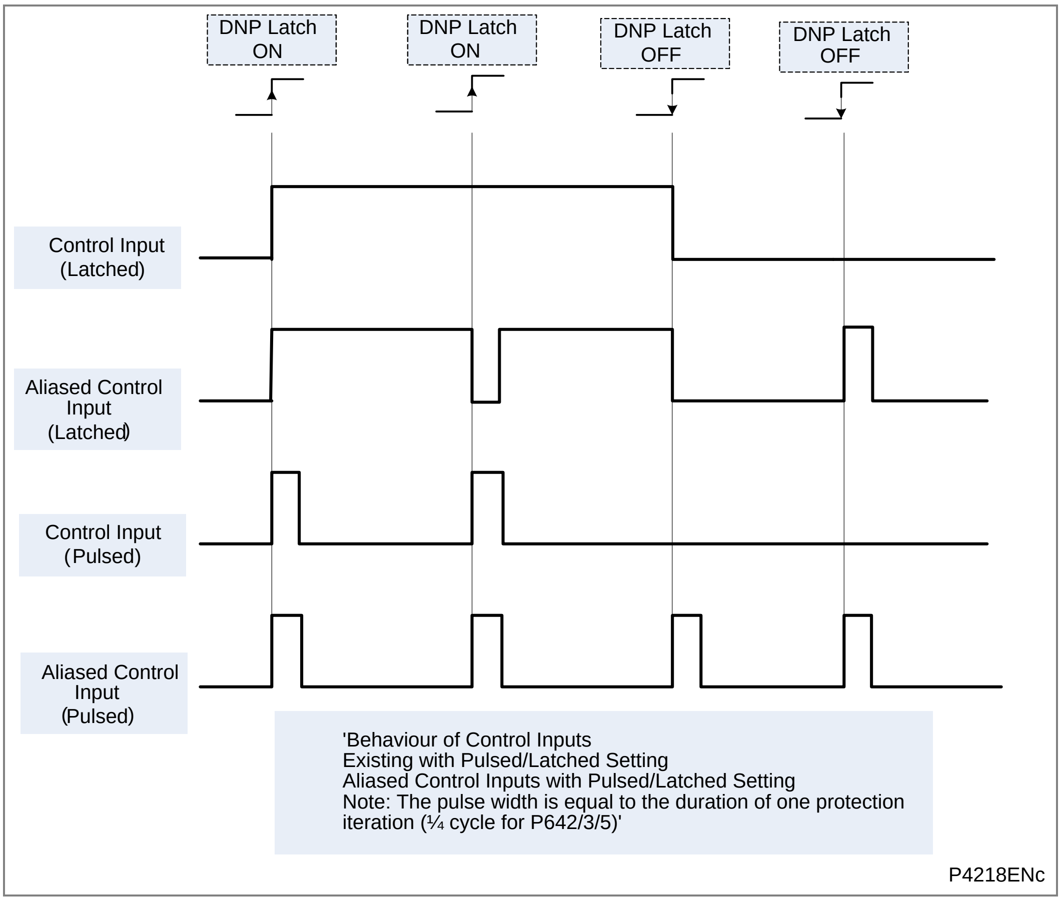
6.4 Object 10 Binary Outputs

Object 10, binary outputs, contains commands that can be operated using DNP3.0. Therefore the points accept commands of type pulse on [null, trip, close] and latch on/off as detailed in the device profile in the *Relay Menu Database document, P64x/EN MD* and execute the command once for either command. The other fields are ignored (queue, clear, trip/close, in time and off time).

There is an additional image of the control inputs. Described as alias control inputs, they reflect the state of the control input, but with a dynamic nature.

- If the Control Input DDB signal is already SET and a new DNP SET command is sent to the Control Input, the Control Input DDB signal goes momentarily to RESET and then back to SET.

- If the Control Input DDB signal is already RESET and a new DNP RESET command is sent to the Control Input, the Control Input DDB signal goes momentarily to SET and then back to RESET.



'Behaviour of Control Inputs
Existing with Pulsed/Latched Setting
Aliased Control Inputs with Pulsed/Latched Setting
Note: The pulse width is equal to the duration of one protection iteration (¼ cycle for P642/3/5)'

Figure 12 - Behavior when control input is set to pulsed or latched

Many of the relay's functions are configurable so some of the object 10 commands described in the following sections may not be available. A read from object 10 reports the point as off-line and an operate command to object 12 generates an error response.

Examples of object 10 points that maybe reported as off-line are:

• Activate setting groups	Ensure setting groups are enabled
• CB trip/close	Ensure remote CB control is enabled
• Reset NPS thermal	Ensure NPS thermal protection is enabled
• Reset thermal O/L	Ensure thermal overload protection is enabled
• Reset RTD flags	Ensure RTD Inputs is enabled
• Control inputs	Ensure control inputs are enabled

6.5 Object 20 Binary Counters

Object 20, binary counters, contains cumulative counters and measurements. The binary counters can be read as their present 'running' value from object 20, or as a 'frozen' value from object 21. The running counters of object 20 accept the read, freeze and clear functions. The freeze function takes the current value of the object 20 running counter and stores it in the corresponding object 21 frozen counter. The freeze and clear function resets the object 20 running counter to zero after freezing its value.

Binary counter and frozen counter change event values are available for reporting from object 22 and object 23 respectively. Counter change events (object 22) only report the most recent change, so the maximum number of events supported is the same as the total number of counters. Frozen counter change events (object 23) are generated whenever a freeze operation is performed and a change has occurred since the previous freeze command. The frozen counter event queues store the points for up to two freeze operations.

6.6 Object 30 Analog Input

Object 30, analog inputs, contains information from the relay’s measurements columns in the menu. All object 30 points can be reported as 16 or 32-bit integer values with flag, 16 or 32-bit integer values without flag, as well as short floating point values.

Analogue values can be reported to the master station as primary, secondary or normalized values (which takes into account the relay’s CT and VT ratios) and this is settable in the DNP3.0 Communications Column in the relay. Corresponding deadband settings can be displayed in terms of a primary, secondary or normalized value. Deadband point values can be reported and written using Object 34 variations.

The deadband is the setting used to determine whether a change event should be generated for each point. The change events can be read using object 32 or object 60. These events are generated for any point which has a value changed by more than the deadband setting since the last time the data value was reported.

Any analog measurement that is unavailable when it is read is reported as offline. For example, the frequency when the current and voltage frequency is outside the tracking range of the relay or the thermal state when the thermal protection is disabled in the configuration column. All object 30 points are reported as secondary values in DNP3.0 (with respect to CT and VT ratios).

6.7 Object 40 Analog Output

The conversion to fixed-point format requires the use of a scaling factor, which is configurable for the various types of data within the relay such as current, voltage, and phase angle. All Object 40 points report the integer scaling values and Object 41 is available to configure integer scaling quantities.

6.8 DNP3.0 Configuration using MiCOM S1 Studio

A PC support package for DNP3.0 is available as part of MiCOM S1 Studio to allow configuration of the relay’s DNP3.0 response. The PC is connected to the relay using a serial cable to the 9-pin connector on the front of the relay, see *chapter P64x/EN IT*. The configuration data is uploaded from the relay to the PC in a block of compressed format data and downloaded to the relay in a similar manner after modification. The new DNP3.0 configuration takes effect in the relay after the download is complete. To restore the default configuration at any time, from the **Configuration** column, select the **Restore Defaults** cell then select **All Settings**.

In MiCOM S1 Studio, the DNP3.0 data is shown in three main folders, one folder each for the point configuration, integer scaling and default variation (data format). The point configuration also includes screens for binary inputs, binary outputs, counters and analogue input configuration.

7 IEC 61850 ETHERNET INTERFACE

7.1 Introduction

IEC 61850 is the international standard for Ethernet-based communication in substations. It enables integration of all protection, control, measurement and monitoring functions in a substation, and provides the means for interlocking and inter-tripping. It combines the convenience of Ethernet with the security which is essential in substations today.

The MiCOM protection relays can integrate with the PACiS substation control systems, to complete Schneider Electric's offer of a full IEC 61850 solution for the substation. The majority of MiCOM Px3x and Px4x relay types can be supplied with Ethernet, in addition to traditional serial protocols. Relays which have already been delivered with UCA2.0 on Ethernet can be easily upgraded to IEC 61850.

7.2 What is IEC 61850?

IEC 61850 is a 14-part international standard, which defines a communication architecture for substations. It is more than just a protocol and provides:

- Standardized models for IEDs and other equipment in the substation
- Standardized communication services (the methods used to access and exchange data)
- Standardized formats for configuration files
- Peer-to-peer (for example, relay to relay) communication

The standard includes mapping of data onto Ethernet. Using Ethernet in the substation offers many advantages, most significantly including:

- High-speed data rates (currently 100 Mbits/s, rather than tens of kbits/s or less used by most serial protocols)
- Multiple masters (called “clients”)
- Ethernet is an open standard in every-day use

Schneider Electric has been involved in the Working Groups which formed the standard, building on experience gained with UCA2.0, the predecessor of IEC 61850.

7.2.1 Interoperability

A major benefit of IEC 61850 is interoperability. IEC 61850 standardizes the data model of substation IEDs which simplifies integration of different vendors’ products. Data is accessed in the same way in all IEDs, regardless of the vendor, even though the protection algorithms of different vendors’ relays may be different.

IEC 61850-compliant devices are not interchangeable, you cannot replace one device with another. However, the terminology is predefined and anyone with knowledge of IEC 61850 can quickly integrate a new device without mapping all of the new data. IEC 61850 improves substation communications and interoperability at a lower cost to the end user.

7.2.2 Data Model

To ease understanding, the data model of any IEC 61850 IED can be viewed as a hierarchy of information. The categories and naming of this information is standardized in the IEC 61850 specification.

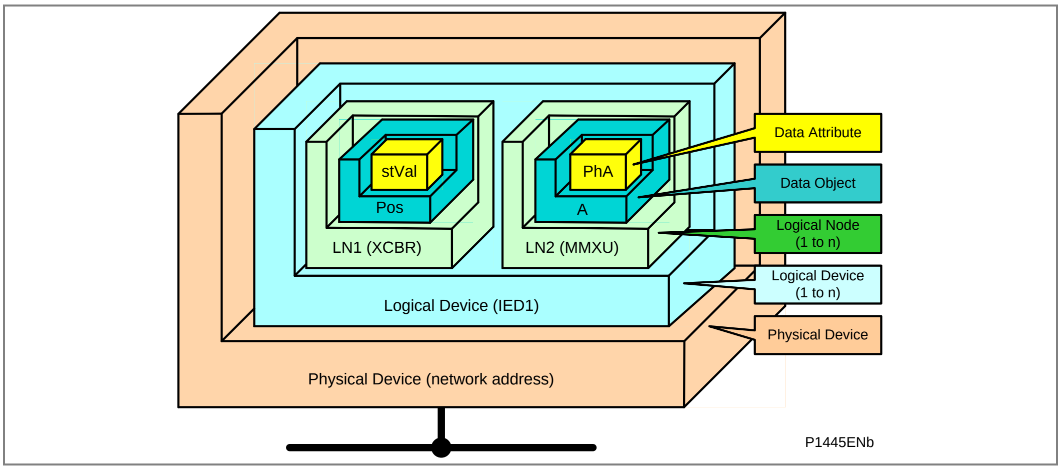

stVal
Pos
LN1 (XCBR)
PhA
A
LN2 (MMXU)
Logical Device (IED1)
Physical Device (network address)
Data Attribute
Data Object
Logical Node (1 to n)
Logical Device (1 to n)
Physical Device
P1445ENb

Figure 13 - Data model layers in IEC 61850

The levels of this hierarchy can be described as follows:

• Physical Device	Identifies the actual IED in a system. Typically the device’s name or IP address can be used (for example **Feeder_1** or **10.0.0.2**).
• Logical Device	Identifies groups of related Logical Nodes inthe Physical Device. For the MiCOM relays, five Logical Devices exist: **Control, Measurements, Protection, Records, System**.
• Wrapper/Logical Node Instance	Identifies the major functional areas in the IEC 61850 data model. Either 3 or 6 characters are used as a prefix to define the functional group (wrapper) while the actual functionality is identified by a 4 character Logical Node name, suffixed by an instance number. For example, XCBR1 (circuit breaker), MMXU1 (measurements), FrqPTOF2 (overfrequency protection, stage 2).
• Data Object	This next layer is used to identify the type of data presented. For example, **Pos** (position) of Logical Node type **XCBR**.
• Data Attribute	This is the actual data (such as measurement value, status, and description). For example, **stVal** (status value) indicates the actual position of the circuit breaker for Data Object type **Pos** of Logical Node type **XCBR**.

7.3 IEC 61850 in MiCOM Relays

IEC 61850 is implemented in MiCOM relays by use of a separate Ethernet card. This card manages the majority of the IEC 61850 implementation and data transfer to avoid any impact on the performance of the protection.

To communicate with an IEC 61850 IED on Ethernet, it is necessary only to know its IP address. This can then be configured into either:

- An IEC 61850 client (or master), for example a PACiS computer (MiCOM C264) or HMI, or
- An MMS browser, with which the full data model can be retrieved from the IED, without any prior knowledge

7.3.1 Capability

The IEC 61850 interface provides these capabilities:

- Read access to measurements

All measurands are presented using the measurement Logical Nodes, in the ‘Measurements’ Logical Device. Reported measurement values are refreshed by the relay once per second, in line with the relay user interface.

- Generation of unbuffered reports on change of status/measurement

Unbuffered reports, when enabled, report any change of state in statuses and measurements (according to deadband settings).

- Support for time synchronization over an Ethernet link

Time synchronization is supported using SNTP (Simple Network Time Protocol). This protocol is used to synchronize the internal real time clock of the relays.

- GOOSE peer-to-peer communication

GOOSE communications of statuses are included as part of the IEC 61850 implementation. See section 7.6 for more details.

- Disturbance record extraction

Disturbance records can be extracted from MiCOM relays by file transfer, as ASCII format COMTRADE files.

- Controls

The following control services are available:

  - Direct Control
  - Direct Control with enhanced security
  - Select Before Operate (SBO) with enhanced security
  - Controls are applied to open and close circuit breakers using XCBR.Pos and DDB signals ‘Control Trip’ and ‘Control Close’.
  - System/LLN0. LLN0.LEDRs are used to reset any trip LED indications.

- Reports

Reports only include data objects that have changed and not the complete dataset. The exceptions to this are a General Interrogation request and integrity reports.

- Buffered Reports

Eight Buffered Report Control Blocks, (BRCB), are provided in SYSTEM/LLN0 in Logical Device ‘System’.

Buffered reports are configurable to use any configurable dataset located in the same Logical device as the BRCB (SYSTEM/LLN0).

- Unbuffered Reports

Sixteen Unbuffered Report Control Blocks (URCB) are provided in SYSTEM/LLN0 in Logical Device ‘System’.

Unbuffered reports are configurable to use any configurable dataset located in the same Logical device as the URCB (SYSTEM/LLN0).

- Configurable Data Sets

It is possible to create and configure datasets in any Logical Node using the IED Configurator. The maximum number of datasets will be specified in an IED’s ICD file. An IED is capable of handling 100 datasets.

- Published GOOSE message

Eight GOCBs are provided in SYSTEM/LLN0.

- Uniqueness of control

The Uniqueness of control mechanism is implemented in the P64x to be consistent with the PACiS mechanism. This requires the relay to subscribe to the OrdRun signal from all devices in the system and be able to publish such a signal in a GOOSE message.

- Select Active Setting Group

Functional protection groups can be enabled or disabled using private mod/beh attributes in the Protection/LLN0.OcpMod object. Setting groups are selectable using the Setting Group Control Block class, (SGCB). The Active Setting Group can be selected using the System/LLN0.SP.SGCB.ActSG data attribute in Logical Device ‘System’.

- Quality for GOOSE

It is possible to process the quality attributes of any Data Object in an incoming GOOSE message. Devices that do not support IEC61850 quality flags send quality attributes as all zeros.

- Address List

An Address List document (to be titled ADL) is produced for each IED which shows the mapping between the IEC61850 data model and the internal data model of the IED. It includes a mapping in the reverse direction, which may be more useful. This document is separate from the PICS/MICS document.

- Originator of Control

Originator of control mechanism is implemented for operate response message and in the data model on the ST of the related control object, consistent with the PACiS mechanism.

- Metering

MMTR (metering) logical node is implemented in P14x. All metered values in the MMTR logical node are of type BCR. The actVal attribute of the BCR class is of type INT128, but this type is not supported by the SISCO MMSLite library. Instead, an INT64 value will be encoded for transmission.

A SPC data object named MTTRs has been included in the MMTR logical node. This control will reset the demand measurements. A SPC data object named MTTRs is also included in the PTTR logical node. This control will reset the thermal measurements.

- Scaled Measurements

The Unit definition, as per IEC specifies an SI unit and an optional multiplier for each measurement. This allows a magnitude of measurement to be specified e.g. mA, A, kA, MA.

The multiplier will always be included in the Unit definition and will be configurable in SCL, but not settable at runtime. It will apply to the magnitude, rangeC.min & rangeC.max attributes. rangeC.min & rangeC.max will not be settable at runtime to be more consistent with Px30 and to reduce configuration problems regarding deadbands.

Setting changes, such as changes to protection settings, are done using MiCOM S1 Studio. These changes can also be done using the relay's front port serial connection or the relay's Ethernet link, and is known as "tunneling".

7.3.2 IEC 61850 Configuration

One of the main objectives of IEC 61850 is to allow IEDs to be directly configured from a configuration file generated at system configuration time. At the system configuration level, the capabilities of the IED are determined from an IED capability description file (ICD), which is provided with the product. Using a collection of these ICD files from different products, the entire protection of a substation can be designed, configured and tested (using simulation tools) before the product is even installed into the substation.

To help this process, the MiCOM S1 Studio Support Software provides an IEC61850 IED Configurator tool. Select **Tools > IEC61850 IED Configurator**. This tool allows the preconfigured IEC 61850 configuration file (SCD or CID) to be imported and transferred to the IED. The configuration files for MiCOM relays can also be created manually, based on their original IED Capability Description (ICD) file.

Other features include the extraction of configuration data for viewing and editing, and a sophisticated error-checking sequence. The error checking ensures the configuration data is valid for sending to the IED and ensures the IED functions correctly in the substation.

To help the user, some configuration data is available in the **IED CONFIGURATOR** column of the relay user interface, allowing read-only access to basic configuration data.

7.3.2.1 Configuration Banks

To promote version management and minimize down-time during system upgrades and maintenance, the MiCOM relays have incorporated a mechanism consisting of multiple configuration banks. These configuration banks are categorized as:

- Active Configuration Bank
- Inactive Configuration Bank

Any new configuration sent to the relay is automatically stored in the inactive configuration bank, therefore not immediately affecting the current configuration. Both active and inactive configuration banks can be extracted at any time.

When the upgrade or maintenance stage is complete, the IED Configurator tool can be used to transmit a command to a single IED. This command authorizes the activation of the new configuration contained in the inactive configuration bank, by switching the active and inactive configuration banks. This technique ensures that the system down-time is minimized to the start-up time of the new configuration. The capability to switch the configuration banks is also available using the **IED CONFIGURATOR** column.

For version management, data is available in the **IED CONFIGURATOR** column in the relay user interface, displaying the SCL Name and Revision attributes of both configuration banks.

7.3.2.2 Network Connectivity

Note	*This section presumes a prior knowledge of IP addressing and related topics. Further details on this topic may be found on the Internet (search for IP Configuration) and in numerous relevant books.*

Configuration of the relay IP parameters (IP Address, Subnet Mask, Gateway) and SNTP time synchronization parameters (SNTP Server 1, SNTP Server 2) is performed by the IED Configurator tool. If these parameters are not available using an SCL file, they must be configured manually.

If the assigned IP address is duplicated elsewhere on the same network, the remote communications do not operate in a fixed way. However, the relay checks for a conflict at power up and every time the IP configuration is changed. An alarm is raised if an IP conflict is detected.

Use the **Gateway** setting to configure the relay to accept data from networks other than the local network.

7.4 Data Model of MiCOM Relays

The data model naming adopted in the Px30 and Px40 relays has been standardized for consistency. The Logical Nodes are allocated to one of the five Logical Devices, as appropriate, and the wrapper names used to instantiate Logical Nodes are consistent between Px30 and Px40 relays.

The data model is described in the Model Implementation Conformance Statement (MICS) document, which is available separately. The MICS document provides lists of Logical Device definitions, Logical Node definitions, Common Data Class and Attribute definitions, Enumeration definitions, and MMS data type conversions. It generally follows the format used in Parts 7-3 and 7-4 of the IEC 61850 standard.

7.5 Communication Services of MiCOM Relays

The IEC 61850 communication services which are implemented in the Px30 and Px40 relays are described in the Protocol Implementation Conformance Statement (PICS) document, which is available separately. The PICS document provides the Abstract Communication Service Interface (ACSI) conformance statements as defined in Annex A of Part 7-2 of the IEC 61850 standard.

7.6 Peer-to-Peer (GSE) Communications

The implementation of IEC 61850 Generic Substation Event (GSE) sets the way for cheaper and faster inter-relay communications. The generic substation event model provides fast and reliable system-wide distribution of input and output data values. The generic substation event model is based on autonomous decentralization This provides an efficient method of allowing simultaneous delivery of the same generic substation event information to more than one physical device, by using multicast services.

The use of multicast messaging means that IEC 61850 GOOSE uses a publisher-subscriber system to transfer information around the network*. When a device detects a change in one of its monitored status points, it publishes (sends) a new message. Any device that is interested in the information subscribes (listens) to the data message.

Note*	*Multicast messages cannot be routed across networks without specialized equipment.*

Each new message is retransmitted at user-configurable intervals until the maximum interval is reached, to overcome possible corruption due to interference and collisions. In practice, the parameters which control the message transmission cannot be calculated. Time must be allocated to the testing of GSE schemes before or during commissioning; in just the same way a hardwired scheme must be tested.

7.6.1 Scope

A maximum of 32 virtual inputs are available in the PSL which can be mapped directly to a published dataset in a GOOSE message (only 1 fixed dataset is supported). All published GOOSE signals are BOOLEAN values.

Each GOOSE signal contained in a subscribed GOOSE message can be mapped to any of the 32 virtual inputs in the PSL. The virtual inputs allow the mapping to internal logic functions for protection control, directly to output contacts or LEDs for monitoring.

The MiCOM relay can subscribe to all GOOSE messages but only the following data types can be decoded and mapped to a virtual input:

- BOOLEAN
- BSTR2
- INT16
- INT32
- INT8
- UINT16
- UINT32
- UINT8

7.6.2 IEC 61850 GOOSE Configuration

From MiCOM S1 Studio select Tools > IEC61850 IED Configurator.

Make sure the configuration is correct as this ensures efficient GOOSE scheme operation.

Use the relay user interface to enable GOOSE signaling and to apply Test Mode.

7.7 Ethernet Functionality

Settings relating to a failed Ethernet link are available in the ‘COMMUNICATIONS’ column of the relay user interface.

7.7.1 Ethernet Disconnection

IEC 61850 ‘Associations’ are unique and made to the relay between the client (master) and server (IEC 61850 device). If the Ethernet is disconnected, such associations are lost and must be re-established by the client. The TCP_KEEPALIVE function is implemented in the relay to monitor each association and terminate any which are no longer active.

7.7.2 Loss of Power

If the relay's power is removed, the relay allows the client to re-establish associations without a negative impact on the relay’s operation. As the relay acts as a server in this process, the client must request the association. Uncommitted settings are cancelled when power is lost. Reports requested by connected clients are reset and must be re-enabled by the client when the client next creates the new association to the relay.

8 SECOND REAR COMMUNICATIONS PORT (COURIER)

Relays with Courier, MODBUS, IEC60870-5-103 or DNP3.0 protocol on the first rear communications port have the option of a second rear port, running the Courier language. The second port is intended typically for dial-up modem access by protection engineers or operators, when the main port is reserved for SCADA communication traffic. Communication is through one of three physical links: K-Bus, EIA(RS)-485 or EIA(RS)-232. The port supports full local or remote protection and control access using MiCOM S1 Studio.

When changing the port configuration between K-Bus, EIA(RS)-485 and EIA(RS)-232, reboot the relay to update the hardware configuration of the second rear port.

The EIA(RS)-485 and EIA(RS)-232 protocols can be configured to operate with a modem, using an IEC60870 10-bit frame.

Port Configuration	Valid Communication Protocol
K-Bus	K-Bus
EIA(RS)-232	IEC60870 FT1.2, 11-bit frame IEC60870, 10-bit frame
EIA(RS)-485	IEC60870 FT1.2, 11-bit frame IEC60870, 10-bit frame

Table 16 - Port configurations and communication protocols

If both rear communications ports are connected to the same bus, make sure their address settings are not the same to avoid message conflicts.

8.1 Courier Protocol

See the following documentation for a detailed description of the Courier protocol, command set and link description.

- R6509 K-Bus Interface Guide
- R6510 IEC60870 Interface Guide
- R6511 Courier Protocol
- R6512 Courier User Guide

The second rear communications port is functionally the same as described in *section 2.2* for a Courier rear communications port, with the following exceptions:

8.1.1 Event Extraction

Automatic event extraction is not supported when the first rear port protocol is Courier, MODBUS or CS103. It is supported when the first rear port protocol is DNP3.0.

8.1.2 Disturbance Record Extraction

Automatic disturbance record extraction is not supported when the first rear port protocol is Courier, MODBUS or CS103. It is supported when the first rear port protocol is DNP3.0.

8.1.3 Connection to the Second Rear Port

The second rear Courier port connects using the 9-way female D-type connector (SK4) in the middle of the card end plate (between the IRIG-B connector and lower D-type). The connection complies with EIA(RS)-574.

For IEC60870-5-2 over EIA(RS)-232	
Pin	**Connection**
1	No Connection
2	RxD
3	TxD
4	DTR#
5	Ground
6	No Connection
7	RTS#
8	CTS#
9	No Connection
# - These pins are control lines for use with a modem.	

For K-bus or IEC60870-5-2 over EIA(RS)-485	
Pin*	**Connection**
4	EIA(RS)-485 - 1 (+ ve)
7	EIA(RS)-485 - 2 (- ve)
* - All other pins unconnected.	

Notes

Connector pins 4 and 7 are used by both the EIA(RS)-232and EIA(RS)-485 physical layers, but for different purposes. Therefore, the cables should be removed during configuration switches.

When using the EIA(RS)-485 protocol, an EIA(RS)-485 to EIA(RS)-232 converter is needed to connect the relay to a modem or PC running MiCOM S1 Studio. A Schneider Electric CK222 is recommended.

EIA(RS)-485 is polarity sensitive, with pin 4 positive (+) and pin 7 negative (-).

The K-Bus protocol can be connected to a PC using a KITZ101 or 102.

Table 17 - Pin connections over EIA(RS)-232 and EIS(RS)-485

9 SK5 PORT CONNECTION

The lower 9-way D-type connector (SK5) is currently unsupported.

Do not connect to this port.

Notes:

SYMBOLS AND GLOSSARY

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Notes:

1 ACRONYMS AND ABBREVIATIONS

Term	Description
<	Less than: Used to indicate an “under” threshold, such as undercurrent (current dropout).
>	Greater than: Used to indicate an “over” threshold, such as overcurrent (current overload)
A	Ampere
AA	Application Association
AC / ac	Alternating Current
ACSI	Abstract Communication Service Interface
ACSR	Aluminum Conductor Steel Reinforced
ALF	Accuracy Limit Factor
AM	Amplitude Modulation
ANSI	American National Standards Institute
AR	Auto-Reclose.
ARIP	Auto-Reclose In Progress
ASCII	American Standard Code for Information Interchange
ATEX	ATEX is the Potentially Explosive Atmospheres directive 94/9/EC
AUX / Aux	Auxiliary
AWG	American Wire Gauge
BAR	Block Auto-Reclose signal.
BCD	Binary Coded Decimal
BCR	Binary Counter Reading
BDEW	Bundesverband der Energie- und Wasserwirtschaft | Startseite (i.e. German Association of Energy and Water Industries)
BMP	BitMaP – a file format for a computer graphic
BOP	Blocking Overreach Protection - a blocking aided-channel scheme.
BPDU	Bridge Protocol Data Unit
BRCB	Buffered Report Control Block
BRP	Beacon Redundancy Protocol
BU	Backup: Typically a back-up protection element
C264	MiCOM C264 is the latest generation of modular substation computers. In addition to the traditional input/output (I/O) management, MiCOM C264 acts as a powerful communication gateway, an advanced measurement center and a fast automation processor. As a remote terminal unit, bay controller or protocol converter, MiCOM C264 is the compact solution to countless applications installed in demanding electromagnetic conditions.
C/O	A ChangeOver contact having normally-closed and normally-open connections: Often called a “form C” contact.
CB	Circuit Breaker
CB Aux.	Circuit Breaker auxiliary contacts: Indication of the breaker open/closed status.
CBF	Circuit Breaker Failure protection
CDC	Common Data Class
CF	Control Function
Ch	Channel: usually a communications or signaling channel
Check Synch	Check Synchronizing function

Term	Description
CLIO	Current Loop Input Output: 0-1 mA/0-10 mA/0-20 mA/4-20 mA transducer inputs and outputs CLI = current loop input - 0-1 mA/0-10 mA/0-20 mA/4-20 mA transducer input CLO = current loop output - 0-1 mA/0-10 mA/0-20 mA/4-20 mA transducer output
CIP	Critical Infrastructure Protection standards
CLK / Clk	Clock
Cls	Close - generally used in the context of close functions in circuit breaker control.
CMV	Complex Measured Value
CNV	Current No Volts
CPNI	Centre for the Protection of National Infrastructure
CRC	Cyclic Redundancy Check
CRP	Cross-network Redundancy Protocol
CRV	Curve (file format for curve information)
CRx	Channel Receive: Typically used to indicate a teleprotection signal received.
CS	Check Synchronism.
CSV	Comma Separated Values (a file format for database information)
CT	Current Transformer
CTRL	Control - as used for the Control Inputs function
CTS	Current Transformer Supervision: To detect CT input failure.
CTx	Channel Transmit: Typically used to indicate a teleprotection signal send.
CUL	Canadian Underwriters Laboratory
CVT	Capacitor-coupled Voltage Transformer - equivalent to terminology CCVT.
DAU	Data Acquisition Unit
DC	Data Concentrator
DC / dc	Direct Current
DCC	An Omicron compatible format
DCE	Data Communication Equipment
DDB	Digital Data Bus within the programmable scheme logic: A logic point that has a zero or 1 status. DDB signals are mapped in logic to customize the relay’s operation.
DDR	Dynamic Disturbance Recorder
DEF	Directional Earth Fault protection: A directionalized ground fault aided scheme.
df/dt	Rate of Change of Frequency
df/dt>1	First stage of df/dt protection
DFT	Discrete Fourier Transform
DG	Distributed Generation
DHCP	Dynamic Host Configuration Protocol
DHM	Dual Homing Manager
DHP	Dual Homing Protocol
Diff	Differential protection.
DIN	Deutsches Institut für Normung (German standards body)
Dist	Distance protection.
DITA	Darwinian Information Typing Architecture
DLDB	Dead-Line Dead-Bus : In system synchronism check, indication that both the line and bus are de-energised.

Term	Description
DLLB	Dead-Line Live-Bus : In system synchronism check, indication that the line is de-energised whilst the bus is energised.
DLR	Dynamic Line Rating
DLY / Dly	Time Delay
DMT	Definite Minimum Time
DNP	Distributed Network Protocol
DPWS	Device Profile for Web Services
DSP	Digital Signal Processor
DST	Daylight Saving Time
DT	Definite Time: in the context of protection elements: An element which always responds with the same constant time delay on operation. Abbreviation of “Dead Time” in the context of auto-reclose:
DTD	Document Type Definition
DTOC	Definite Time Overcurrent
DTS	Date and Time Stamp
EF or E/F	Earth Fault (Directly equivalent to Ground Fault)
EIA	Electronic Industries Alliance
ELR	Environmental Lapse Rate
EMC	ElectroMagnetic Compatibility
ENA	Energy Networks Association
ER	Engineering Recommendation
ESD	Electrostatic Discharge
FAA	Ageing Acceleration Factor: Used by Loss of Life (LOL) element
FFail	A field failure (loss of excitation) element: Could be labeled 40 in ANSI terminology.
FFT	Fast Fourier Transform
FIR	Finite Impulse Response
FLC	Full load current: The nominal rated current for the circuit.
FLT / Flt	Fault - typically used to indicate faulted phase selection.
Fn or FN	Function
FPGA	Field Programmable Gate Array
FPS	Frames Per Second
FTP	File Transfer Protocol or Foil Twisted Pair
FWD, Fwd or Fwd.	Indicates an element responding to a flow in the “Forward” direction
Gen Diff	A generator differential element: Could be labeled 87G in ANSI terminology.
Gen-Xformer Diff	A generator-transformer differential element: Could be labeled 87GT in ANSI terminology.
GIF	Graphic Interchange Format – a file format for a computer graphic
GND / Gnd	Ground: used in distance settings to identify settings that relate to ground (earth) faults.
GOOSE	Generic Object Oriented Substation Event
GPS	Global Positioning System
GRP / Grp	Group. Typically an alternative setting group.

Term	Description
GSE	General Substation Event
GSSE	Generic Substation Status Event
GUESS	Generator Unintentional Energization at StandStill.
GUI	Graphical User Interface
HMI	Human Machine Interface
HSR	High-availability Seamless Ring
HTML	Hypertext Markup Language
I	Current
I/O	Input/Output
I/P	Input
IANA	Internet Assigned Numbers Authority
ICAO	International Civil Aviation Organization
ID	Identifier or Identification. Often a label used to track a software version installed.
IDMT	Inverse Definite Minimum Time. A characteristic whose trip time depends on the measured input (e.g. current) according to an inverse-time curve.
IEC	International Electro-technical Commission
IED	Intelligent Electronic Device - a term used to describe microprocessor-based controllers of power system equipment. Common types of IEDs include protective relaying devices, load tap changer controllers, circuit breaker controllers, capacitor bank switches, recloser controllers, voltage regulators, etc.
IEEE	Institute of Electrical and Electronics Engineers
IETF	Internet Engineering Task Force
IIR	Infinite Impulse Response
Inh	An Inhibit signal
Inst	An element with Instantaneous operation: i.e. having no deliberate time delay.
IP	Internet Protocol
IRIG	InterRange Instrumentation Group
ISA	International Standard Atmosphere
ISA	Instrumentation Systems and Automation Society
ISO	International Standards Organization
JPEF	Joint Photographic Experts Group – a file format for a computer graphic
L	Live
LAN	Local Area Network
LCD	Liquid Crystal Display: The front-panel text display on the relay.
LD	Level Detector: An element responding to a current or voltage below its set threshold.
LDOV	Level Detector for Overvoltage
LDUV	Level Detector for Undervoltage
LED	Light Emitting Diode: Red or green indicator on the front-panel.
LLDB	Live-Line Dead-Bus : In system synchronism check, indication that the line is energized whilst the bus is de-energized.
Ln	Natural logarithm
LN	Logical Node
LoL	A Loss of Load scheme, providing a fast distance trip without needing a signaling channel.
LPDU	Link Protocol Data Unit

Term	Description
LPHD	Logical Physical Device
MC	MultiCast
MCB	Miniature Circuit Breaker
MIB	Management Information Base
MICS	Model Implementation Conformance Statement
MIDOS	Modular Integrated DrawOut System
MMF	Magneto-Motive Force
MMS	Manufacturing Message Specification
MRP	Media Redundancy Protocol
MU	Merging Unit
MV	Measured Value
N	Neutral
N/A	Not Applicable
N/C	A Normally Closed or “break” contact: Often called a “form B” contact.
N/O	A Normally Open or “make” contact: Often called a “form A” contact.
NERC	North American Reliability Corporation
NIST	National Institute of Standards and Technology
NPS	Negative Phase Sequence
NVD	Neutral voltage displacement: Equivalent to residual overvoltage protection.
NXT	Abbreviation of “Next”: In connection with hotkey menu navigation.
O/C	Overcurrent
O/P	Output
OCB	Oil Circuit Breaker
OID	Object IDentifier
Opto	An Optically coupled logic input. Alternative terminology: binary input.
OSI	Open Systems Interconnection
PCB	Printed Circuit Board
PCT	Protective Conductor Terminal (Ground)
PDC	Phasor Data Concentrator
Ph	Phase - used in distance settings to identify settings that relate to phase-phase faults.
PICS	Protocol Implementation Conformance Statement
PMU	Phasor Measurement Unit
PNG	Portable Network Graphics – a file format for a computer graphic
Pol	Polarize - typically the polarizing voltage used in making directional decisions.
POR	A Permissive OverReaching transfer trip scheme (alternative terminology: POTT).
PRP	Parallel Redundancy Protocol
PSB	Power Swing Blocking, to detect power swing/out of step functions (ANSI 78).
PSL	Programmable Scheme Logic: The part of the relay’s logic configuration that can be modified by the user, using the graphical editor within MiCOM S1 Studio software.
PSlip	A Pole slip (out of step - OOS) element: could be labeled 78 in ANSI terminology.
PT	Power Transformer
PTP	Precision Time Protocol

Term	Description
PUR	A Permissive UnderReaching transfer trip scheme (alternative terminology: PUTT).
Q	Quantity defined as per unit value
R	Resistance
R&TTE	Radio and Telecommunications Terminal Equipment
RBAC	Role Based Access Control
RCA	Relay Characteristic Angle - The center of the directional characteristic.
REB	Redundant Ethernet Board
REF	Restricted Earth Fault
Rev.	Indicates an element responding to a flow in the “reverse” direction
RMS / rms	Root mean square. The equivalent a.c. current: Taking into account the fundamental, plus the equivalent heating effect of any harmonics.
RP	Rear Port: The communication ports on the rear of the IED
RS232	A common serial communications standard defined by the EIA
RS485	A common serial communications standard defined by the EIA (multi-drop)
RST or Rst	Reset generally used in the context of reset functions in circuit breaker control.
RSTP	Rapid Spanning Tree Protocol
RTD	Resistance Temperature Device
RTU	Remote Terminal Unit
Rx	Receive: Typically used to indicate a communication transmit line/pin.
SBS	Straight Binary Second
SC	Synch-Check or system Synchronism Check.
SCADA	Supervisory Control and Data Acquisition
SCL	Substation Configuration Language
SCU	Substation Control Unit
SEF	Sensitive Earth Fault Protection
Sen	Sensitive
SHM	Self-Healing Manager
SHP	Self Healing Protocol
SIR	Source Impedance Ratio
SLA	Service Level Agreement
SMV	Sampled Measured Values
SNTP	Simple Network Time Protocol
SOA	Service Oriented Architecture
SOAP	Simple Object Access Protocol
SOC	Second of Century
SOTF	Switch on to Fault protection. Modified protection on manual closure of the circuit breaker.
SP	Single pole.
SPAR	Single pole auto-reclose.
SPC	Single Point Controllable
SPDT	Single Pole Dead Time. The dead time used in single pole auto-reclose cycles.
SPS	Single Point Status
SQRT	Square Root
SSL	Source Impedance Ratio

Term	Description
STP	Shielded Twisted Pair or Spanning Tree Protocol
SV	Sampled Values
SVC	Sampled Value Model
SVM	Sampled Value Model
TAF	Turbine Abnormal Frequency
TCP	Transmission Control Protocol
TCS	Second of Century
TCS	Trip Circuit Supervision
TD	Time Dial. The time dial multiplier setting: Applied to inverse-time curves (ANSI/IEEE).
TE	Unit for case measurements: One inch = 5TE units
THD	Total Harmonic Distortion
TICS	Technical Issues Conformance Statement
TIFF	Tagged Image File Format – a file format for a computer graphic
TLS	Transport Layer Security protocol
TMS	Time Multiplier Setting: Applied to inverse-time curves (IEC)
TOC	Trip On Close (“line check”) protection. Offers SOTF and TOR functionality.
TOR	Trip On Reclose protection. Modified protection on autoreclosure of the circuit breaker.
TP	Two-Part
TUC	Timed UnderCurrent
TVE	Total Vector Error
Tx	Transmit
UDP	User Datagram Protocol
UL	Underwriters Laboratory
UPCT	User Programmable Curve Tool
UTC	Universal Time Coordinated
V	Voltage
VA	Phase A voltage: Sometimes L1, or red phase
VB	Phase B voltage: Sometimes L2, or yellow phase
VC	Phase C voltage: Sometimes L3, or blue phase
VCO	Voltage Controlled Overcurrent element
VDEP OC>	A voltage dependent overcurrent element: could be a voltage controlled or voltage restrained overcurrent element and could be labeled 51V in ANSI terminology.
VDR	Voltage Dependant Resistor
V/Hz	An overfluxing element, flux is proportional to voltage/frequency: could be labeled 24 in ANSI terminology.
Vk	IEC knee point voltage of a current transformer.
VT	Voltage Transformer
VTS	Voltage Transformer Supervision: To detect VT input failure.
WAN	Wide Area Network
Xformer	Transformer
XML	Extensible Markup Language

Term	Description
XSD	XML Schema Definition

Table 1 - Acronyms and abbreviations

2 COMPANY PROPRIETARY TERMS

Symbol	Description
Courier	Schneider Electric’s proprietary SCADA communications protocol
Metrosil	Brand of non-linear resistor produced by M&I Materials Ltd.
MiCOM	Schneider Electric’s brand of protection relays

Table 2 - Company-proprietary terms

3 ANSI TERMS

ANSI no.	Description
3PAR	Three pole auto-reclose.
3PDT	Three pole dead time. The dead time used in three pole auto-reclose cycles.
52a	A circuit breaker closed auxiliary contact: The contact is in the same state as the breaker primary contacts
52b	A circuit breaker open auxiliary contact: The contact is in the opposite state to the breaker primary contacts
64R	Rotor earth fault protection
64S	100% stator earth (ground) fault protection using a low frequency injection method.

Table 3 - ANSI abbreviations

ANSI no.	Function	Description
Current Protection Functions		
50/51	Phase overcurrent	Three-phase protection against overloads and phase-to-phase short-circuits.
50N/51N	Earth fault	Earth fault protection based on measured or calculated residual current values: • 50N/51N: residual current calculated or measured by 3 phase current sensors
50G/51G	Sensitive earth fault	Sensitive earth fault protection based on measured residual current values: • 50G/51G: residual current measured directly by a specific sensor such as a core balance CT
50BF	Breaker failure	If a breaker fails to be triggered by a tripping order, as detected by the non-extinction of the fault current, this backup protection sends a tripping order to the upstream or adjacent breakers.
46	Negative sequence / unbalance	Protection against phase unbalance, detected by the measurement of negative sequence current: • sensitive protection to detect 2-phase faults at the ends of long lines • protection of equipment against temperature build-up, caused by an unbalanced power supply, phase inversion or loss of phase, and against phase current unbalance
46BC	Broken conductor protection	Protection against phase imbalance, detected by measurement of I2/I1.
49RMS	Thermal overload	Protection against thermal damage caused by overloads on machines (transformers, motors or generators). The thermal capacity used is calculated according to a mathematical model which takes into account: • current RMS values • ambient temperature • negative sequence current, a cause of motor rotor temperature rise
Re-Closer		
79	Recloser	Automation device used to limit down time after tripping due to transient or semipermanent faults on overhead lines. The recloser orders automatic reclosing of the breaking device after the time delay required to restore the insulation has elapsed. Recloser operation is easy to adapt for different operating modes by parameter setting.
Directional Current Protection		
67N/67NC type 1 and 67	Directional phase overcurrent	Phase-to-phase short-circuit protection, with selective tripping according to fault current direction. It comprises a phase overcurrent function associated with direction detection, and picks up if the phase overcurrent function in the chosen direction (line or busbar) is activated for at least one of the three phases.

ANSI no.	Function	Description
67N/67NC	Directional earth fault	Earth fault protection, with selective tripping according to fault current direction. Three types of operation: • Type 1: the protection function uses the projection of the I0 vector • Type 2: the protection function uses the I0 vector magnitude with half-plane tripping zone • Type 3: the protection function uses the I0 vector magnitude with angular sector tripping zone
67N/67NC type 1	Directional current protection	Directional earth fault protection for impedant, isolated or compensated neutral systems, based on the projection of measured residual current.
67N/67NC type 2	Directional current protection	Directional overcurrent protection for impedance and solidly earthed systems, based on measured or calculated residual current. It comprises an earth fault function associated with direction detection, and picks up if the earth fault function in the chosen direction (line or busbar) is activated.
67N/67NC type 3	Directional current protection	Directional overcurrent protection for distribution networks in which the neutral earthing system varies according to the operating mode, based on measured residual current. It comprises an earth fault function associated with direction detection (angular sector tripping zone defined by 2 adjustable angles), and picks up if the earth fault function in the chosen direction (line or busbar) is activated.
Directional Power Protection Functions		

32P	Directional active overpower	Two-way protection based on calculated active power, for the following applications:
		• active overpower protection to detect overloads and allow load shedding
		• reverse active power protection:
		  • against generators running like motors when the generators consume active power
		  • against motors running like generators when the motors supply active power

32Q/40	Directional reactive overpower	Two-way protection based on calculated reactive power to detect field loss on synchronous machines: • reactive overpower protection for motors which consume more reactive power with field loss • reverse reactive overpower protection for generators which consume reactive power with field loss.
Machine Protection Functions		
37	Phase undercurrent	Protection of pumps against the consequences of a loss of priming by the detection of motor no-load operation. It is sensitive to a minimum of current in phase 1, remains stable during breaker tripping and may be inhibited by a logic input.

48/51LR/14	Locked rotor / excessive starting time	Protection of motors against overheating caused by:
		• excessive motor starting time due to overloads (e.g. conveyor) or insufficient supply voltage.
		The reacceleration of a motor that is not shut down, indicated by a logic input, may be considered as starting.
		• locked rotor due to motor load (e.g. crusher):
		  • in normal operation, after a normal start
		  • directly upon starting, before the detection of excessive starting time, with detection of locked rotor by a zero speed detector connected to a logic input, or by the underspeed function.

66	Starts per hour	Protection against motor overheating caused by:
		• too frequent starts: motor energizing is inhibited when the maximum allowable number of starts is reached, after counting of:
		  • starts per hour (or adjustable period)
		  • consecutive motor hot or cold starts (reacceleration of a motor that is not shut down, indicated by a logic input, may be counted as a start)
		• starts too close together in time: motor re-energizing after a shutdown is only allowed after an adjustable waiting time.

ANSI no.	Function	Description
50V/51V	Voltage-restrained overcurrent	Phase-to-phase short-circuit protection, for generators. The current tripping set point is voltage-adjusted in order to be sensitive to faults close to the generator which cause voltage drops and lowers the short-circuit current.
26/63	Thermostat/Buchholz	Protection of transformers against temperature rise and internal faults via logic inputs linked to devices integrated in the transformer.
38/49T	Temperature monitoring	Protection that detects abnormal temperature build-up by measuring the temperature inside equipment fitted with sensors: • transformer: protection of primary and secondary windings • motor and generator: protection of stator windings and bearings.
Voltage Protection Functions		
27D	Positive sequence undervoltage	Protection of motors against faulty operation due to insufficient or unbalanced network voltage, and detection of reverse rotation direction.
27R	Remanent undervoltage	Protection used to check that remanent voltage sustained by rotating machines has been cleared before allowing the busbar supplying the machines to be re-energized, to avoid electrical and mechanical transients.
27	Undervoltage	Protection of motors against voltage sags or detection of abnormally low network voltage to trigger automatic load shedding or source transfer. Works with phase-to-phase voltage.
59	Overvoltage	Detection of abnormally high network voltage or checking for sufficient voltage to enable source transfer. Works with phase-to-phase or phase-to-neutral voltage, each voltage being monitored separately.
59N	Neutral voltage displacement	Detection of insulation faults by measuring residual voltage in isolated neutral systems.
47	Negative sequence overvoltage	Protection against phase unbalance resulting from phase inversion, unbalanced supply or distant fault, detected by the measurement of negative sequence voltage.
Frequency Protection Functions		
81O	Overfrequency	Detection of abnormally high frequency compared to the rated frequency, to monitor power supply quality. Other organizations may use 81H instead of 81O.
81U	Underfrequency	Detection of abnormally low frequency compared to the rated frequency, to monitor power supply quality. The protection may be used for overall tripping or load shedding. Protection stability is ensured in the event of the loss of the main source and presence of remanent voltage by a restraint in the event of a continuous decrease of the frequency, which is activated by parameter setting. Other organizations may use 81L instead of 81U.
81R	Rate of change of frequency	Protection function used for fast disconnection of a generator or load shedding control. Based on the calculation of the frequency variation, it is insensitive to transient voltage disturbances and therefore more stable than a phase-shift protection function. **Disconnection** In installations with autonomous production means connected to a utility, the “rate of change of frequency” protection function is used to detect loss of the main system in view of opening the incoming circuit breaker to: • protect the generators from a reconnection without checking synchronization • avoid supplying loads outside the installation. **Load shedding** The “rate of change of frequency” protection function is used for load shedding in combination with the underfrequency protection to: • either accelerate shedding in the event of a large overload • or inhibit shedding following a sudden drop in frequency due to a problem that should not be solved by shedding.
Dynamic Line Rating (DLR) Protection Functions		

ANSI no.	Function	Description
49DLR	Dynamic line rating (DLR)	Protection of overhead lines based on calculation of rating or ampacity to dynamically take into account the effect of prevailing weather conditions as monitored by external sensors for: • Ambient Temperature • Wind Velocity • Wind Direction • Solar Radiation

Table 4 - ANSI descriptions

4 CONCATENATED TERMS

Term
Undercurrent
Overcurrent
Overfrequency
Underfrequency
Undervoltage
Overvoltage

Table 5 - Concatenated terms

5 UNITS FOR DIGITAL COMMUNICATIONS

Unit	Description
b	bit
B	Byte
kb	Kilobit(s)
kbps	Kilobits per second
kB	Kilobyte(s)
Mb	Megabit(s)
Mbps	Megabits per second
MB	Megabyte(s)
Gb	Gigabit(s)
Gbps	Gigabits per second
GB	Gigabyte(s)
Tb	Terabit(s)
Tbps	Terabits per second
TB	Terabyte(s)

Table 6 - Units for digital communications

6 AMERICAN VS BRITISH ENGLISH TERMINOLOGY

British English	American English
…ae…	…e…
…ence	…ense
…ise	…ize
…oe…	…e…
…ogue	…og
…our	…or
…ourite	…orite
…que	…ck
…re	…er
…yse	…yze
Aluminium	Aluminum
Centre	Center
Earth	Ground
Fibre	Fiber
Ground	Earth
Speciality	Specialty

Table 7 - American vs British English terminology

7 LOGIC SYMBOLS AND TERMS

Symbol	Description	Units
&	Logical "AND": Used in logic diagrams to show an AND-gate function.	
Σ	"Sigma": Used to indicate a summation, such as cumulative current interrupted.	
τ	"Tau": Used to indicate a time constant, often associated with thermal characteristics.	
ω	System angular frequency	rad
<	Less than: Used to indicate an "under" threshold, such as undercurrent (current dropout).	
>	Greater than: Used to indicate an "over" threshold, such as overcurrent (current overload)	
o	A small circle on the input or output of a logic gate: Indicates a NOT (invert) function.	
1	Logical "OR": Used in logic diagrams to show an OR-gate function.	
ABC	Clockwise phase rotation.	
ACB	Anti-Clockwise phase rotation.	
C	Capacitance	A
df/dt	Rate of Change of Frequency protection	Hz/s
df/dt>1	First stage of df/dt protection	Hz/s
F<	Underfrequency protection: Could be labeled 81-U in ANSI terminology.	Hz
F>	Overfrequency protection: Could be labeled 81-O in ANSI terminology.	Hz
F<1	First stage of under frequency protection: Could be labeled 81-U in ANSI terminology.	Hz
F>1	First stage of over frequency protection: Could be labeled 81-O in ANSI terminology.	Hz
f_{max}	Maximum required operating frequency	Hz
f_{min}	Minimum required operating frequency	Hz
f_n	Nominal operating frequency	Hz
I	Current	A
I∧	Current raised to a power: Such as when breaker statistics monitor the square of ruptured current squared (∧ power = 2).	An
I'f	Maximum internal secondary fault current (may also be expressed as a multiple of In)	A
I<	An undercurrent element: Responds to current dropout.	A
I>>	Current setting of short circuit element	In
I>	A phase overcurrent protection: Could be labeled 50/51 in ANSI terminology.	A
I>1	First stage of phase overcurrent protection: Could be labeled 51-1 in ANSI terminology.	A
I>2	Second stage of phase overcurrent protection: Could be labeled 51-2 in ANSI terminology.	A
I>3	Third stage of phase overcurrent protection: Could be labeled 51-3 in ANSI terminology.	A
I>4	Fourth stage of phase overcurrent protection: Could be labeled 51-4 in ANSI terminology.	A
I0	Earth fault current setting Zero sequence current: Equals one third of the measured neutral/residual current.	A
I1	Positive sequence current.	A
I2	Negative sequence current.	A
I2>	Negative sequence overcurrent protection (NPS element).	A
I2pol	Negative sequence polarizing current.	A
I2therm>	A negative sequence thermal element: Could be labeled 46T in ANSI terminology.	
IA	Phase A current: Might be phase L1, red phase.. or other, in customer terminology.	A
IB	Phase B current: Might be phase L2, yellow phase.. or other, in customer terminology.	A
IC	Phase C current: Might be phase L3, blue phase.. or other, in customer terminology.	A
Idiff	Current setting of biased differential element	A

Symbol	Description	Units
If	Maximum secondary through-fault current	A
If max	Maximum secondary fault current (same for all feeders)	A
If max int	Maximum secondary contribution from a feeder to an internal fault	A
If Z1	Maximum secondary phase fault current at Zone 1 reach point	A
Ife	Maximum secondary through fault earth current	A
IfeZ1	Maximum secondary earth fault current at Zone 1 reach point	A
Ifn	Maximum prospective secondary earth fault current or 31 x I> setting (whichever is lowest)	A
Ifp	Maximum prospective secondary phase fault current or 31 x I> setting (whichever is lowest)	A
I_m	Mutual current	A
IM64	InterMiCOM64.	
IMx	InterMiCOM64 bit (x=1 to 16)	
I_n	Current transformer nominal secondary current. The rated nominal current of the relay: Software selectable as 1 amp or 5 amp to match the line CT input.	A
IN	Neutral current, or residual current: This results from an internal summation of the three measured phase currents.	A
IN>	A neutral (residual) overcurrent element: Detects earth/ground faults.	A
IN>1	First stage of ground overcurrent protection: Could be labeled 51N-1 in ANSI terminology.	A
IN>2	Second stage of ground overcurrent protection: Could be labeled 51N-2 in ANSI terminology.	A
Inst	An element with “instantaneous” operation: i.e. having no deliberate time delay.	
I/O	Inputs and Outputs - used in connection with the number of optocoupled inputs and output contacts within the relay.	
I/P	Input	
Iref	Reference current of P63x calculated from the reference power and nominal voltage	A
IREF>	A Restricted Earth Fault overcurrent element: Detects earth (ground) faults. Could be labeled 64 in ANSI terminology.	A
IRm2	Second knee-point bias current threshold setting of P63x biased differential element	A
Is	Value of stabilizing current	A
IS1	Differential current pick-up setting of biased differential element	A
IS2	Bias current threshold setting of biased differential element	A
I_{SEF}>	Sensitive earth fault overcurrent element.	A
Isn	Rated secondary current (I secondary nominal)	A
Isp	Stage 2 and 3 setting	A
Ist	Motor start up current referred to CT secondary side	A
K	Dimensioning factor	
K_1	Lower bias slope setting of biased differential element	%
K_2	Higher bias slope setting of biased differential element	%
K_e	Dimensioning factor for earth fault	
km	Distance in kilometers	
K_{max}	Maximum dimensioning factor	
K_{rpa}	Dimensioning factor for reach point accuracy	
K_s	Dimensioning factor dependent upon through fault current	
K_{ssc}	Short circuit current coefficient or ALF	
K_t	Dimensioning factor dependent upon operating time	
kZm	The mutual compensation factor (mutual compensation of distance elements and fault locator for parallel line coupling effects).	

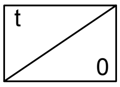
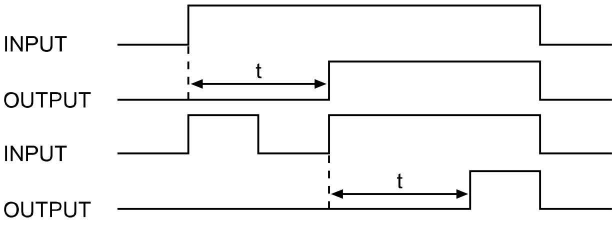
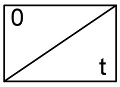
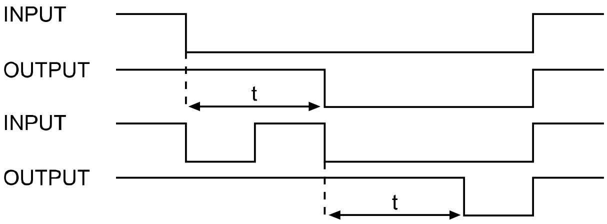
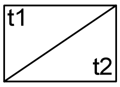
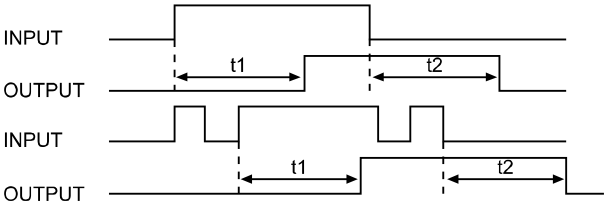
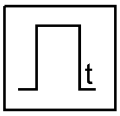
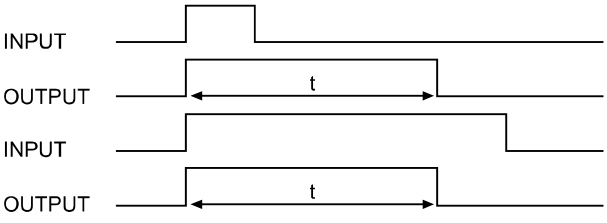
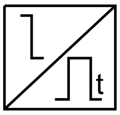
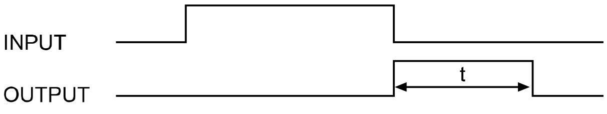
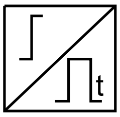
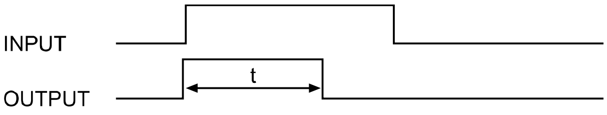
Symbol	Description	Units
kZN	The residual compensation factor: Ensuring correct reach for ground distance elements.	
L	Inductance	A
m1	Lower bias slope setting of P63x biased differential element	None
m2	Higher bias slope setting of P63x biased differential element	None
mi	Distance in miles.	
N	Indication of “Neutral” involvement in a fault: i.e. a ground (earth) fault.	
-P>	A reverse power (W) element: could be labeled 32R in ANSI terminology.	
P>	An overpower (W) element: could be labeled 32O in ANSI terminology.	
P<	A low forward power (W) element: could be labeled 32L in ANSI terminology.	
P1	Used in IEC terminology to identify the primary CT terminal polarity: Replace by a dot when using ANSI standards.	
P2	Used in IEC terminology to identify the primary CT terminal polarity: The non-dot terminal.	
P_n	Rotating plant rated single phase power	W
PN>	Wattmetric earth fault protection: Calculated using residual voltage and current quantities.	
Q<	A reactive under power (VAr) element	
R	Resistance (Ω)	Ω
R< or 64S R<	A 100% stator earth (ground) fault via low frequency injection under resistance element: could be labeled 64S in ANSI terminology.	
R Gnd.	A distance zone resistive reach setting: Used for ground (earth) faults.	
R Ph	A distance zone resistive reach setting used for Phase-Phase faults.	
Rct	Secondary winding resistance	Ω
Rl	Resistance of single lead from relay to current transformer	Ω
Rr	Resistance of any other protective relays sharing the current transformer	Ω
Rrn	Resistance of relay neutral current input	Ω
Rrp	Resistance of relay phase current input	Ω
Rs	Value of stabilizing resistor	Ω
Rx	Receive: typically used to indicate a communication receive line/pin.	
S<	An apparent under power (VA) element	
S1	Used in IEC terminology to identify the secondary CT terminal polarity: Replace by a dot when using ANSI standards.	
S2	Used in IEC terminology to identify the secondary CT terminal polarity: The non-dot terminal. Also used to signify negative sequence apparent power, S2 = V2 x I2.	
S2>	A negative sequence apparent power element, S2 = V2 x I2.	
t	A time delay.	
t’	Duration of first current flow during auto-reclose cycle	s
T1	Primary system time constant	s
TF	Through Fault monitoring	
tfr	Auto-reclose dead time	s
Thermal I>	A stator thermal overload element: could be labeled 49 in ANSI terminology.	
Thru/TF	Through Fault monitoring	
tIdiff	Current differential operating time	s
Ts	Secondary system time constant	s
Tx	Transmit: typically used to indicate a communication transmit line/pin.	
V	Voltage.	V
V<	An undervoltage element: could be labeled 27 in ANSI terminology	V

Symbol	Description	Units
V<1	First stage of undervoltage protection: Could be labeled 27-1 in ANSI terminology.	V
V<2	Second stage of undervoltage protection: Could be labeled 27-2 in ANSI terminology.	V
V>	An overvoltage element: could be labeled 59 in ANSI terminology	V
V>1	First stage of overvoltage protection: Could be labeled 59-1 in ANSI terminology.	V
V>2	Second stage of overvoltage protection: Could be labeled 59-2 in ANSI terminology.	V
V0	Zero sequence voltage: Equals one third of the measured neutral/residual voltage.	V
V1	Positive sequence voltage.	V
V2	Negative sequence voltage.	V
V2>	A negative phase sequence (NPS) overvoltage element: could be labeled 47 in ANSI terminology.	
$V2_{pol}$	Negative sequence polarizing voltage.	V
V_A	Phase A voltage: Might be phase L1, red phase.. or other, in customer terminology.	V
V_B	Phase B voltage: Might be phase L2, yellow phase.. or other, in customer terminology.	V
V_C	Phase C voltage: Might be phase L3, blue phase.. or other, in customer terminology.	V
Vf	Theoretical maximum voltage produced if CT saturation did not occur	V
Vin	Input voltage e.g. to an opto-input	V
V_k	Required CT knee-point voltage. IEC knee point voltage of a current transformer.	V
VN	Neutral voltage displacement, or residual voltage.	V
VN>	A residual (neutral) overvoltage element: could be labeled 59N in ANSI terminology.	V
V_n	Nominal voltage	V
Vn	The rated nominal voltage of the relay: To match the line VT input.	V
VN>1	First stage of residual (neutral) overvoltage protection.	V
VN>2	Second stage of residual (neutral) overvoltage protection.	V
VN3H>	A 100% stator earth (ground) fault 3rd harmonic residual (neutral) overvoltage element: could be labeled 59TN in ANSI terminology.	
VN3H<	A 100% stator earth (ground) fault 3rd harmonic residual (neutral) undervoltage element: could be labeled 27TN in ANSI terminology.	
Vres.	Neutral voltage displacement, or residual voltage.	V
Vs	Value of stabilizing voltage	V
V_x	An auxiliary supply voltage: Typically the substation battery voltage used to power the relay.	V
WI	Weak Infeed logic used in teleprotection schemes.	
X	Reactance	None
X/R	Primary system reactance/resistance ratio	None
Xe/Re	Primary system reactance/resistance ratio for earth loop	None
Xt	Transformer reactance (per unit)	p.u.
Y	Admittance	p.u.
Z	Impedance	p.u.
Z<	An under impedance element: could be labeled 21 in ANSI terminology.	
Z0	Zero sequence impedance.	
Z1	Positive sequence impedance.	
Z1	Zone 1 distance protection.	
Z1X	Reach-stepped Zone 1X, for zone extension schemes used with auto-reclosure.	
Z2	Negative sequence impedance.	
Z2	Zone 2 distance protection.	
ZP	Programmable distance zone that can be set forward or reverse looking.	

Symbol	Description	Units
Zs	Used to signify the source impedance behind the relay location.	
Φal	Accuracy limit flux	Wb
Ψr	Remanent flux	Wb
Ψs	Saturation flux	Wb

Table 8 - Logic Symbols and Terms

8 LOGIC TIMERS

Logic symbols	Explanation	Time chart
	Delay on pick-up timer, t	 INPUT OUTPUT t INPUT OUTPUT t
	Delay on drop-off timer, t	 INPUT OUTPUT t INPUT OUTPUT t
	Delay on pick-up/drop-off timer	 INPUT OUTPUT t1 t2 INPUT OUTPUT t1 t2
	Pulse timer	 INPUT OUTPUT t INPUT OUTPUT t
	Pulse pick-up falling edge	 INPUT OUTPUT t
	Pulse pick-up raising edge	 INPUT OUTPUT t

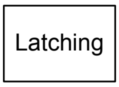
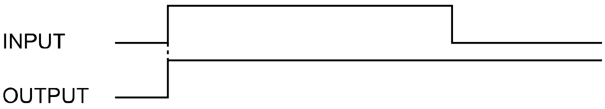
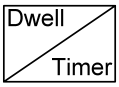
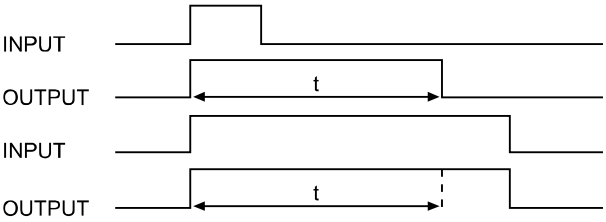
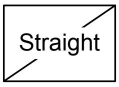
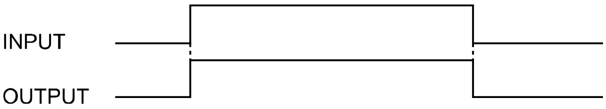
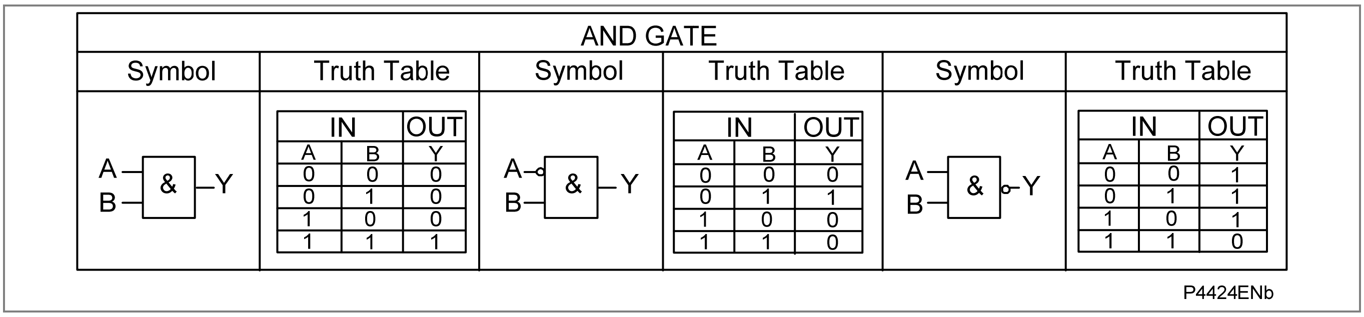
Logic symbols	Explanation	Time chart
	Latch	 INPUT OUTPUT
 Dwell Timer	Dwell timer	 INPUT OUTPUT t INPUT OUTPUT t
	Straight (non latching): Hold value until input reset signal	 INPUT OUTPUT

Table 9 - Logic Timers

9 LOGIC GATES

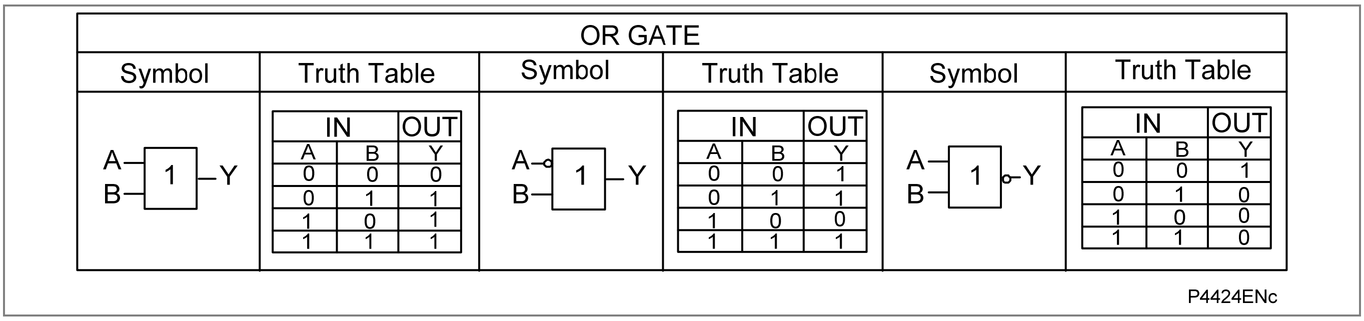

AND GATE
Symbol
Truth Table
A
B
&
Y
P4424ENb

IN		OUT
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

IN		OUT
A	B	Y
0	0	0
0	1	1
1	0	0
1	1	0

IN		OUT
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Figure 1 - Logic Gates - AND Gate

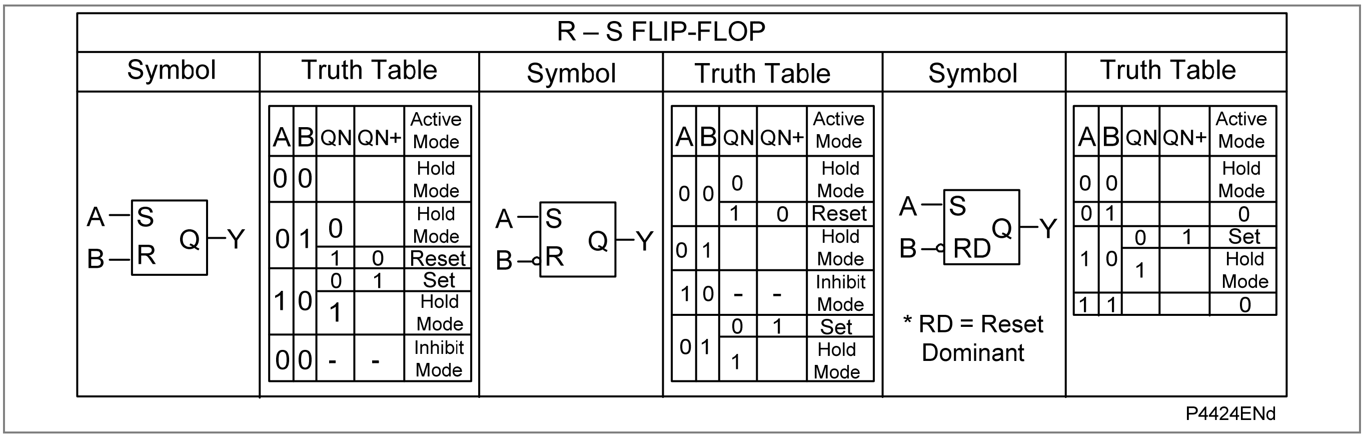

OR GATE
Symbol
Truth Table
A
B
1
Y
P4424ENc

IN		OUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

IN		OUT
A	B	Y
0	0	1
0	1	1
1	0	0
1	1	1

IN		OUT
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Figure 2 - Logic Gates - OR Gate


R – S FLIP-FLOP
Symbol
Truth Table
A
B
S
R
Q
Y
RD
P4424ENd

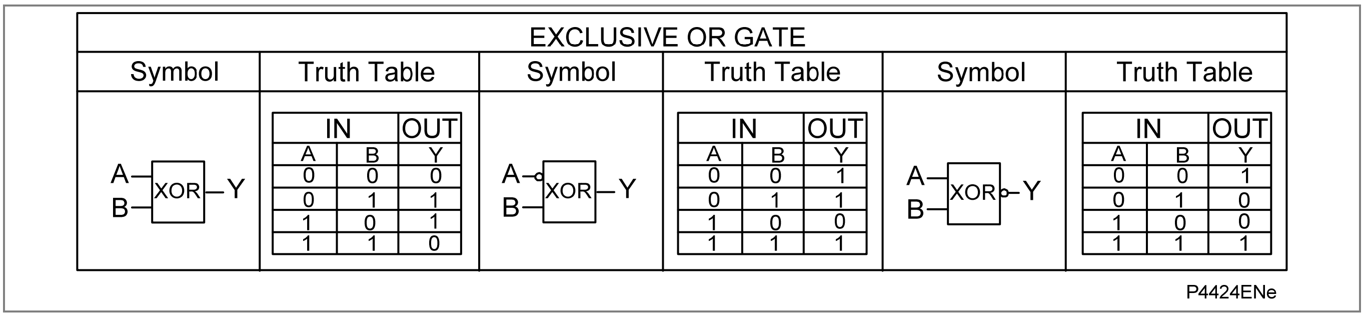
A	B	QN	QN+	Active Mode
0	0			Hold Mode
0	1	0		Hold Mode
		1	0	Reset
1	0	0	1	Set
		1		Hold Mode
0	0	-	-	Inhibit Mode

A	B	QN	QN+	Active Mode
0	0	0		Hold Mode
		1	0	Reset
0	1			Hold Mode
1	0	-	-	Inhibit Mode
0	1	0	1	Set
		1		Hold Mode

* RD = Reset Dominant

A	B	QN	QN+	Active Mode
0	0			Hold Mode
0	1			0
1	0	0	1	Set
		1		Hold Mode
1	1			0

Figure 3 - Logic Gates - R-S Flip-Flop Gate

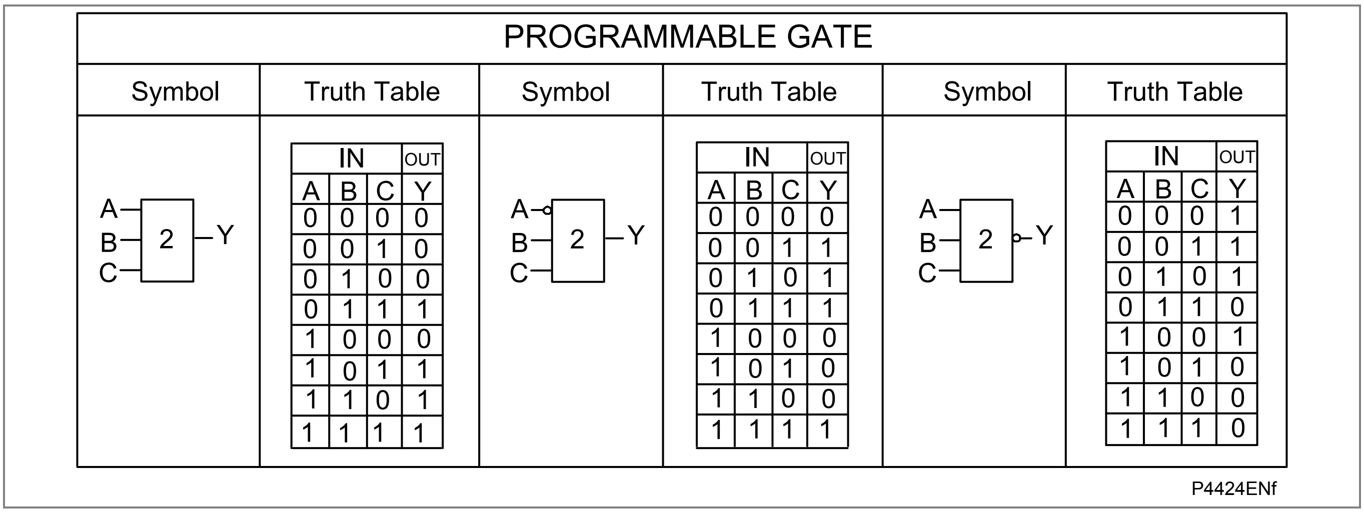

EXCLUSIVE OR GATE
Symbol
Truth Table
A
B
XOR
Y
P4424ENe

IN		OUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

IN		OUT
A	B	Y
0	0	1
0	1	1
1	0	0
1	1	1

IN		OUT
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Figure 4 - Logic Gates - Exclusive OR Gate

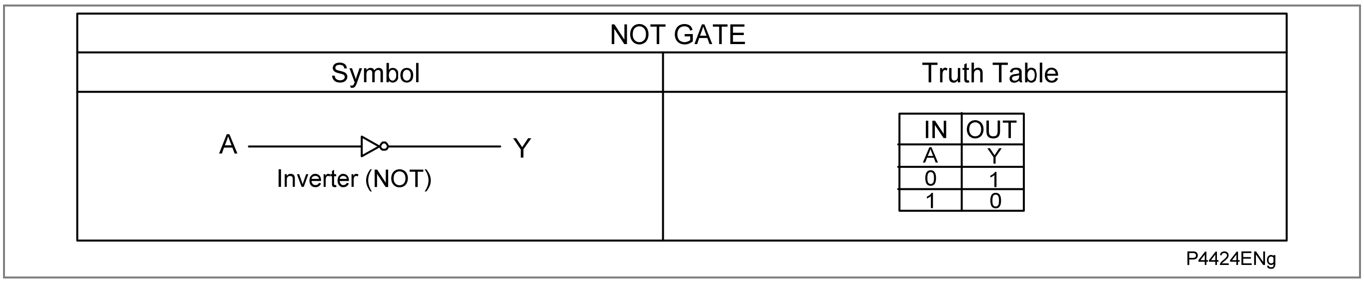

PROGRAMMABLE GATE
Symbol
Truth Table
Symbol
Truth Table
Symbol
Truth Table
A
B
C
2
Y
A
B
C
2
Y
A
B
C
2
Y
P4424ENf

IN			OUT
A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

IN			OUT
A	B	C	Y
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	1

IN			OUT
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

Figure 5 - Logic Gates - Programmable Gate


NOT GATE
Symbol
Truth Table
A
Y
Inverter (NOT)
P4424ENg

IN	OUT
A	Y
0	1
1	0

Figure 6 - Logic Gates - NOT Gate

Notes:

INSTALLATION

CHAPTER NO 15

Date:	12/2013
Hardware Suffix:	J (P642) K(P643/P645)
Software Version:	04
Connection Diagrams:	10P642xx (xx = 1 to 10) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9)

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1 RECEIPT, HANDLING, STORAGE AND UNPACKING

1.1 Receipt of Relays

Protective relays, although generally of robust construction, require careful treatment before installation on site. On receipt, examine relays immediately to ensure there has been no external damage in transit. If the relay has been damaged, make a claim to the transport contractor and notify Red House Consultancy Services Ltd promptly.

Relays that are supplied unmounted and not intended for immediate installation should be returned to their protective polythene bags and delivery carton. Section 1.3 - Storage gives more information about the storage of relays.

1.2 Handling Electronic Equipment

Caution	**Before carrying out any work on the equipment, the user should be familiar with the contents of the Safety Guide (SFTY/4L M/G11) or later issue, or the Safety and Technical Data sections of this Technical Manual and also the ratings on the equipment's rating label.**

A person's normal movements can easily generate electrostatic potentials of several thousand volts. Discharge of these voltages into semiconductor devices when handling electronic circuits can cause serious damage that, although not always immediately apparent, reduces the reliability of the circuit.

The relay's electronic circuits are protected from electrostatic discharge when housed in the case. Do not expose them to risk by removing the front panel or Printed Circuit Boards (PCBs) unnecessarily.

Each PCB incorporates the highest practicable protection for its semiconductor devices. However, if it becomes necessary to remove a PCB, the following precautions should be taken to preserve the high reliability and long life for which the relay has been designed and manufactured.

- Before removing a PCB, ensure that you are at the same electrostatic potential as the equipment by touching the case.
- Handle analog input modules by the front panel, frame or edges of the PCBs. PCBs should only be handled by their edges. Avoid touching the electronic components, printed circuit tracks or connectors.
- Do not pass the module to another person without first ensuring you are both at the same electrostatic potential. Shaking hands achieves this.
- Place the module on an anti-static surface, or on a conducting surface that is at the same potential as yourself.
- If it is necessary to store or transport PCBs removed from the case, place them individually in electrically conducting anti-static bags.

In the unlikely event that you make measurements on the internal electronic circuitry of a relay in service, you must be earthed (grounded) to the case with a conductive wrist strap. Wrist straps should have a resistance to ground of 500kΩ to 10 MΩ. If a wrist strap is not available, keep frequent contact with the case to prevent a build-up of electrostatic potential. Instrumentation which may be used for measurements should also be earthed (grounded) to the case.

Detailed investigations on electronic circuitry or modification work should be carried out in a special handling area. For more information on safe working procedures for all electronic equipment, see *BS EN 100015: Part 1:1992*.

1.3 Storage

If relays are not installed immediately on receipt, store them in a place free from dust and moisture in their original cartons. Keep any de-humidifier bags included in the packing. The de-humidifier crystals lose their efficiency if the bag is exposed to ambient conditions. Restore the crystals by gently heating the bag for about an hour before replacing it in the carton.

To prevent battery drain during transportation and storage, a battery isolation strip is fitted during manufacture. Open the lower access cover and check the red tab of the battery isolation strip protrudes from the positive battery terminal.

On subsequent unpacking, make sure that any dust on the carton does not fall inside. In locations of high humidity the carton and packing may become impregnated with moisture and the de-humidifier crystals will lose their efficiency.

Before installation, store relays between –25º to +70ºC (-13ºF to +158ºF).

1.4 Unpacking

When unpacking and installing the relays, take care not to damage any of the parts and make sure that additional components are not accidentally left in the packing or lost. Do not discard any User’s CDROM or technical documentation - this should accompany the relay to its destination substation.

Note *With the lower access cover open, the red tab of the battery isolation strip protrudes from the positive battery terminal. Do not remove this strip because it prevents battery drain during transportation and storage and will be removed as part of the commissioning tests. See Figure 1.*

Relays must only be handled by skilled persons.

The site should be well lit to aid inspection, clean, dry and reasonably free from dust and excessive vibration. This particularly applies to installations that are being carried out at the same time as construction work.

2 RELAY MOUNTING

MiCOM relays are dispatched either individually or as part of a panel or rack assembly.

Individual relays are normally supplied with an outline diagram showing the dimensions for panel cut-outs and hole centers. This information can also be found in the product publication.

Secondary front covers to prevent unauthorized changing of settings and alarm status can be supplied as an optional item. They are available in sizes:

- 40TE (GN0037 001) and 60TE/80TE (GN0038 001) for P64xxxxxxxxxxxA/B/C and
- 40TE (GN0242 001) and 60TE/80TE (GN0243 001) for P64xxxxxxxxxxxJ/K.

The relay is designed so the fixing holes in the mounting flanges are only accessible when the access covers are open.

If you include a P991 or MMLG test block with the relays, when viewed from the front, position the test block on the right-hand side of the associated relays. This minimizes the wiring between the relay and test block, and allows the correct test block to be easily identified during commissioning and maintenance tests.

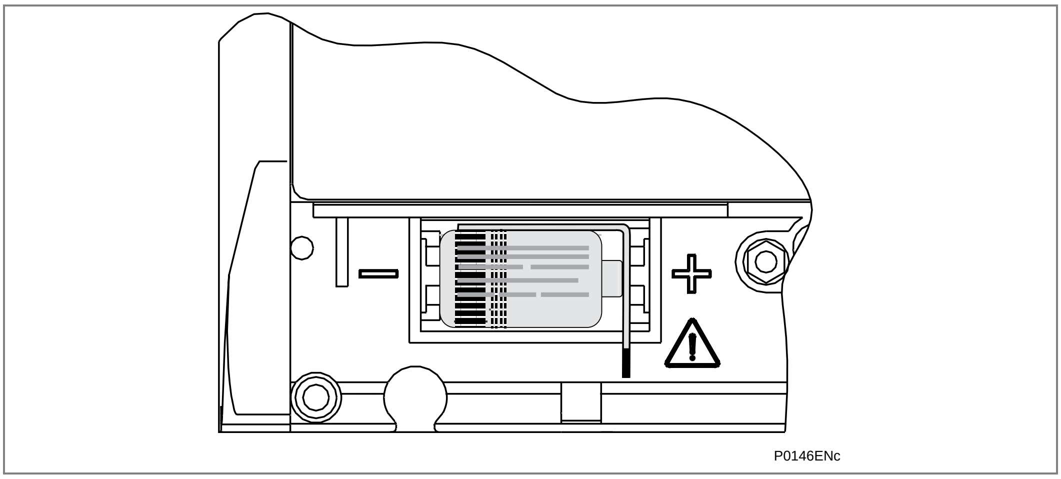


Figure 1 - Location of battery isolation strip

If you need to test the relay for correct operation during installation, remove the battery isolation strip. If commissioning of the scheme is not imminent, refit the strip to prevent unnecessary battery drain during transportation and installation. The red tab of the isolation strip protrudes from the positive battery terminal when the lower access cover is open. To remove the isolation strip, hold the battery in place and pull the red tab. To refit the battery isolation strip, insert it between the battery and the battery compartment positive terminal, with the red tab protruding. See Figure 1.

2.1 Rack Mounting

MiCOM relays can be rack mounted using single-tier rack frames (part number FX0021 101), see Figure 2. These frames have dimensions in accordance with IEC60297 and are supplied pre-assembled ready to use. On a standard 483 mm rack this enables combinations of case widths up to a total equivalent of size 80TE to be mounted side by side.

The two horizontal rails of the rack frame have holes drilled at approximately 26 mm intervals. Attach the relays by their mounting flanges using M4 Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit). These fastenings are available in packs of five (part number ZA0005 104).

Warning **Risk of damage to the front cover molding. Do not use conventional self-tapping screws, including those supplied for mounting MiDOS relays because they have slightly larger heads.**

Once the tier is complete, the frames are fastened into the racks using mounting angles at each end of the tier.

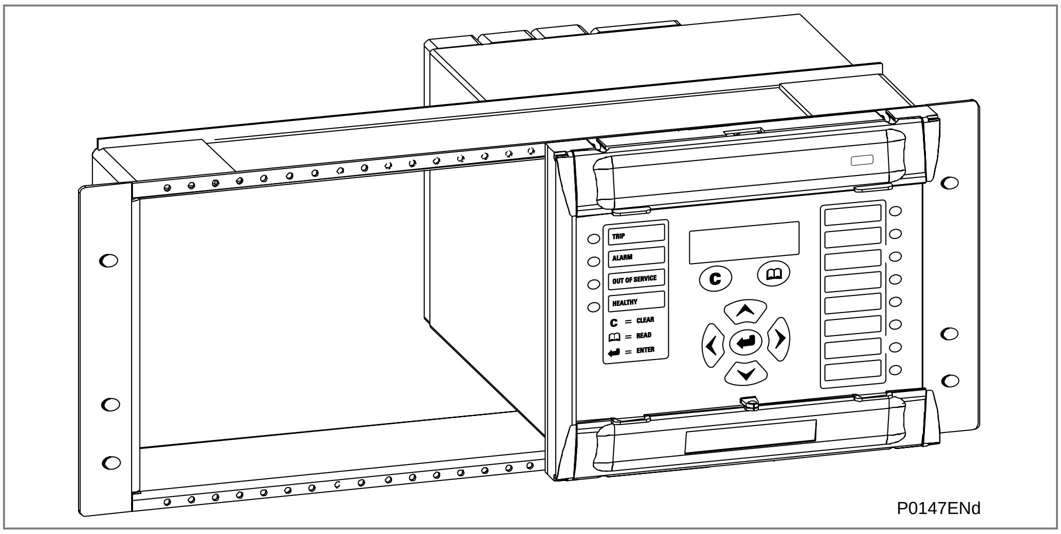


Figure 2 - Rack mounting of relays

Relays can be mechanically grouped into single tier (4U) or multi-tier arrangements using the rack frame. This enables schemes using products from the MiCOM and MiDOS product ranges to be pre-wired together before mounting.

Use blanking plates if there are empty spaces. The spaces may be for future installation of relays or because the total size is less than 80TE on any tier. Blanking plates can also be used to mount ancillary components. Table 1 shows the sizes that can be ordered.

Note *Blanking plates are only available in black.*

For further details on mounting MiDOS relays, see publication *R7012, MiDOS Parts Catalogue and Assembly Instructions*.

Case size summation	Blanking plate part number
5TE	GJ2028 101
10TE	GJ2028 102
15TE	GJ2028 103
20TE	GJ2028 104
25TE	GJ2028 105
30TE	GJ2028 106
35TE	GJ2028 107
40TE	GJ2028 108

Table 1 - Blanking plates

2.2 Panel Mounting

The relays can be flush mounted into panels using M4 SEMS Taptite self-tapping screws with captive 3 mm thick washers (also known as a SEMS unit). These fastenings are available in packs of five (Red House Consultancy Services Ltd part number ZA0005 104).

Warning **Risk of damage to the front cover molding. Do not use conventional self-tapping screws, including those supplied for mounting MiDOS relays because they have slightly larger heads.**

Alternatively tapped holes can be used if the panel has a minimum thickness of 2.5 mm.

For applications where relays need to be semi-projection or projection mounted, a range of collars are available. Further details can be obtained from the Red House Consultancy Services Ltd Contracts Department.

If several relays are mounted in a single cut-out in the panel, mechanically group them horizontally or vertically into rigid assemblies before mounting in the panel.

Note *Fastening MiCOM relays with pop rivets is not advised because it does not allow easy removal if repair is necessary.*

If a relay assembly is mounted on a panel complying with BS EN60529 IP52, fit a metallic sealing strip between adjoining relays (Part no GN2044 001) and fit a sealing ring from Table 2 around the complete assembly.

Width	Single tier	Double tier
10TE	GJ9018 002	GJ9018 018
15TE	GJ9018 003	GJ9018 019
20TE	GJ9018 004	GJ9018 020
25TE	GJ9018 005	GJ9018 021
30TE	GJ9018 006	GJ9018 022
35TE	GJ9018 007	GJ9018 023
40TE	GJ9018 008	GJ9018 024
45TE	GJ9018 009	GJ9018 025
50TE	GJ9018 010	GJ9018 026
55TE	GJ9018 011	GJ9018 027
60TE	GJ9018 012	GJ9018 028
65TE	GJ9018 013	GJ9018 029
70TE	GJ9018 014	GJ9018 030
75TE	GJ9018 015	GJ9018 031
80TE	GJ9018 016	GJ9018 032

Table 2 - IP52 sealing rings

For further details on mounting MiDOS relays, see publication *R7012, MiDOS Parts Catalogue and Assembly Instructions*.

3 RELAY WIRING

This section serves as a guide to selecting the appropriate cable and connector type for each terminal on the MiCOM relay.

Caution **Before carrying out any work on the equipment the user should be familiar with the contents of the Safety Section or Safety Guide SFTY/4LM/G11 or later issue and the ratings on the equipment's rating label.**

3.1 Medium and Heavy Duty Terminal Block Connections

Loose relays are supplied with sufficient M4 screws for making connections to the rear-mounted terminal blocks using ring terminals, with a recommended maximum of two ring terminals per relay terminal.

If required, Red House Consultancy Services Ltd can supply M4 90° crimp ring terminals in three different sizes depending on wire size (see Table 3). Each type is available in bags of 100.

Part number	Wire size	Insulation color
ZB9124 901	0.25 – 1.65 mm2 (22 – 16 AWG)	Red
ZB9124 900	1.04 – 2.63 mm2 (16 – 14 AWG)	Blue
ZB9124 904	2.53 – 6.64 mm2 (12 – 10 AWG)	Not insulated*

* *To maintain the terminal block insulation requirements for safety, fit an insulating sleeve over the ring terminal after crimping.*

Table 3 - M4 90° crimp ring terminals

The following minimum wire sizes are recommended:

Current Transformers	2.5 mm^2
Auxiliary Supply, Vx	1.5 mm^2
EIA(RS)485 Port	See separate section
Other Circuits	1.0 mm^2

Due to the limitations of the ring terminal, the maximum wire size that can be used for any of the medium or heavy duty terminals is 6.0 mm^2 using ring terminals that are not pre-insulated. If using only pre-insulated ring terminals, the maximum wire size that can be used is reduced to 2.63 mm^2 per ring terminal. If you need a larger wire size, use two wires in parallel, each terminated in a separate ring terminal at the relay.

The wire used for all connections to the medium and heavy duty terminal blocks, except the first rear EIA(RS)485 port and second rear EIA(RS)232/485 port, should have a minimum voltage rating of 300 Vrms.

It is recommended that the auxiliary supply wiring is protected by a 16 A High Rupture Capacity (HRC) fuse of type NIT or TIA. For safety reasons, current transformer circuits must never be fused. Other circuits should be appropriately fused to protect the wire used.

Each opto input has selectable filtering. This allows use of a preset filter of ½ cycle which renders the input immune to induced noise on the wiring: although this method is secure it can be slow, particularly for intertripping. This can be improved by switching off the ½ cycle filter in which case one of the following methods to reduce ac noise should be considered. The first method is to use double pole switching on the input, the second is to use screened twisted cable on the input circuit. The recognition time of the opto inputs without the filtering is <2 ms and with the filtering is <12 ms.

3.2 EIA(RS)485 Port

Connections to the first rear EIA(RS)485 port use ring terminals. 2-core screened cable is recommended with a maximum total length of 1000 m or 200 nF total cable capacitance.

A typical cable specification would be:

Each core:	16/0.2 mm copper conductors PVC insulated
Nominal conductor area:	0.5 mm^2 per core
Screen:	Overall braid, PVC sheathed

3.3 Ethernet Port for IEC 61850 (if Applicable)

3.3.1 Fiber Optic Port

The relays can have a 100 Mbps Ethernet port. FO connection is recommended for use in permanent connections in a substation environment. The 100 Mbit port uses a type ST connector, compatible with fiber multimode 50/125 µm or 62.5/125 µm to 13000 nm.

3.3.2 RJ-45 Metallic Port

The relays can be connected to either a 10Base-T or a 100Base-TX Ethernet hub; the port automatically senses which type of hub is connected. Due to the possibility of noise and interference, this connection type is recommended for short-term connections over short distances, ideally where the relays and hubs are in the same cubicle.

The connector for the Ethernet port is a shielded RJ-45. Table 4 shows the signals and pins on the connector.

Pin	Signal name	Signal definition
1	TXP	Transmit (positive)
2	TXN	Transmit (negative)
3	RXP	Receive (positive)
4	-	Not used
5	-	Not used
6	RXN	Receive (negative)
7	-	Not used
8	-	Not used

Table 4 - Signals on the Ethernet connector

3.4 RTD Connections (if Applicable)

Where RTD inputs are available on a MiCOM relay, the connections are made using screw clamp connectors on the rear of the relay that can accept wire sizes between 0.1 mm^2 and 1.5 mm^2. The connections between the relay and the RTDs must be made using a screened 3-core cable with a total resistance less than 10 Ω. The cable should have a minimum voltage rating of 300 Vrms.

A 3-core cable should be used even for 2-wire RTD applications, as it allows for the cable's resistance to be removed from the overall resistance measurement. In such cases the 3rd wire is connected to the 2nd wire at the point the cable is joined to the RTD.

The screen of each cable must only be earthed (grounded) at one end, preferably at the relay end and must be continuous. Multiple earthing (grounding) of the screen can cause circulating current to flow along the screen, which induces noise and is unsafe.

It is recommended to minimize noise pick-up in the RTD cables by keeping them close to earthed (grounded) metal casings and avoiding areas of high electromagnetic and radio interference. The RTD cables should not be run adjacent to or in the same conduit as other high voltage or current cables.

A typical cable specification would be:

Each core:	7/0.2 mm copper conductors heat resistant PVC insulated
Nominal conductor area:	0.22 mm^2 per core
Screen:	Nickel-plated copper wire braid heat resistant PVC sheathed

The following extract may be useful in defining cable recommendations for the RTDs.

Noise pick up by cables can be categorized into these types:

- Resistive
- Capacitive
- Inductive

Resistive coupling requires an electrical connection to the noise source. Assuming the wire and cable insulation are in good condition and the junctions are clean, this can be dismissed.

Capacitive coupling requires sufficient capacitance for the impedance path to the noise source to be small enough to allow for significant coupling. This is a function of the dielectric strength between the signal cable on the noise source and the power of the noise source.

Inductive coupling occurs when the signal cable is adjacent to a wire carrying the noise or it is exposed to a radiated EMF.

Standard screened cable is normally used to protect against capacitively-coupled noise. However, for it to be effective the screen must only be bonded to the system ground at one point, otherwise a current could flow and the noise would be coupled into the signal wires of the cable. There are different types of screening available, but basically there are two types: aluminium foil wrap and tin-copper braid.

Foil screens are good for low to medium frequencies and braid is good for high frequencies. High-fidelity screen cables provide both types.

Protection against magnetic inductive coupling requires very careful cable routing and magnetic shielding. The latter can be achieved with steel-armored cable and steel cable trays. The cable armor must be grounded at both ends so the EMF of the induced current cancels the field of the noise source and shields the cables conductors from it. However, the system ground must be designed to not bridge two isolated ground systems since this could be hazardous and defeat the objectives of the original ground design. The cable should be laid in the cable trays as close as possible to the metal of the tray and under no circumstance should any power cable be in or near to the tray. Power cables should only cross the signal cables at 90 degrees and never be adjacent to them.

Both the capacitive and inductive screens must be contiguous from the RTD probes to the relay terminals.

The best types of cable are those provided by the RTD manufacturers. These are usually three conductors, known as a triad, which are screened with foil. Such triad cables are available in armored forms as well as multi-triad armored forms.

3.5 Current Loop Input Output (CLIO) Connections (if Applicable)

Screw clamp connectors are used on MiCOM relays that have current loop inputs and outputs. The connectors are on the rear of the relay and can accept wire sizes from 0.1 mm^2 to 1.5 mm^2. Screened cable is recommended for connections between the relay and the current loop inputs and outputs. The wire should have a minimum voltage rating of 300 Vrms.

3.6 IRIG-B Connections (if Applicable)

The IRIG-B input has a BNC connection. The cable and connector shave a recommended characteristic impedance of 50 Ω. Connections between the IRIG-B equipment and the relay are recommended to be made using coaxial cable 50Ω characteristic impedance with a halogen free, fire retardant sheath, type RG59LSF.

3.7 EIA(RS)232 Port

Short-term connections to the EIA(RS)232 port, behind the bottom access cover, can be made using a screened multi-core communication cable up to 15 m long, or a total capacitance of 2500 pF. The cable should be terminated at the relay end with a 9-way metal-shelled D-type male plug. See the *Getting Started* chapter *P64x/EN GS* of this manual for the pin allocations.

3.8 Download/Monitor Port

Short term connections to the download/monitor port, behind the bottom access cover, can be made using a screened 25-core communication cable up to 4 m long. The cable should be terminated at the relay end with a 25-way, metal shelled, D-type male plug. See the *Getting Started* chapter *P64x/EN CM* of this manual for the pin allocations.

3.9 Second EIA(RS)232/485 Port

Relays with Courier, MODBUS, IEC60870-5-103 or DNP3 protocol on the first rear communications port have the option of a second rear port, running Courier language.

The second rear communications port can be used over one of three physical links:

- twisted pair K-Bus (non-polarity sensitive)
- twisted pair EIA(RS)485 (connection polarity sensitive) or
- EIA(RS)232. This port complies with EIA(RS)574, the 9-pin version of EIA(RS)232, see www.tiaonline.org

3.9.1 Connection to the Second Rear Port

The second rear Courier port uses a 9-way female D-type connector (SK4) in the middle of the card end plate, between IRIG-B connector and lower D-type. The connection complies with EIA(RS)574.

Pin	Connection
1	No Connection
2	RxD
3	TxD
4	DTR#
5	Ground

Pin	Connection
6	No Connection
7	RTS#
8	CTS#
9	No Connection

Table 5 - IEC60870-5-2 over EIA(RS)232/574 pin allocations

Connections to the second rear port configured for EIA(RS)232 operation can be made using a screened multi-core communication cable up to 15 m long, or a total capacitance of 2500 pF. The cable should be terminated at the relay end with a 9-way, metal shelled D-type male plug. Table 5 shows the pin allocations.

3.9.2 For K-bus or IEC60870-5-2 over EIA(RS)485

Pin*	Connection
4	EIA(RS)485 - 1 (+ ve)
7	EIA(RS)485 - 2 (- ve)
* - All other pins disconnected.	
# - These pins are control lines for use with a modem.	

Notes:

Connector pins 4 and 7 are used by both the EIA(RS)232/574 and EIA(RS)485 physical layers, but for different purposes. Therefore, the cables should be removed during configuration switches.

For the EIA(RS)485 protocol an EIA(RS)485 to EIA(RS)232/574 converter is needed to connect a modem or PC running MiCOM S1, to the relay. A Red House Consultancy Services Ltd CK222 is recommended.

EIA(RS)485 is polarity-sensitive, with pin 4 positive (+) and pin 7 negative (-).

The K-Bus protocol can be connected to a PC using a KITZ101 or 102.

2-core screened cable is recommended. To avoid exceeding the second communications port flash clearances, the length of cable between the port and the communications equipment should be less than 300 m. This length can be increased to 1000 m or 200 nF total cable capacitance if the communications cable is not close to high current-carrying conductors.

Earth (ground) the cable screen at one end only.

Table 6 - K-bus or IEC60870-5-2 over EIA(RS)485 pin allocations

A typical cable specification would be:

Each core:	16/0.2mm copper conductors PVC insulated
Nominal conductor area:	0.5mm2 per core
Screen:	Overall braid, PVC sheathed

3.10 Protective Conductor (Earth) Connection

Every relay must be connected to the local earth (ground) bar using the M4 earth (ground) studs in the bottom left hand corner of the relay case. The minimum recommended wire size is 2.5 mm^2 and should have a ring terminal at the relay end. Due to the limitations of the ring terminal, the maximum wire size that can be used for any of the medium or heavy duty terminals is 6.0 mm^2 per wire. If a greater cross-sectional area is required, two parallel connected wires, each terminated in a separate ring terminal at the relay, or a metal earth (ground) bar could be used.

Note	*To prevent any possibility of electrolytic action between brass or copper earth (ground) conductors and the rear panel of the relay, precautions should be taken to isolate them from one another. This could be achieved in several ways, including placing a nickel-plated or insulating washer between the conductor and the relay case, or using tinned ring terminals.*

4 P64X CASE DIMENSIONS

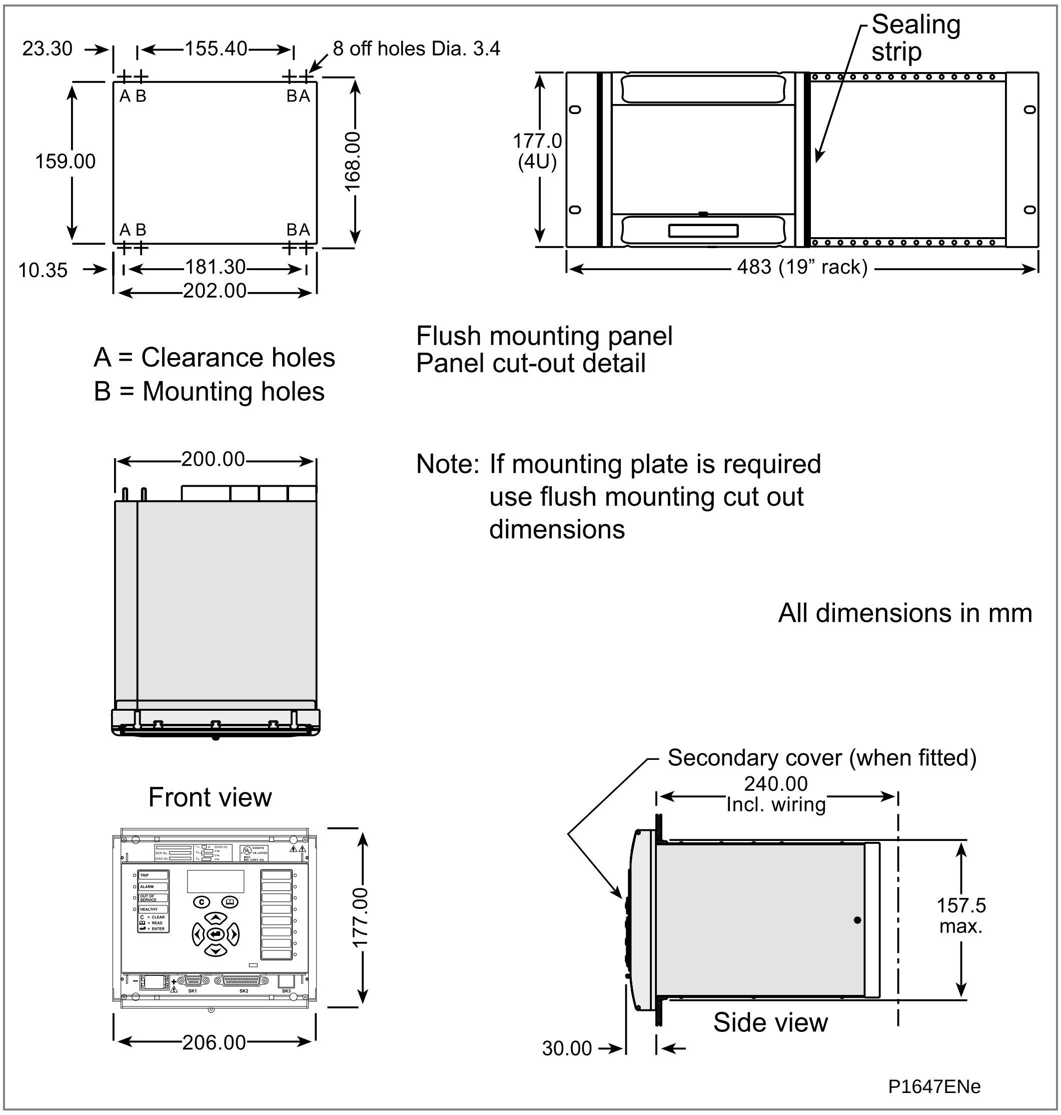

23.30
155.40
8 off holes Dia. 3.4
A B
B A
159.00
168.00
A B
B A
10.35
181.30
202.00
A = Clearance holes
B = Mounting holes
Sealing strip
177.0 (4U)
483 (19” rack)
Flush mounting panel
Panel cut-out detail
200.00
Note: If mounting plate is required use flush mounting cut out dimensions
All dimensions in mm
Front view
177.00
206.00
Secondary cover (when fitted)
240.00 Incl. wiring
157.5 max.
Side view
30.00
P1647ENe

Figure 3 - P642 case dimensions (40TE case)

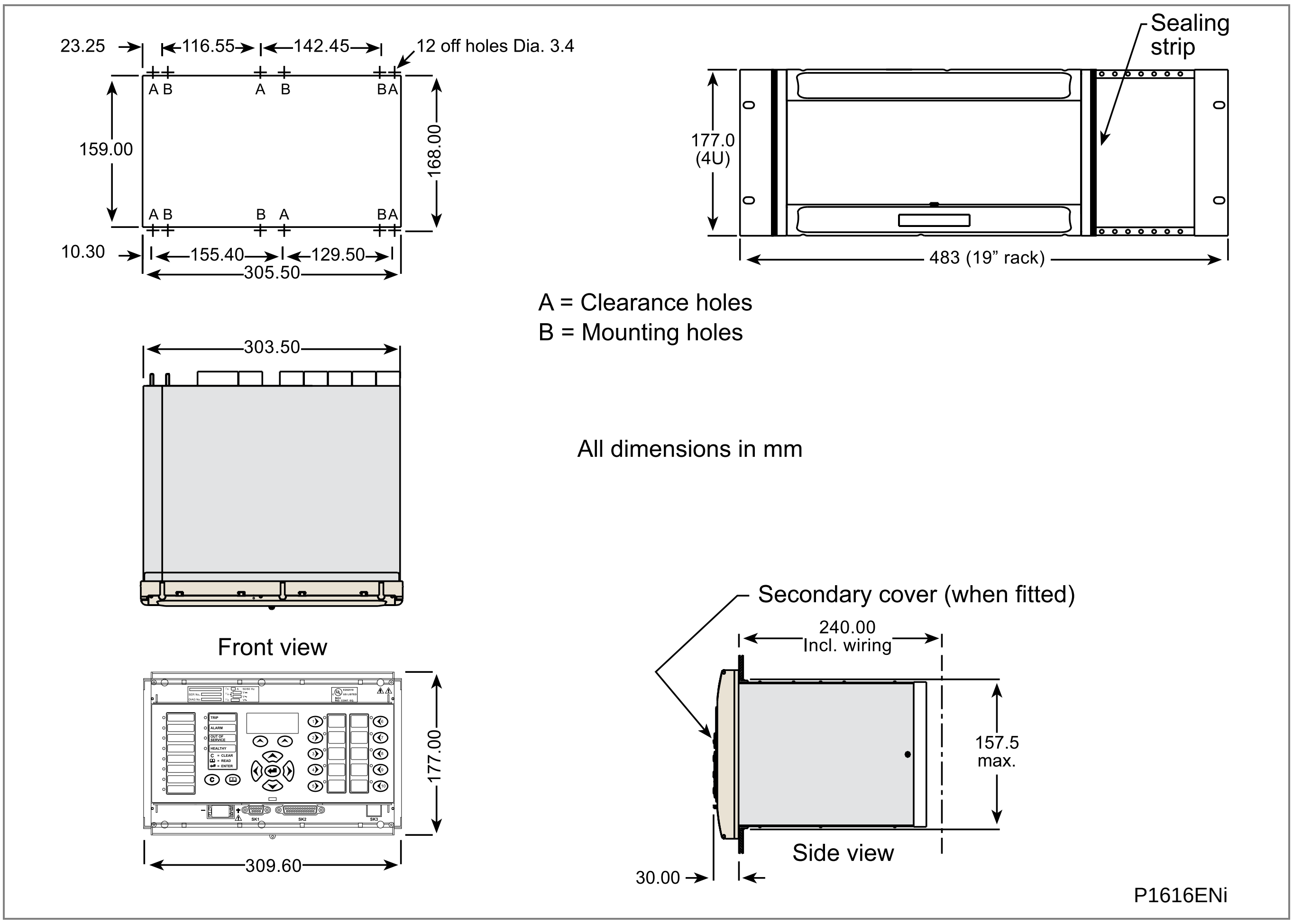

23.25
116.55
142.45
12 off holes Dia. 3.4
A B
A B
B A
159.00
168.00
A B
B A
B A
10.30
155.40
129.50
305.50
A = Clearance holes
B = Mounting holes
303.50
All dimensions in mm
Sealing strip
177.0 (4U)
483 (19" rack)
Front view
177.00
309.60
Secondary cover (when fitted)
240.00 Incl. wiring
157.5 max.
Side view
30.00
P1616ENi

Figure 4 - P643 case dimensions (60TE case)

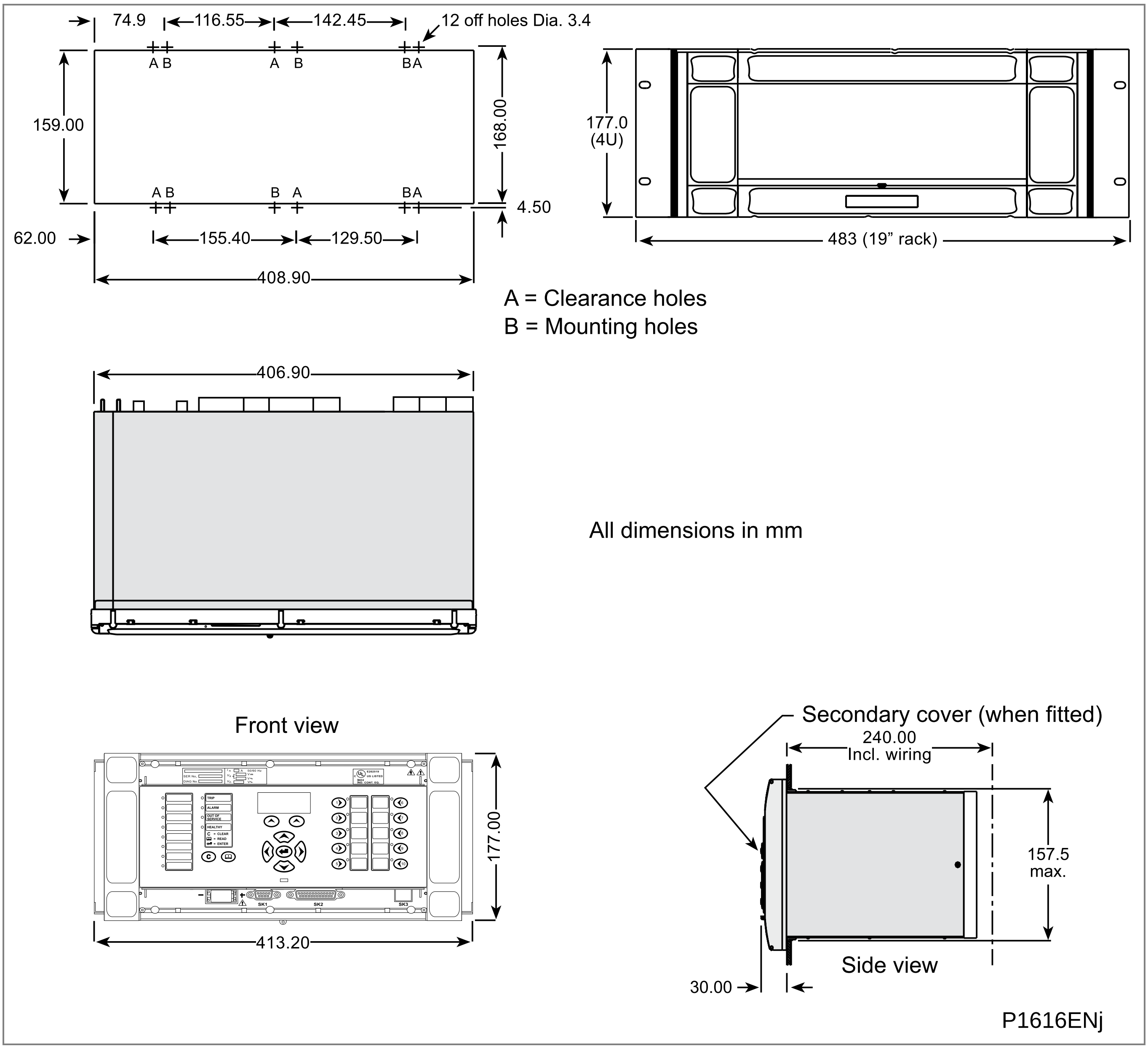

74.9
116.55
142.45
12 off holes Dia. 3.4
A B
A B
B A
159.00
168.00
A B
B A
B A
4.50
62.00
155.40
129.50
408.90
177.0
(4U)
483 (19" rack)
A = Clearance holes
B = Mounting holes
406.90
All dimensions in mm
Front view
TRIP
ALARM
OUT OF SERVICE
HEALTHY
C = CLEAR
= READ
= ENTER
SK1
SK2
SK3
177.00
413.20
Secondary cover (when fitted)
240.00
Incl. wiring
157.5
max.
Side view
30.00
P1616ENj

Figure 5 - P645 case dimensions (80TE case)

P64X EXTERNAL CONNECTION DIAGRAMS

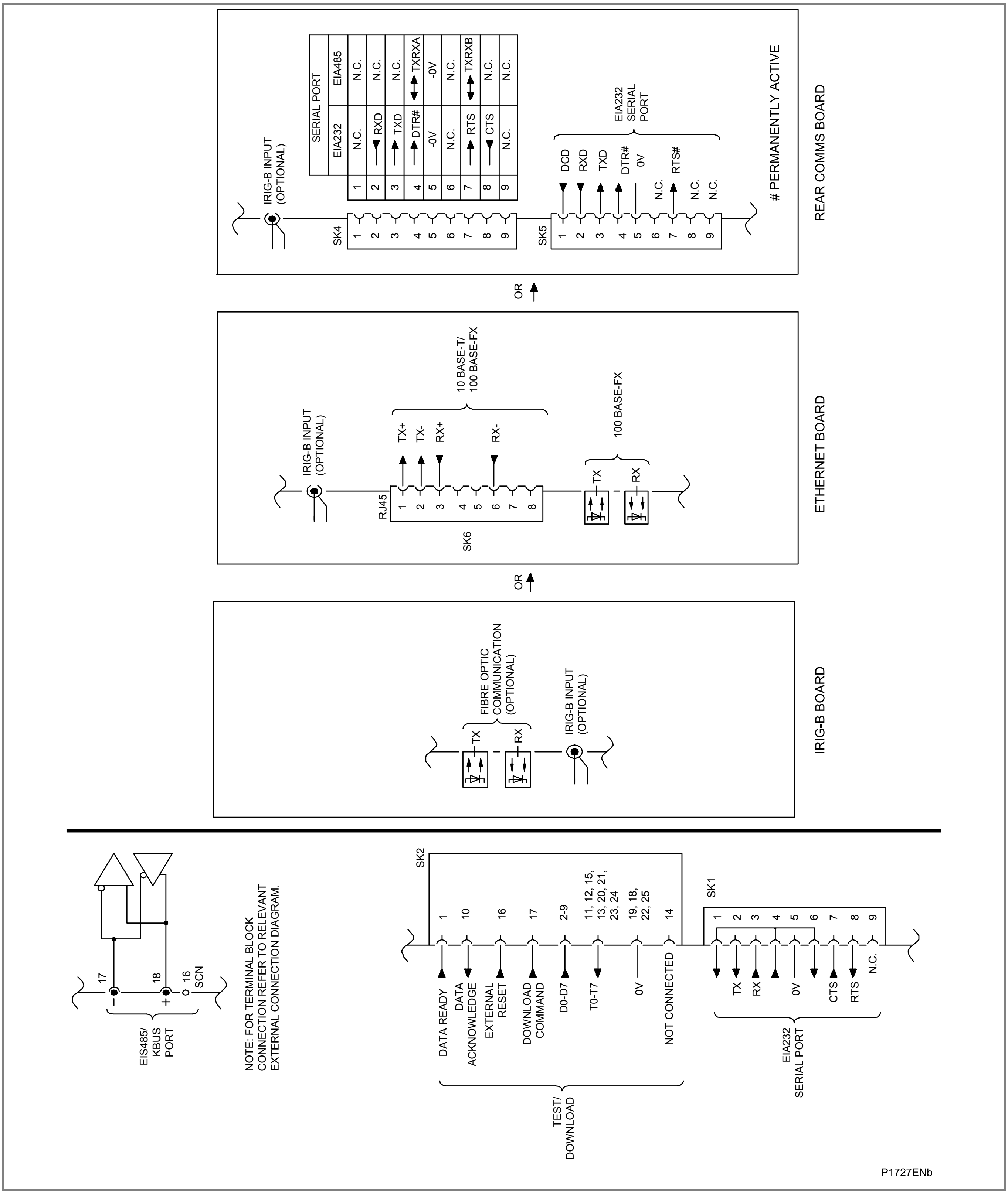

REAR COMMS BOARD
IRIG-B INPUT (OPTIONAL)
SERIAL PORT
EIA232
EIA485
N.C.
RXD
TXD
DTR#
-0V
RTS
CTS
TXRXA
TXRXB
SK4
SK5
EIA232 SERIAL PORT
DCD
0V
RTS#
# PERMANENTLY ACTIVE
OR
ETHERNET BOARD
10 BASE-T/ 100 BASE-FX
100 BASE-FX
TX+
TX-
RX+
RX-
TX
RX
RJ45
SK6
IRIG-B BOARD
FIBRE OPTIC COMMUNICATION (OPTIONAL)
SK2
DATA READY
DATA ACKNOWLEDGE
EXTERNAL RESET
DOWNLOAD COMMAND
D0-D7
T0-T7
NOT CONNECTED
11, 12, 15, 13, 20, 21, 23, 24
19, 18, 22, 25
TEST/ DOWNLOAD
SK1
CTS
RTS
EIA232 SERIAL PORT
EIS485/ KBUS PORT
SCN
NOTE: FOR TERMINAL BLOCK CONNECTION REFER TO RELEVANT EXTERNAL CONNECTION DIAGRAM.
P1727ENb

Figure 6 - Comms. Options MiCOM Px40 platform

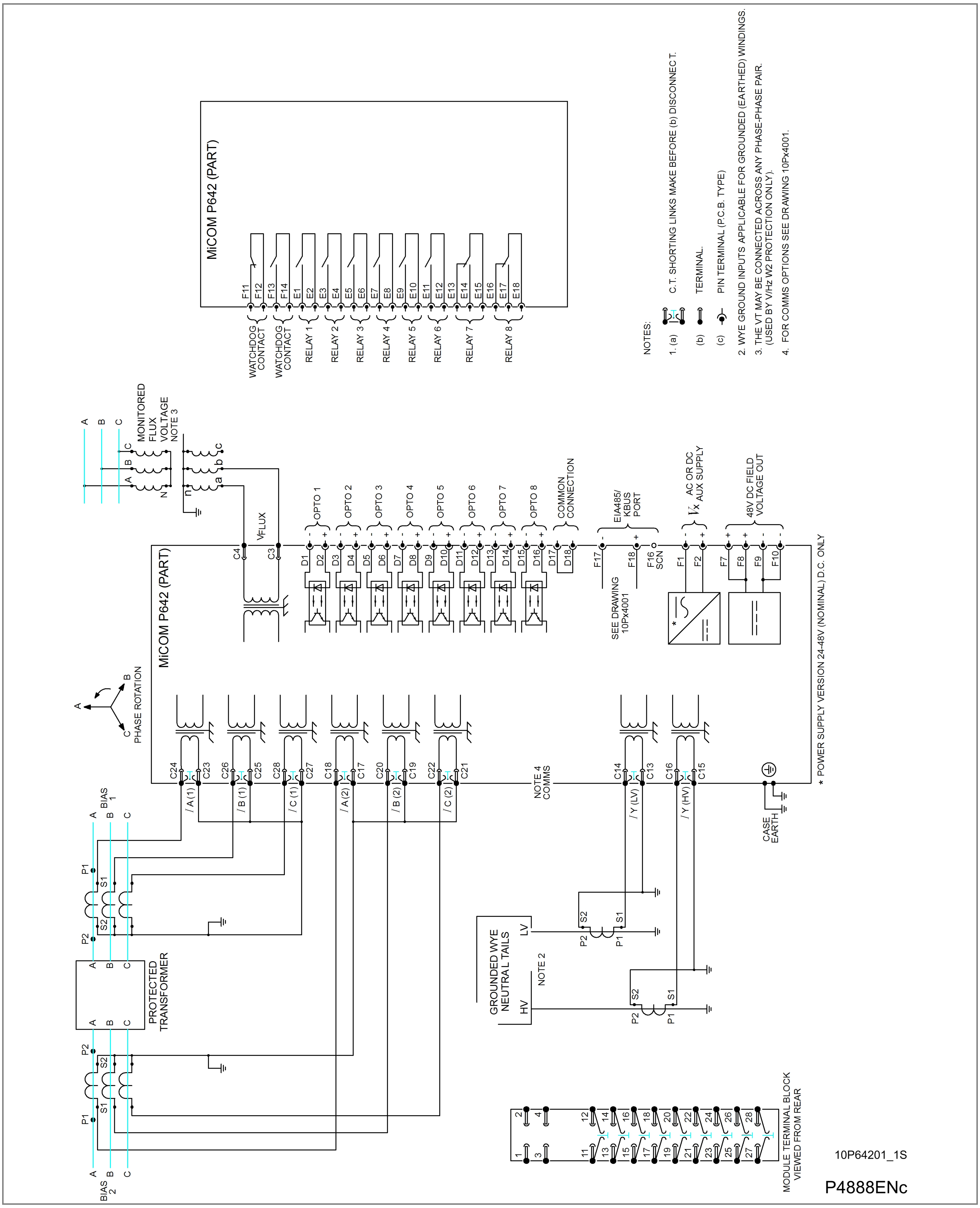

MiCOM P642 (PART)
F11
F12
F13
F14
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
E11
E12
E13
E14
E15
E16
E17
E18
WATCHDOG CONTACT
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
NOTES:
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
(b) TERMINAL.
(c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
A
B
C
MONITORED FLUX VOLTAGE NOTE 3
A
B
C
N
a
b
c
n
VFLUX
C4
C3
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
EIA485/ KBUS PORT
F17
F18
F16 SCN
SEE DRAWING 10Px4001
AC OR DC AUX SUPPLY
Vx
F1
F2
48V DC FIELD VOLTAGE OUT
F7
F8
F9
F10
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
MiCOM P642 (PART)
A
B
C
PHASE ROTATION
C24
C23
C26
C25
C28
C27
C18
C17
C20
C19
C22
C21
NOTE 4 COMMS
C14
C13
C16
C15
CASE EARTH
/ A (1)
/ B (1)
/ C (1)
/ A (2)
/ B (2)
/ C (2)
/ Y (LV)
/ Y (HV)
BIAS 1
A
B
C
P1
S1
S2
P2
PROTECTED TRANSFORMER
A
B
C
A
B
C
P2
S2
S1
P1
A
B
C
BIAS 2
GROUNDED WYE NEUTRAL TAILS
LV
HV
NOTE 2
S2
S1
P2
P1
S2
S1
P2
P1
2
4
1
3
12
14
16
18
20
22
24
26
28
11
13
15
17
19
21
23
25
27
MODULE TERMINAL BLOCK VIEWED FROM REAR
10P64201_1S
P4888ENc

Figure 7 - Two bias input transformer differential (8 I/P & 8 O/P) with 1 pole VT input (40TE)

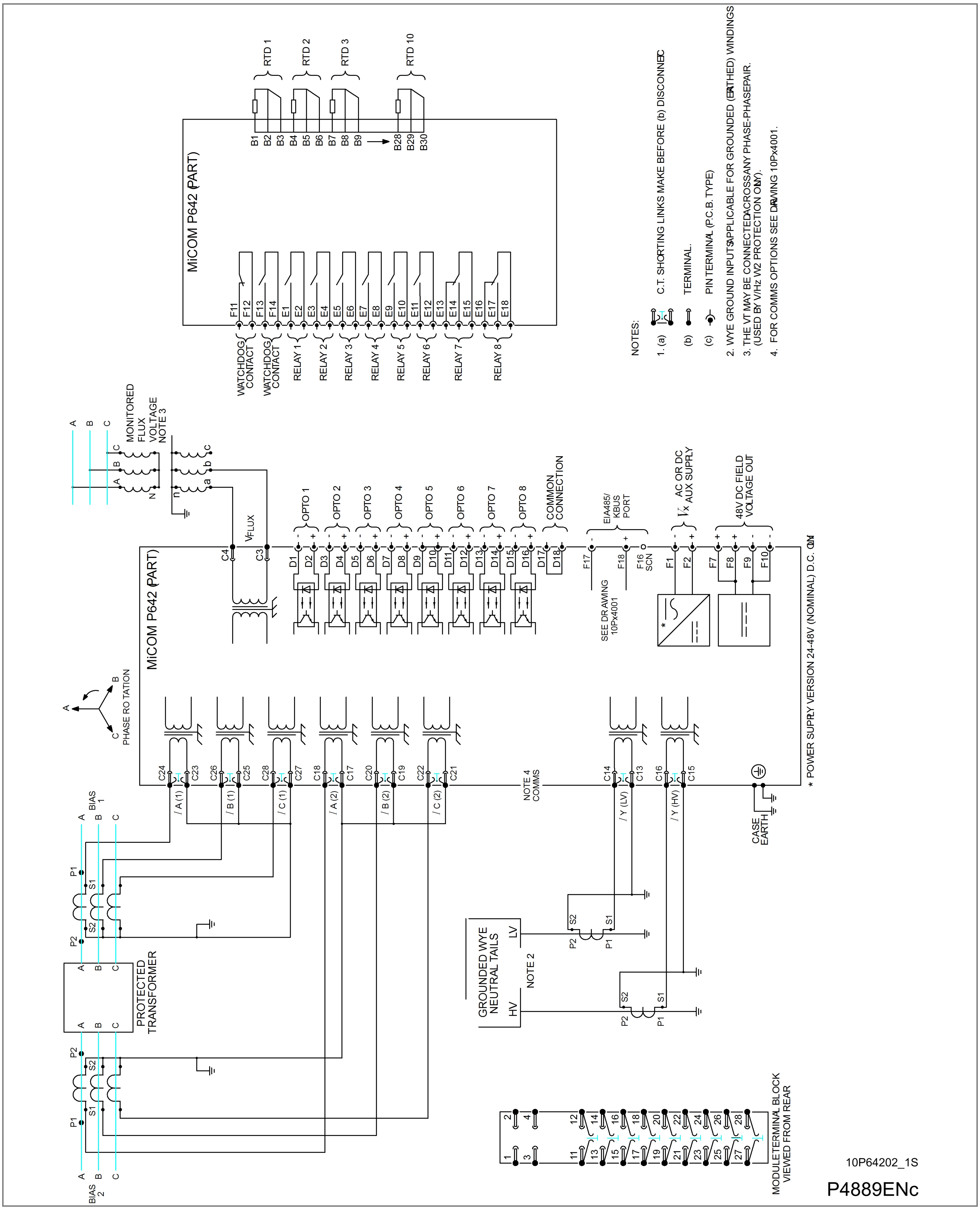

MiCOM P642 (PART)
RTD 1
RTD 2
RTD 3
RTD 10
B1 B2 B3 B4 B5 B6 B7 B8 B9 B28 B29 B30
F11 F12 F13 F14 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18
WATCHDOG CONTACT
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
NOTES:
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECTS
(b) TERMINAL.
(c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
A B C
MONITORED FLUX VOLTAGE NOTE 3
N n a b c
V FLUX
C4 C3
MiCOM P642 (PART)
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
EIA485/ KBUS PORT
F17 F18 F16 SCN
SEE DRAWING 10Px4001
AC OR DC AUX SUPPLY
Vx
F1 F2
48V DC FIELD VOLTAGE OUT
F7 F8 F9 F10
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
PHASE ROTATION
A B C
C24 C23 C26 C25 C28 C27 C18 C17 C20 C19 C22 C21
/ A (1)
/ B (1)
/ C (1)
/ A (2)
/ B (2)
/ C (2)
NOTE 4 COMMS
C14 C13 C16 C15
/ Y (LV)
/ Y (HV)
CASE EARTH
BIAS 1
BIAS 2
P1 P2 S1 S2
PROTECTED TRANSFORMER
GROUNDED WYE NEUTRAL TAILS
LV
HV
NOTE 2
1 2 3 4 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28
MODULE TERMINAL BLOCK VIEWED FROM REAR
10P64202_1S
P4889ENc

Figure 8 - Two bias input transformer differential (8 I/P & 8 O/P + RTD) with 1 pole VT input (40TE)

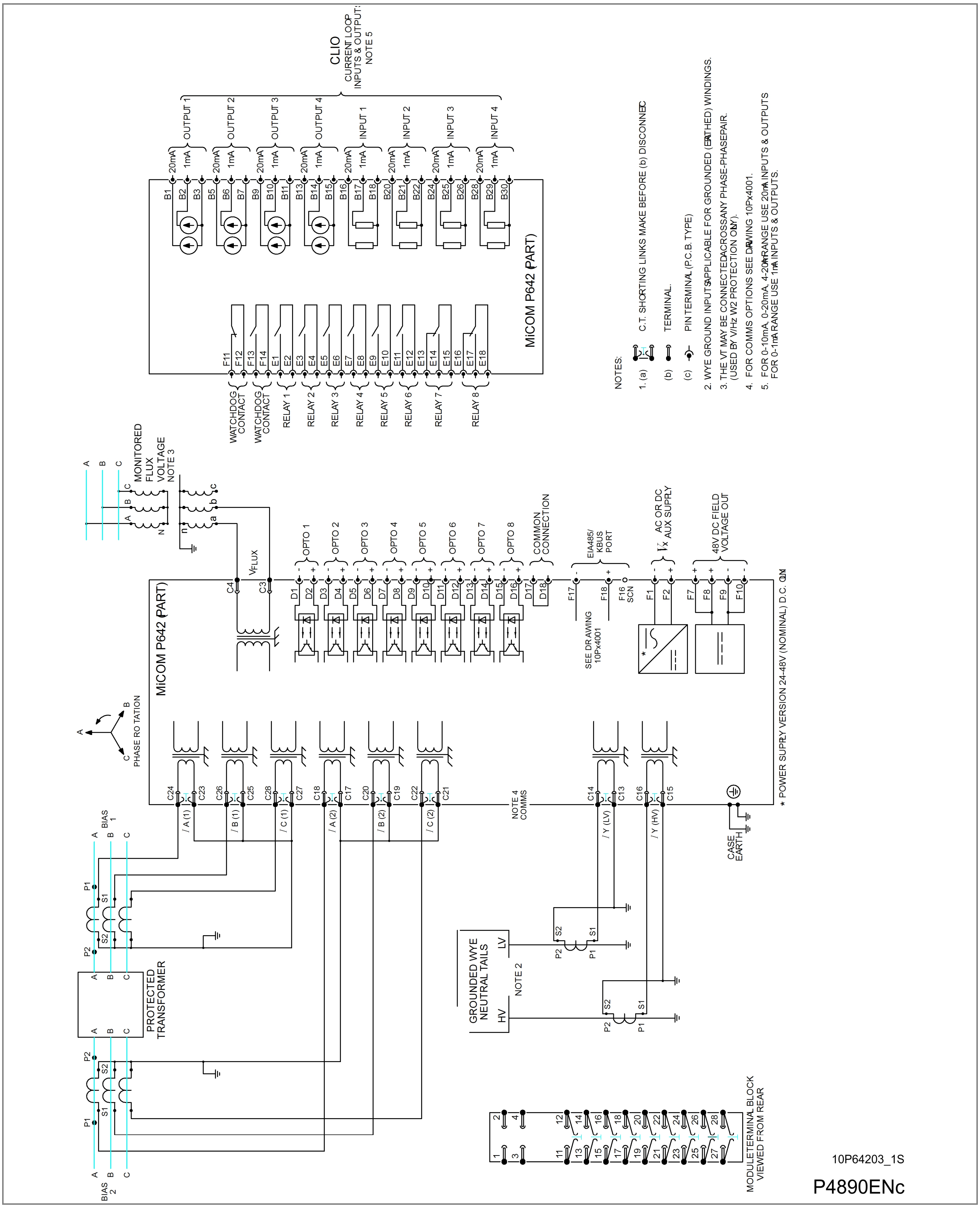

CLIO
CURRENT LOOP INPUTS & OUTPUTS
NOTE 5
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
INPUT 1
INPUT 2
INPUT 3
INPUT 4
20mA
1mA
B1 B2 B3 B5 B6 B7 B9 B10 B11 B13 B14 B15 B16 B17 B18 B20 B21 B22 B24 B25 B26 B28 B29 B30
MiCOM P642 (PART)
F11 F12 F13 F14 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18
WATCHDOG CONTACT
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
NOTES:
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT
(b) TERMINAL.
(c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
5. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.
A B C
MONITORED FLUX VOLTAGE NOTE 3
A B C N
a b c n
V_{FLUX}
C4 C3
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18
EIA485/ KBUS PORT
F17 F18 F16 SCN
SEE DRAWING 10Px4001
V_x AC OR DC AUX SUPPLY
F1 F2
48V DC FIELD VOLTAGE OUT
F7 F8 F9 F10
MiCOM P642 (PART)
PHASE ROTATION
A B C
C24 C23 C26 C25 C28 C27 C18 C17 C20 C19 C22 C21
/ A (1)
/ B (1)
/ C (1)
/ A (2)
/ B (2)
/ C (2)
NOTE 4 COMMS
C14 C13 C16 C15
/ Y (LV)
/ Y (HV)
CASE EARTH
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
BIAS 1
P1 S1 S2 P2
PROTECTED TRANSFORMER
BIAS 2
GROUNDED WYE NEUTRAL TAILS
LV
HV
NOTE 2
MODULE TERMINAL BLOCK VIEWED FROM REAR
1 2 3 4 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28
10P64203_1S
P4890ENc

Figure 9 - Two bias input transformer differential (8 I/P & 8 O/P + CLIO) with 1 pole VT input (40TE)

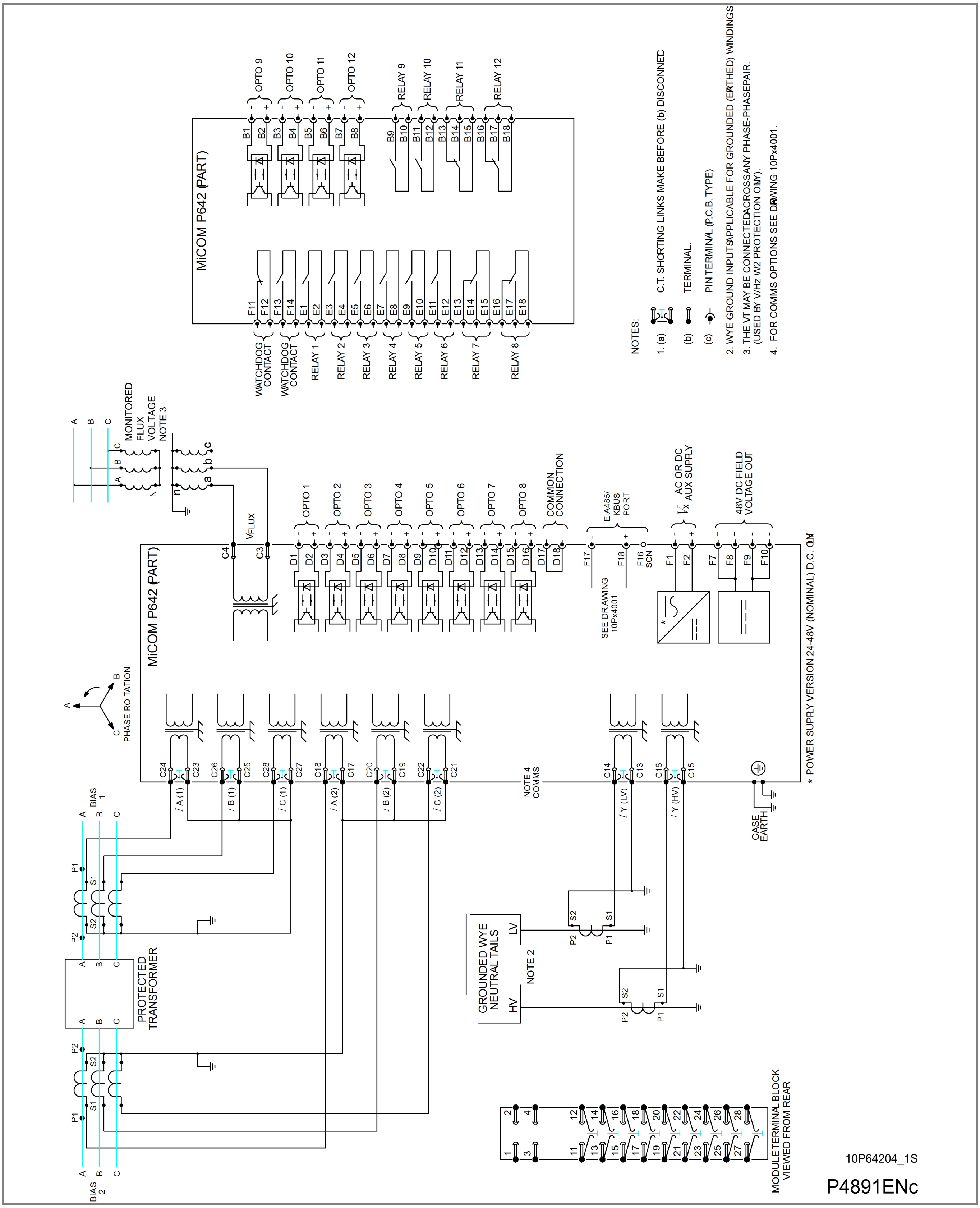

MiCOM P642 (PART)
OPTO 9
OPTO 10
OPTO 11
OPTO 12
RELAY 9
RELAY 10
RELAY 11
RELAY 12
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18
F11 F12 F13 F14 E1 E2 E3 E4 E5 E6 E7 E8 E9 E10 E11 E12 E13 E14 E15 E16 E17 E18
WATCHDOG CONTACT
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
NOTES:
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECTS.
(b) TERMINAL.
(c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
A B C
MONITORED FLUX VOLTAGE NOTE 3
N n a b c
V_{FLUX}
C4 C3
MiCOM P642 (PART)
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
EIA485/ KBUS PORT
F17 F18 F16 SCN
SEE DRAWING 10Px4001
V_x AC OR DC AUX SUPPLY
F1 F2
48V DC FIELD VOLTAGE OUT
F7 F8 F9 F10
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
PHASE ROTATION
A B C
C24 C23 C26 C25 C28 C27 C18 C17 C20 C19 C22 C21
/ A (1)
/ B (1)
/ C (1)
/ A (2)
/ B (2)
/ C (2)
NOTE 4 COMMS
C14 C13 C16 C15
/ Y (LV)
/ Y (HV)
CASE EARTH
BIAS 1
BIAS 2
P1 P2 S1 S2
PROTECTED TRANSFORMER
GROUNDED WYE NEUTRAL TAILS
LV
HV
NOTE 2
1 2 3 4 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28
MODULE TERMINAL BLOCK VIEWED FROM REAR
10P64204_1S
P4891ENc

Figure 10 - Two bias input transformer differential (12 I/P & 12 O/P) with 1 pole VT input (40TE)

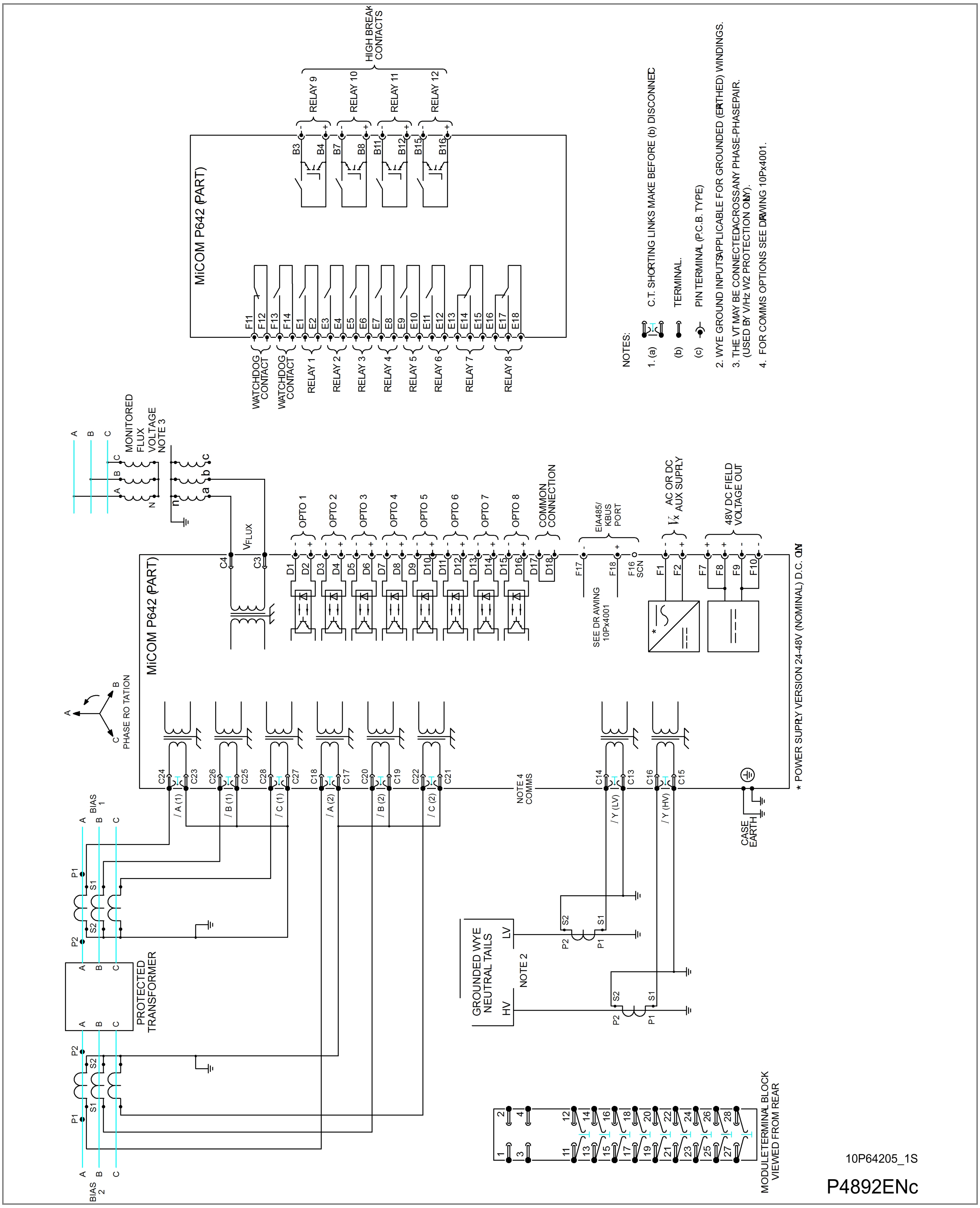
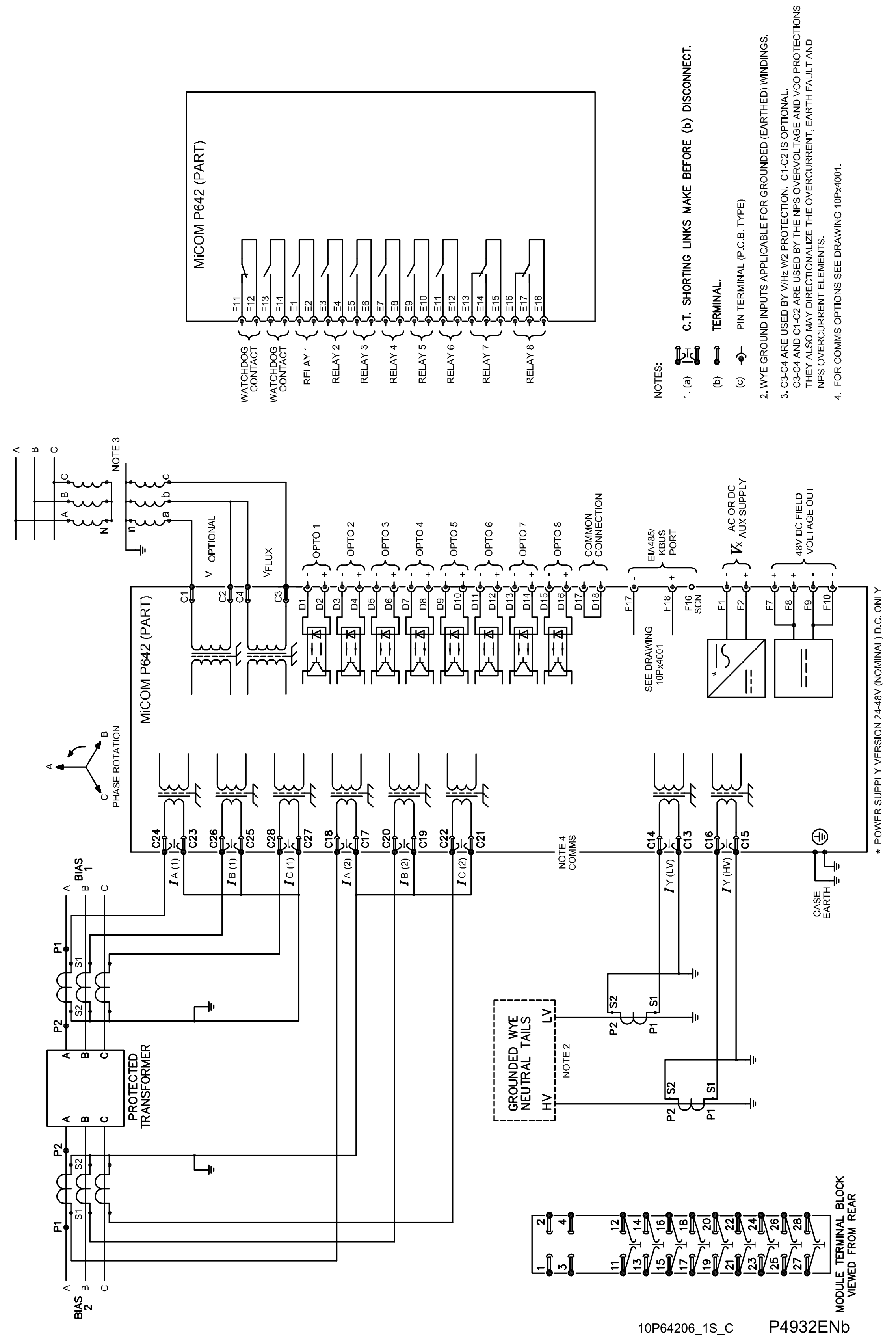

MiCOM P642 (PART)
HIGH BREAK CONTACTS
RELAY 9
RELAY 10
RELAY 11
RELAY 12
WATCHDOG CONTACT
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
MONITORED FLUX VOLTAGE NOTE 3
VFLUX
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
EIA485/ KBUS PORT
SEE DRAWING 10Px4001
SCN
AC OR DC AUX SUPPLY
Vx
48V DC FIELD VOLTAGE OUT
PHASE ROTATION
BIAS 1
BIAS 2
PROTECTED TRANSFORMER
/ A (1)
/ B (1)
/ C (1)
/ A (2)
/ B (2)
/ C (2)
NOTE 4 COMMS
/ Y (LV)
/ Y (HV)
CASE EARTH
GROUNDED WYE NEUTRAL TAILS
NOTE 2
LV
HV
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
NOTES:
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
(b) TERMINAL.
(c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
MODULE TERMINAL BLOCK VIEWED FROM REAR
10P64205_1S
P4892ENc

Figure 11 - Two bias input transformer differential (8 I/P & 12 O/P) with 1 pole input (40TE)



MiCOM P642 (PART)
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
F11
F12
F13
F14
E1
E2
E3
E4
E5
E6
E7
E8
E9
E10
E11
E12
E13
E14
E15
E16
E17
E18
A
B
C
N
n
a
b
c
NOTE 3
V OPTIONAL
VFLUX
C1
C2
C4
C3
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
EIA485/ KBUS PORT
F17
F18
F16 SCN
SEE DRAWING 10Px4001
AC OR DC AUX SUPPLY
Vx
F1
F2
48V DC FIELD VOLTAGE OUT
F7
F8
F9
F10
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
PHASE ROTATION
C24
C23
C26
C25
C28
C27
C18
C17
C20
C19
C22
C21
C14
C13
C16
C15
IA (1)
IB (1)
IC (1)
IA (2)
IB (2)
IC (2)
IY (LV)
IY (HV)
NOTE 4 COMMS
CASE EARTH
BIAS 1
BIAS 2
P1
P2
S1
S2
PROTECTED TRANSFORMER
GROUNDED WYE NEUTRAL TAILS
LV
HV
NOTE 2
1
2
3
4
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
MODULE TERMINAL BLOCK VIEWED FROM REAR
10P64206_1S_C
P4932ENb

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.

   (b) TERMINAL.

   (c) PIN TERMINAL (P.C.B. TYPE)

2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. C3-C4 ARE USED BY V/Hz W2 PROTECTION. C1-C2 IS OPTIONAL. C3-C4 AND C1-C2 ARE USED BY THE NPS OVERVOLTAGE AND VCO PROTECTIONS. THEY ALSO MAY DIRECTIONALIZE THE OVERCURRENT, EARTH FAULT AND NPS OVERCURRENT ELEMENTS.
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

Figure 12 - Two bias input transformer differential (8 I/P & 8 O/P) with 2 pole VT inputs (40TE)

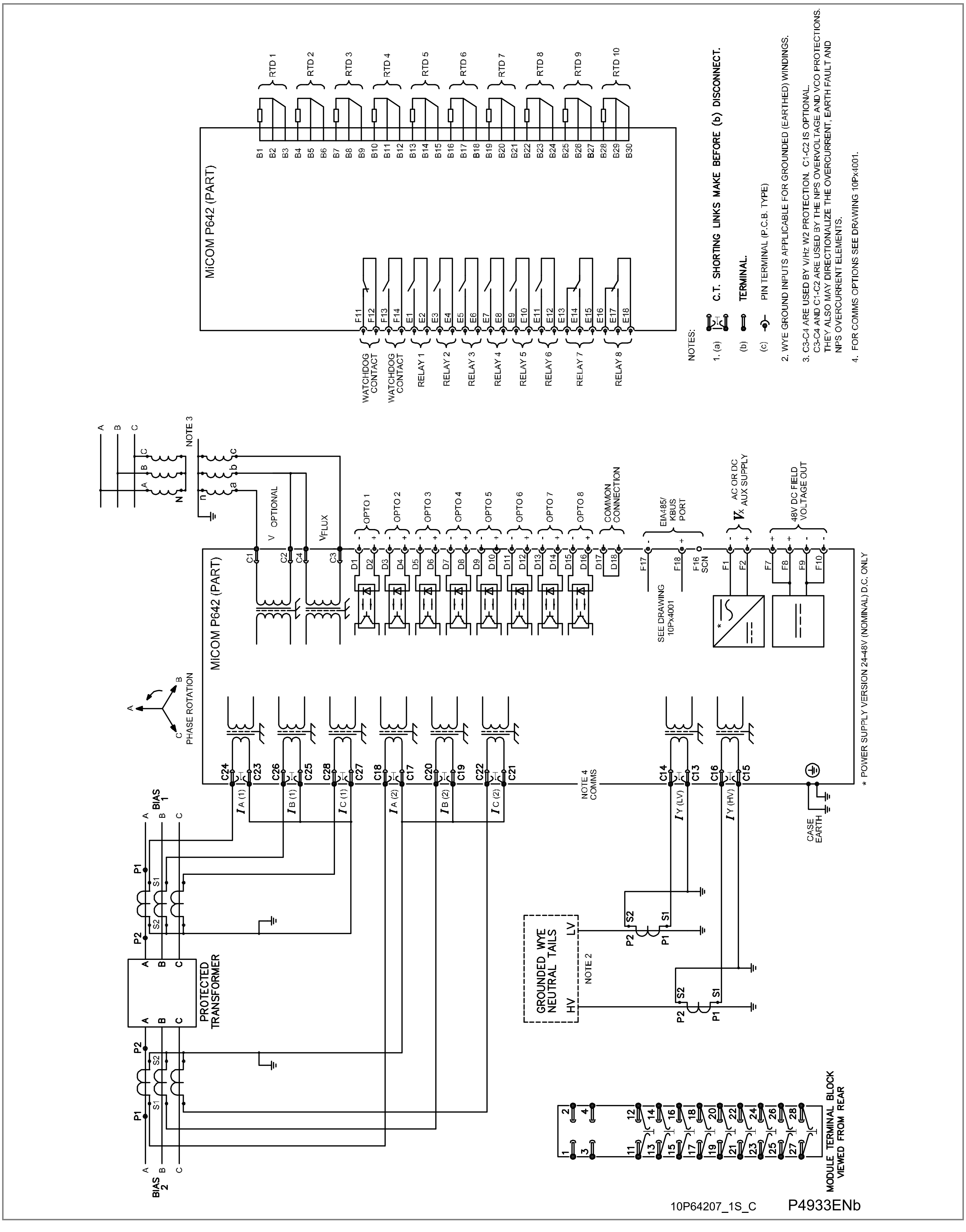
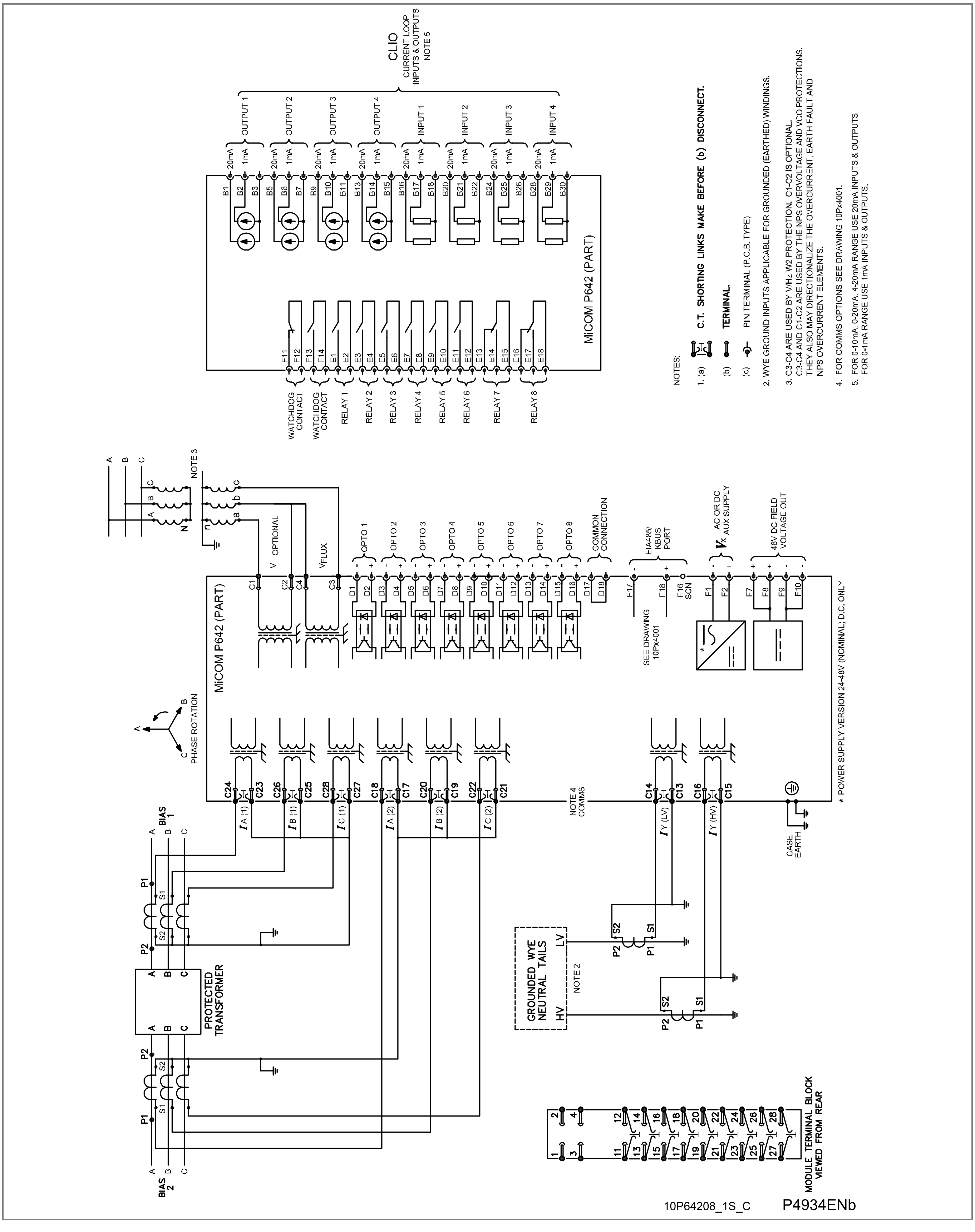

MiCOM P642 (PART)
RTD 1
RTD 2
RTD 3
RTD 4
RTD 5
RTD 6
RTD 7
RTD 8
RTD 9
RTD 10
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
NOTE 3
V OPTIONAL
VFLUX
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
EIA485/ KBUS PORT
SEE DRAWING 10Px4001
F16 SCN
AC OR DC AUX SUPPLY
Vx
48V DC FIELD VOLTAGE OUT
PHASE ROTATION
BIAS 1
BIAS 2
PROTECTED TRANSFORMER
NOTE 4 COMMS
IA (1)
IB (1)
IC (1)
IA (2)
IB (2)
IC (2)
IY (LV)
IY (HV)
CASE EARTH
GROUNDED WYE NEUTRAL TAILS
LV
HV
NOTE 2
P1
P2
S1
S2
NOTES:
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
(b) TERMINAL.
(c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. C3-C4 ARE USED BY V/Hz W2 PROTECTION. C1-C2 IS OPTIONAL.
C3-C4 AND C1-C2 ARE USED BY THE NPS OVERVOLTAGE AND VCO PROTECTIONS. THEY ALSO MAY DIRECTIONALIZE THE OVERCURRENT, EARTH FAULT AND NPS OVERCURRENT ELEMENTS.
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
MODULE TERMINAL BLOCK VIEWED FROM REAR
10P64207_1S_C
P4933ENb

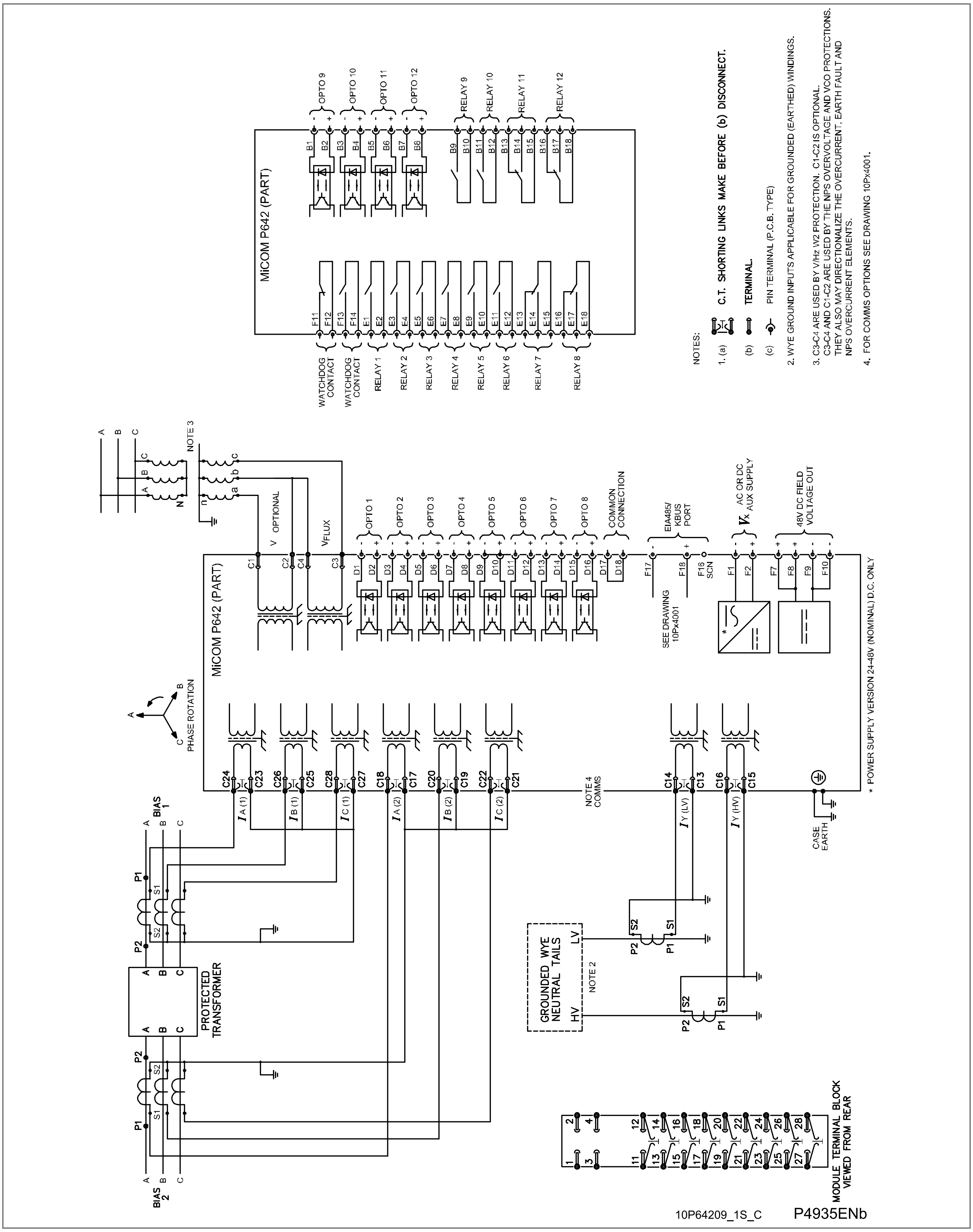
Figure 13 - Two bias input transformer differential (8 I/P & 8 O/P + RTD) with 2 pole VT inputs (40TE)


CLIO
CURRENT LOOP INPUTS & OUTPUTS
NOTE 5
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
INPUT 1
INPUT 2
INPUT 3
INPUT 4
20mA
1mA
MiCOM P642 (PART)
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
NOTE 3
V OPTIONAL
VFLUX
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
EIA485/ KBUS PORT
SEE DRAWING 10Px4001
F16 SCN
Vx AC OR DC AUX SUPPLY
48V DC FIELD VOLTAGE OUT
PHASE ROTATION
NOTE 4 COMMS
CASE EARTH
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
BIAS 1
BIAS 2
PROTECTED TRANSFORMER
GROUNDED WYE NEUTRAL TAILS
NOTE 2
LV
HV
IA (1)
IB (1)
IC (1)
IA (2)
IB (2)
IC (2)
IY (LV)
IY (HV)
MODULE TERMINAL BLOCK VIEWED FROM REAR
10P64208_1S_C
P4934ENb

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. C3-C4 ARE USED BY V/Hz W2 PROTECTION. C1-C2 IS OPTIONAL. C3-C4 AND C1-C2 ARE USED BY THE NPS OVERVOLTAGE AND VCO PROTECTIONS. THEY ALSO MAY DIRECTIONALIZE THE OVERCURRENT, EARTH FAULT AND NPS OVERCURRENT ELEMENTS.
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
5. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Figure 14 - Two bias input transformer differential (8 I/P & 8 O/P + CLIO) with 2 pole VT inputs (40TE)


MiCOM P642 (PART)
OPTO 9
OPTO 10
OPTO 11
OPTO 12
RELAY 9
RELAY 10
RELAY 11
RELAY 12
WATCHDOG CONTACT
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
NOTE 3
V OPTIONAL
VFLUX
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
EIA485/ KBUS PORT
SEE DRAWING 10Px4001
AC OR DC AUX SUPPLY
48V DC FIELD VOLTAGE OUT
PHASE ROTATION
IA (1)
IB (1)
IC (1)
IA (2)
IB (2)
IC (2)
IY (LV)
IY (HV)
NOTE 4 COMMS
CASE EARTH
BIAS 1
BIAS 2
PROTECTED TRANSFORMER
GROUNDED WYE NEUTRAL TAILS
NOTE 2
HV
LV
MODULE TERMINAL BLOCK VIEWED FROM REAR
10P64209_1S_C
P4935ENb

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.

(b) TERMINAL.

(c) PIN TERMINAL (P.C.B. TYPE)

2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.

3. C3-C4 ARE USED BY V/Hz W2 PROTECTION. C1-C2 IS OPTIONAL. C3-C4 AND C1-C2 ARE USED BY THE NPS OVERVOLTAGE AND VCO PROTECTIONS. THEY ALSO MAY DIRECTIONALIZE THE OVERCURRENT, EARTH FAULT AND NPS OVERCURRENT ELEMENTS.

4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY

Figure 15 - Two bias input transformer differential (12 I/P & 12 O/P) with 2 pole VT inputs (40TE)

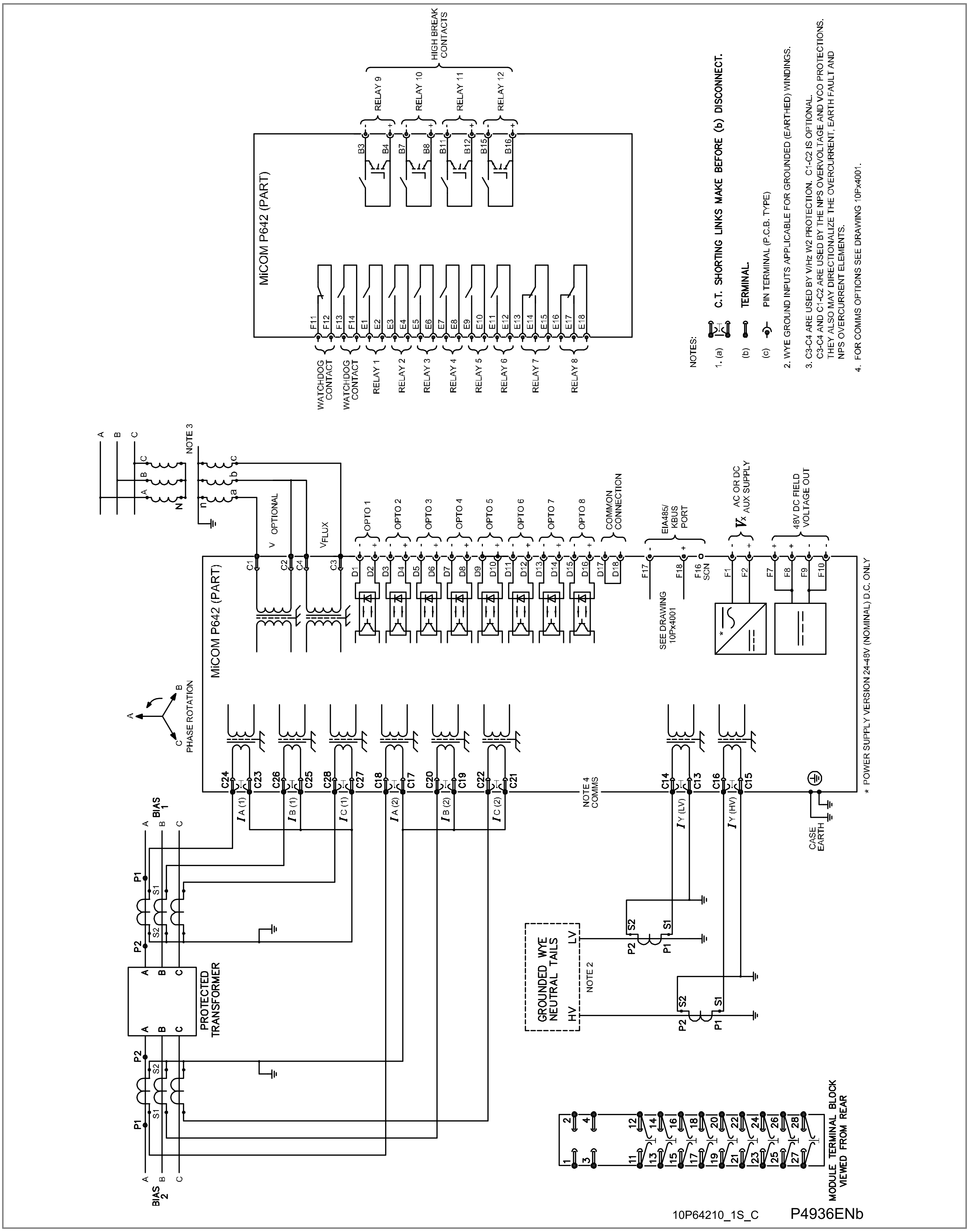

MiCOM P642 (PART)
HIGH BREAK CONTACTS
RELAY 9
RELAY 10
RELAY 11
RELAY 12
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
NOTE 3
V OPTIONAL
VFLUX
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
EIA485/ KBUS PORT
SEE DRAWING 10Px4001
SCN
AC OR DC AUX SUPPLY
Vx
48V DC FIELD VOLTAGE OUT
PHASE ROTATION
BIAS 1
BIAS 2
PROTECTED TRANSFORMER
IA (1)
IB (1)
IC (1)
IA (2)
IB (2)
IC (2)
NOTE 4 COMMS
IY (LV)
IY (HV)
CASE EARTH
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
GROUNDED WYE NEUTRAL TAILS
NOTE 2
LV
HV
MODULE TERMINAL BLOCK VIEWED FROM REAR
NOTES:
1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
(b) TERMINAL.
(c) PIN TERMINAL (P.C.B. TYPE)
2. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
3. C3-C4 ARE USED BY V/Hz W2 PROTECTION. C1-C2 IS OPTIONAL. C3-C4 AND C1-C2 ARE USED BY THE NPS OVERVOLTAGE AND VCO PROTECTIONS. THEY ALSO MAY DIRECTIONALIZE THE OVERCURRENT, EARTH FAULT AND NPS OVERCURRENT ELEMENTS.
4. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
10P64210_1S_C
P4936ENb

Figure 16 - Two bias input transformer differential (8 I/P & 12 O/P) with 2 pole inputs (40TE)

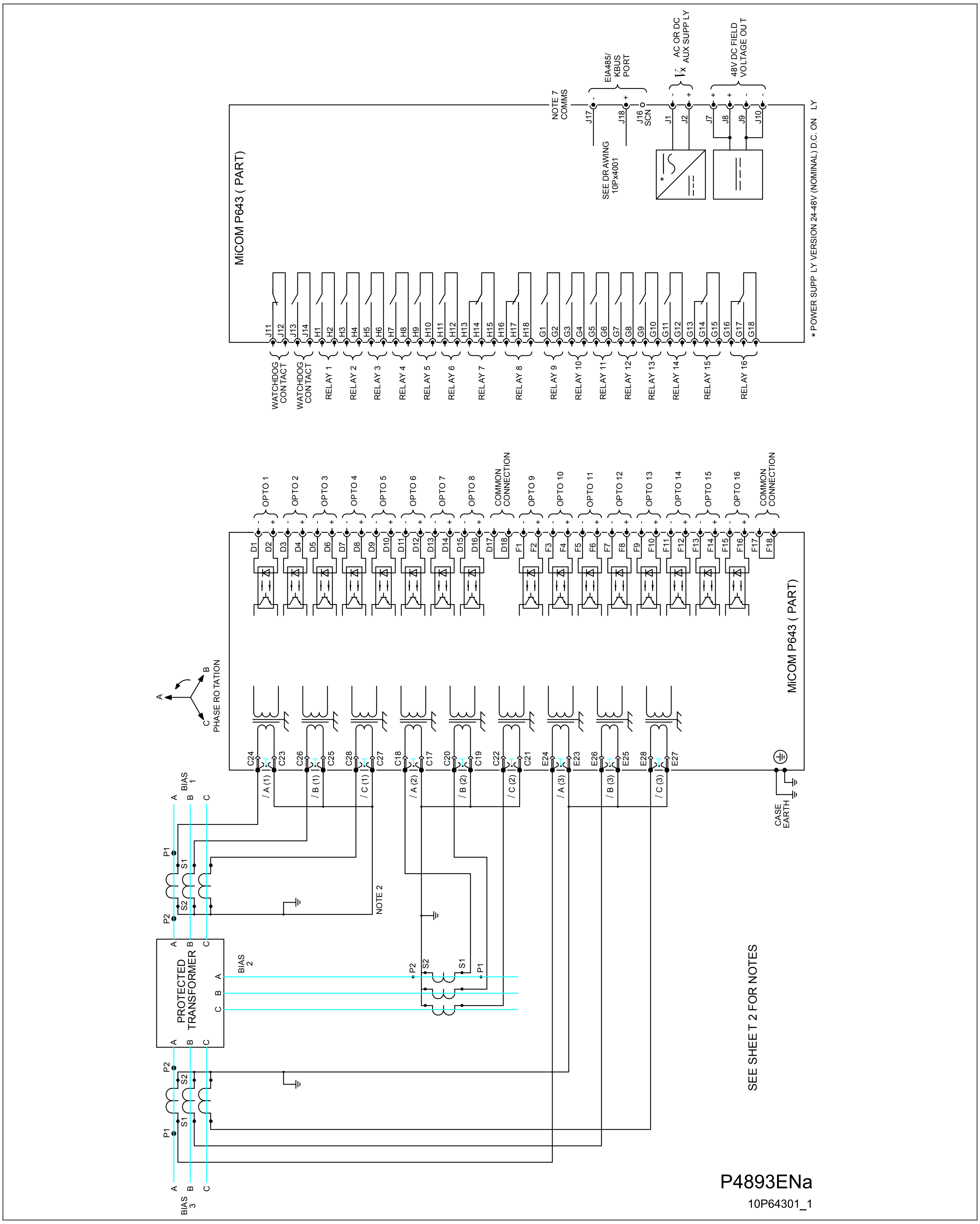
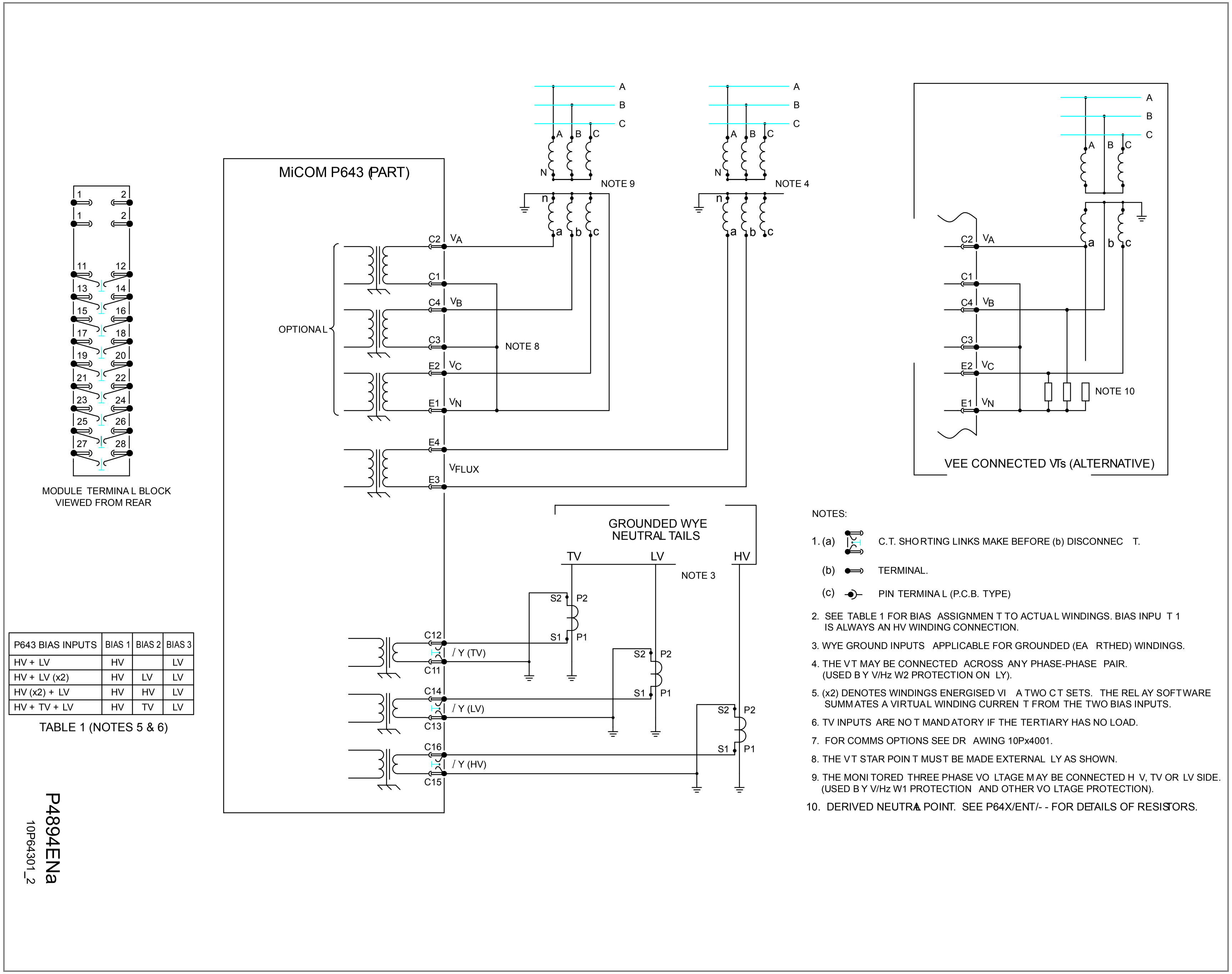

MiCOM P643 (PART)
NOTE 7 COMMS
EIA485/ KBUS PORT
J17 -
J18 +
J16 SCN
SEE DRAWING 10Px4001
AC OR DC AUX SUPPLY
J1 -
J2 +
48V DC FIELD VOLTAGE OUT
J7 +
J8 +
J9 -
J10 -
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
WATCHDOG CONTACT
J11 J12
WATCHDOG CONTACT
J13 J14
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
RELAY 9
RELAY 10
RELAY 11
RELAY 12
RELAY 13
RELAY 14
RELAY 15
RELAY 16
H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13 H14 H15 H16 H17 H18
G1 G2 G3 G4 G5 G6 G7 G8 G9 G10 G11 G12 G13 G14 G15 G16 G17 G18
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
OPTO 9
OPTO 10
OPTO 11
OPTO 12
OPTO 13
OPTO 14
OPTO 15
OPTO 16
COMMON CONNECTION
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18
F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15 F16 F17 F18
MiCOM P643 (PART)
PHASE ROTATION
A B C
C24 C23 C26 C25 C28 C27 C18 C17 C20 C19 C22 C21 E24 E23 E26 E25 E28 E27
/ A (1)
/ B (1)
/ C (1)
/ A (2)
/ B (2)
/ C (2)
/ A (3)
/ B (3)
/ C (3)
CASE EARTH
BIAS 1
BIAS 2
BIAS 3
P1 S1 S2 P2
NOTE 2
PROTECTED TRANSFORMER
SEE SHEET 2 FOR NOTES
P4893ENa
10P64301_1

Figure 17 - Three bias input transformer differential (16 I/P & 16 O/P) with 4 pole VT inputs (60TE)


MiCOM P643 (PART)
A
B
C
N
n
a
b
c
NOTE 9
NOTE 4
NOTE 8
NOTE 10
NOTE 3
C2
VA
C1
C4
VB
C3
E2
VC
E1
VN
E4
VFLUX
E3
OPTIONAL
C12
/ Y (TV)
C11
C14
/ Y (LV)
C13
C16
/ Y (HV)
C15
GROUNDED WYE
NEUTRAL TAILS
TV
LV
HV
S1
S2
P1
P2
VEE CONNECTED VTs (ALTERNATIVE)
MODULE TERMINAL BLOCK
VIEWED FROM REAR
1
2
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
P4894ENa
10P64301_2

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
10. DERIVED NEUTRAL POINT. SEE P64X/ENT/- - FOR DETAILS OF RESISTORS.

P643 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3
HV + LV	HV		LV
HV + LV (x2)	HV	LV	LV
HV (x2) + LV	HV	HV	LV
HV + TV + LV	HV	TV	LV

TABLE 1 (NOTES 5 & 6)

Figure 18 - Three bias input transformer differential (16 I/P & 16 O/P) with 4 pole VT inputs (60TE)

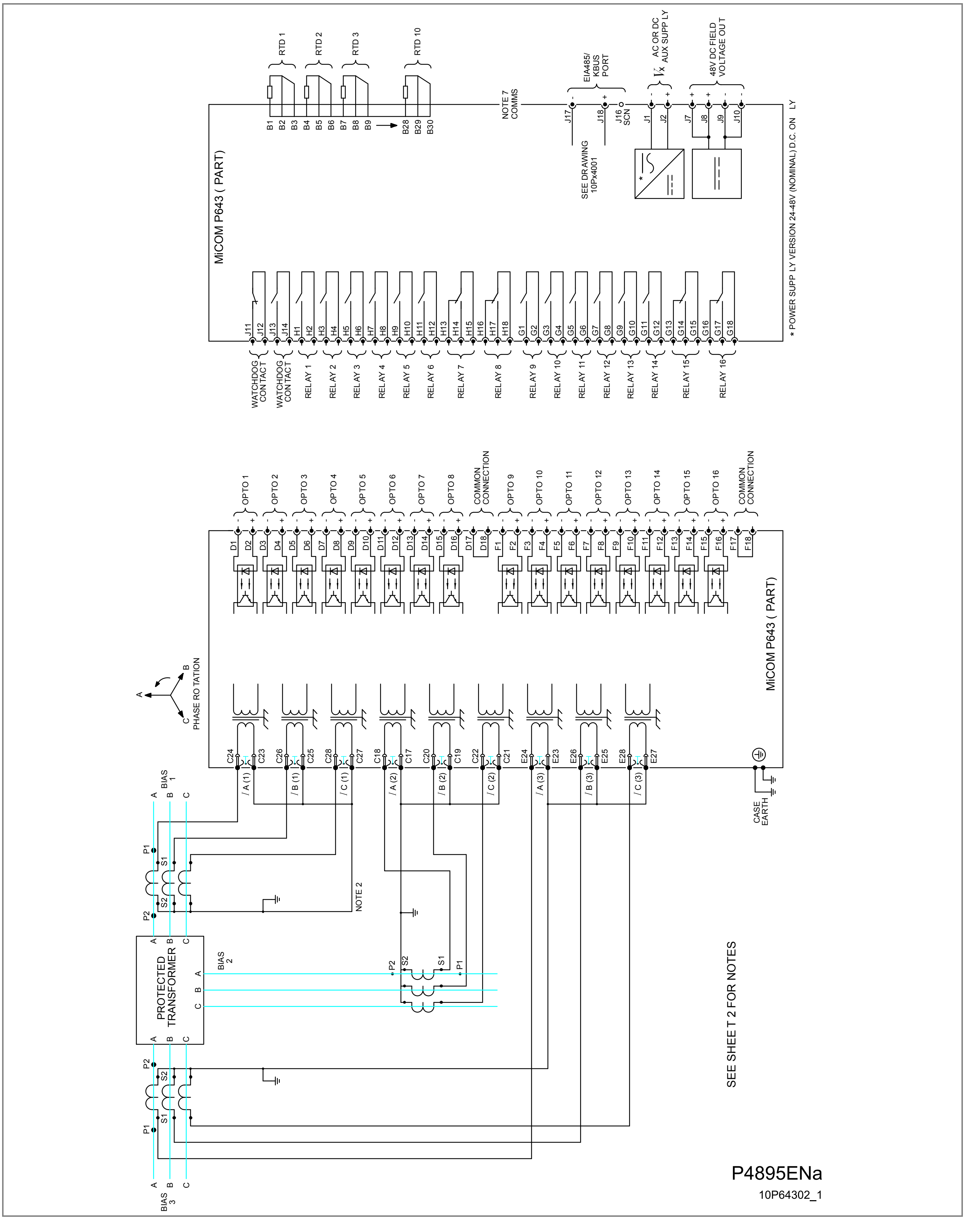
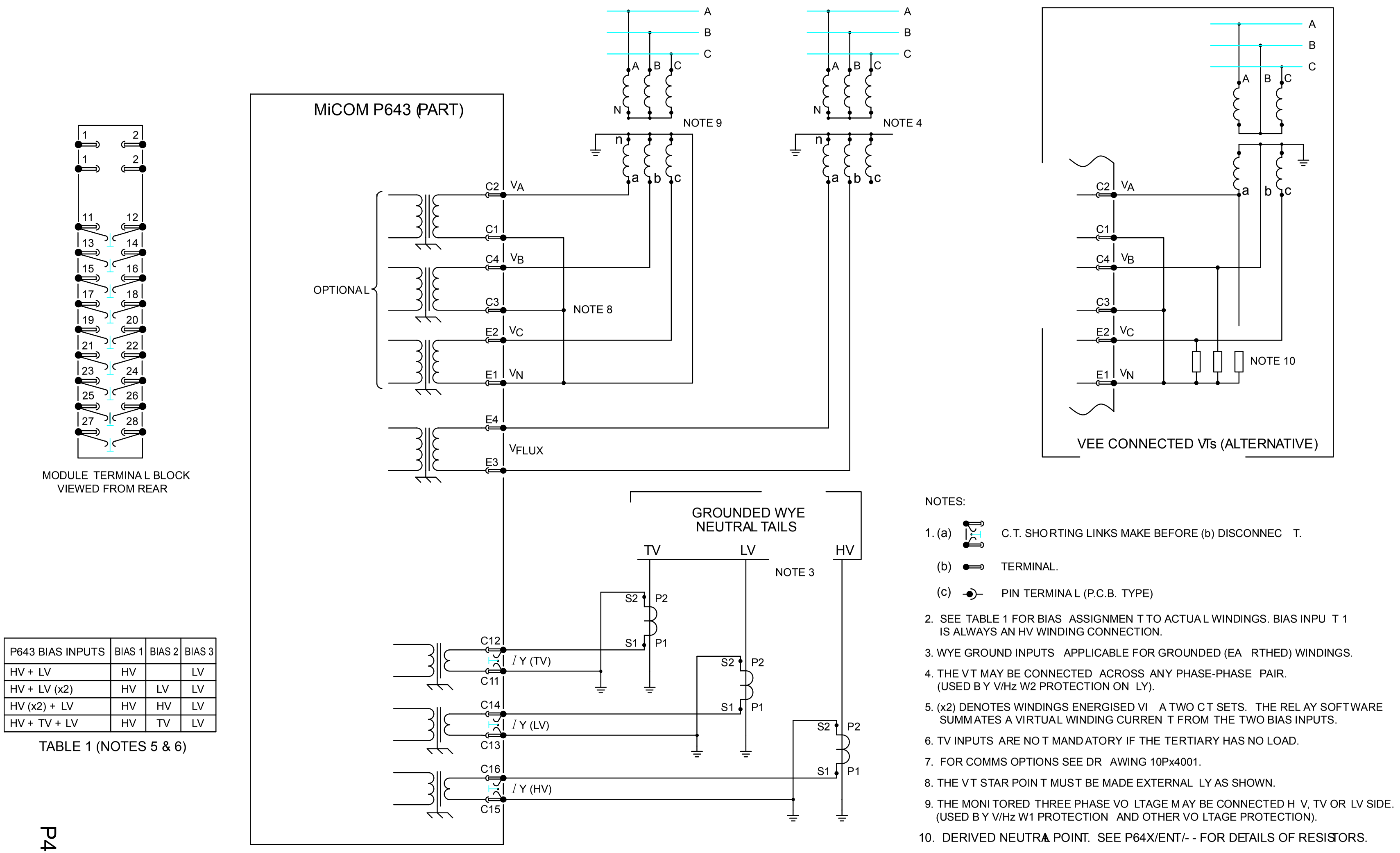

MiCOM P643 (PART)
RTD 1
RTD 2
RTD 3
RTD 10
B1
B2
B3
B4
B5
B6
B7
B8
B9
B28
B29
B30
NOTE 7
COMMS
EIA485/
KBUS
PORT
J17
J18
J16
SCN
SEE DRAWING
10Px4001
AC OR DC
AUX SUPP LY
Vx
J1
J2
48V DC FIELD
VOLTAGE OUT
J7
J8
J9
J10
* POWER SUPP LY VERSION 24-48V (NOMINAL) D.C. ON LY
J11
J12
J13
J14
H1
H2
H3
H4
H5
H6
H7
H8
H9
H10
H11
H12
H13
H14
H15
H16
H17
H18
G1
G2
G3
G4
G5
G6
G7
G8
G9
G10
G11
G12
G13
G14
G15
G16
G17
G18
WATCHDOG CONTACT
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
RELAY 9
RELAY 10
RELAY 11
RELAY 12
RELAY 13
RELAY 14
RELAY 15
RELAY 16
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
OPTO 9
OPTO 10
OPTO 11
OPTO 12
OPTO 13
OPTO 14
OPTO 15
OPTO 16
COMMON CONNECTION
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12
F13
F14
F15
F16
F17
F18
MiCOM P643 (PART)
A
B
C
PHASE ROTATION
C24
C23
C26
C25
C28
C27
C18
C17
C20
C19
C22
C21
E24
E23
E26
E25
E28
E27
/ A (1)
/ B (1)
/ C (1)
/ A (2)
/ B (2)
/ C (2)
/ A (3)
/ B (3)
/ C (3)
CASE EARTH
A
B
C
BIAS 1
P1
S1
P2
S2
NOTE 2
PROTECTED TRANSFORMER
A
B
C
BIAS 2
P2
S2
S1
P1
P2
S2
S1
P1
A
B
C
BIAS 3
SEE SHEET 2 FOR NOTES
P4895ENa
10P64302_1

Figure 19 - Three bias input transformer differential (16 I/P & 16 O/P + RTD) with 4 pole VT inputs (60TE)


MiCOM P643 (PART)
A
B
C
N
n
a
b
c
NOTE 9
NOTE 4
NOTE 8
NOTE 10
NOTE 3
C2
VA
C1
C4
VB
C3
E2
VC
E1
VN
E4
E3
VFLUX
OPTIONAL
VEE CONNECTED VTs (ALTERNATIVE)
GROUNDED WYE NEUTRAL TAILS
TV
LV
HV
S2
P2
S1
P1
C12
C11
/ Y (TV)
C14
C13
/ Y (LV)
C16
C15
/ Y (HV)
1
2
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
MODULE TERMINAL BLOCK VIEWED FROM REAR
P4896ENa
10P64302_2

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
10. DERIVED NEUTRAL POINT. SEE P64X/ENT/- - FOR DETAILS OF RESISTORS.

P643 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3
HV + LV	HV		LV
HV + LV (x2)	HV	LV	LV
HV (x2) + LV	HV	HV	LV
HV + TV + LV	HV	TV	LV

TABLE 1 (NOTES 5 & 6)

Figure 20 - Three bias input transformer differential (16 I/P & 16 O/P + RTD) with 4 pole VT inputs (60TE)

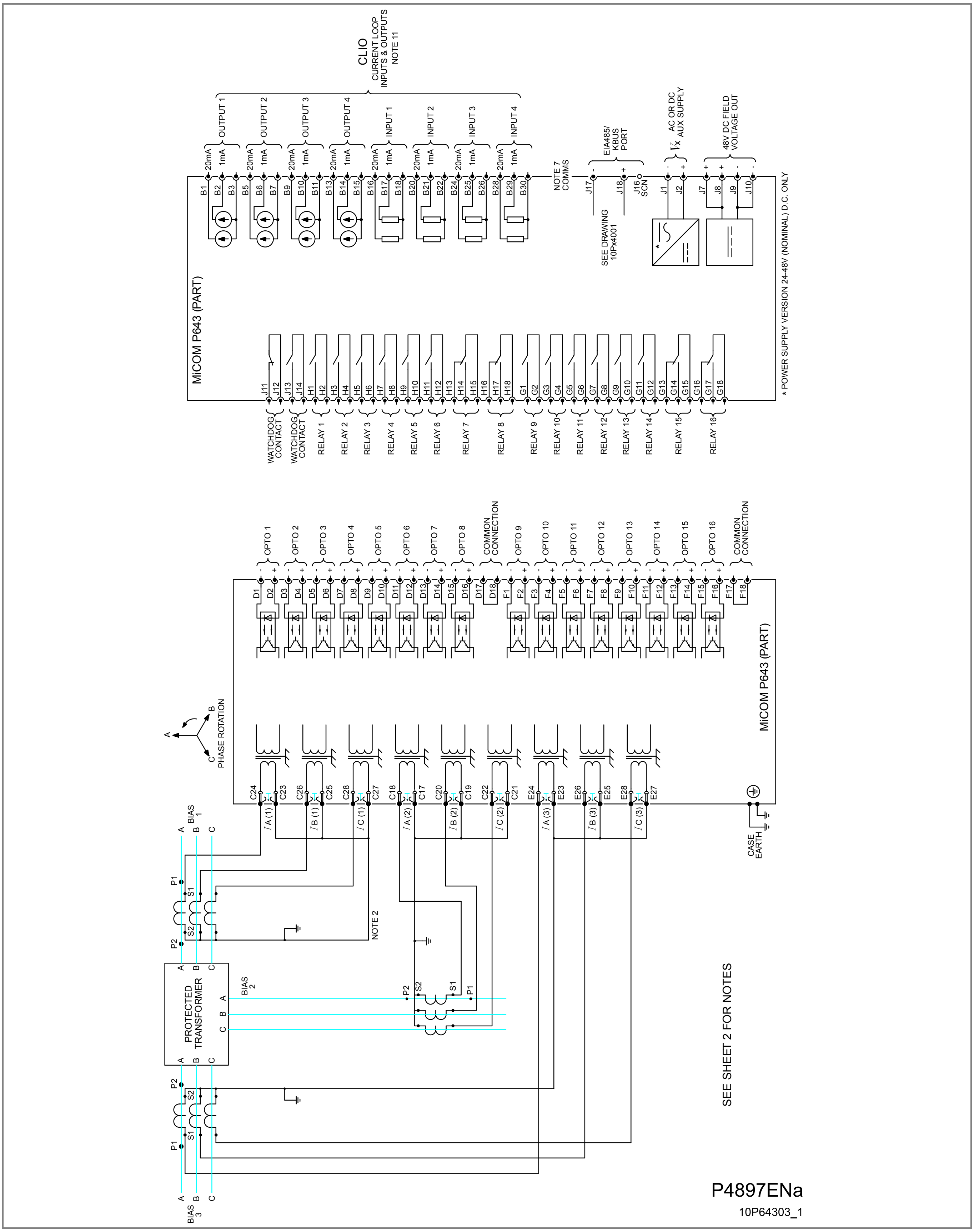
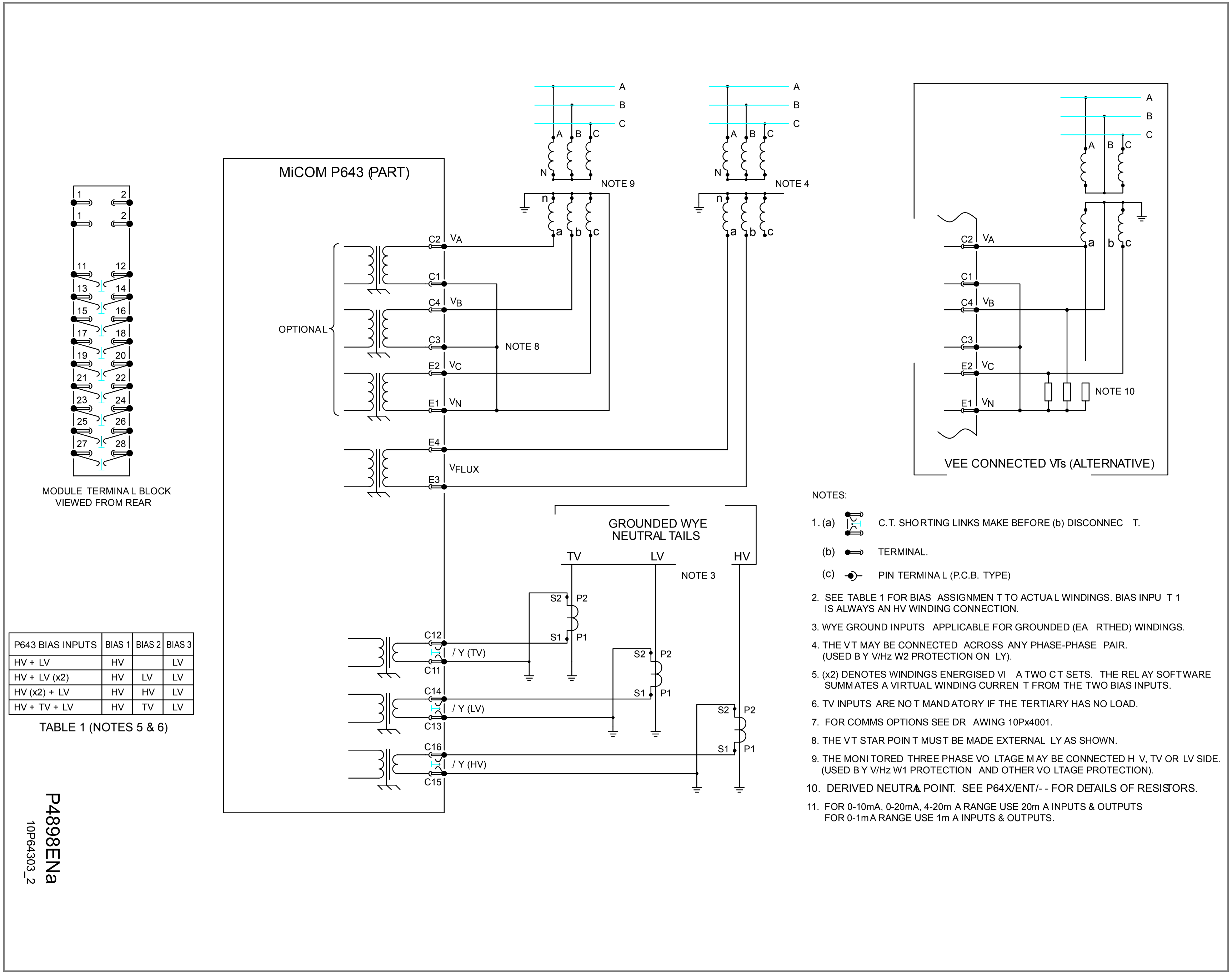

CLIO
CURRENT LOOP
INPUTS & OUTPUTS
NOTE 11
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
INPUT 1
INPUT 2
INPUT 3
INPUT 4
20mA
1mA
B1
B2
B3
B5
B6
B7
B9
B10
B11
B13
B14
B15
B16
B17
B18
B20
B21
B22
B24
B25
B26
B28
B29
B30
NOTE 7
COMMS
EIA485/
KBUS
PORT
J17
J18
J16
SCN
SEE DRAWING
10Px4001
AC OR DC
AUX SUPPLY
Vx
J1
J2
48V DC FIELD
VOLTAGE OUT
J7
J8
J9
J10
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
MiCOM P643 (PART)
J11
J12
J13
J14
H1
H2
H3
H4
H5
H6
H7
H8
H9
H10
H11
H12
H13
H14
H15
H16
H17
H18
G1
G2
G3
G4
G5
G6
G7
G8
G9
G10
G11
G12
G13
G14
G15
G16
G17
G18
WATCHDOG
CONTACT
WATCHDOG
CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
RELAY 9
RELAY 10
RELAY 11
RELAY 12
RELAY 13
RELAY 14
RELAY 15
RELAY 16
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON
CONNECTION
OPTO 9
OPTO 10
OPTO 11
OPTO 12
OPTO 13
OPTO 14
OPTO 15
OPTO 16
COMMON
CONNECTION
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12
F13
F14
F15
F16
F17
F18
MiCOM P643 (PART)
A
B
C
PHASE ROTATION
C24
C23
C26
C25
C28
C27
C18
C17
C20
C19
C22
C21
E24
E23
E26
E25
E28
E27
/ A (1)
/ B (1)
/ C (1)
/ A (2)
/ B (2)
/ C (2)
/ A (3)
/ B (3)
/ C (3)
CASE
EARTH
BIAS
1
P1
S1
S2
P2
NOTE 2
PROTECTED
TRANSFORMER
BIAS
2
BIAS
3
SEE SHEET 2 FOR NOTES
P4897ENa
10P64303_1

Figure 21 - Three bias input transformer differential (16 I/P & 16 O/P + CLIO) with 4 pole VT inputs (60TE)


MiCOM P643 (PART)
OPTIONAL
C2 VA
C1
C4 VB
C3
E2 VC
E1 VN
E4
VFLUX
E3
NOTE 8
NOTE 9
NOTE 4
A
B
C
N
n
a
b
c
C12
/ Y (TV)
C11
C14
/ Y (LV)
C13
C16
/ Y (HV)
C15
GROUNDED WYE NEUTRAL TAILS
TV
LV
HV
NOTE 3
S2
P2
S1
P1
VEE CONNECTED VTs (ALTERNATIVE)
NOTE 10
MODULE TERMINAL BLOCK VIEWED FROM REAR
1
2
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
P4898ENa
10P64303_2

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
10. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
11. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

P643 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3
HV + LV	HV		LV
HV + LV (x2)	HV	LV	LV
HV (x2) + LV	HV	HV	LV
HV + TV + LV	HV	TV	LV

TABLE 1 (NOTES 5 & 6)

Figure 22 - Three bias input transformer differential (16 I/P & 16 O/P + CLIO) with 4 pole VT inputs (60TE)

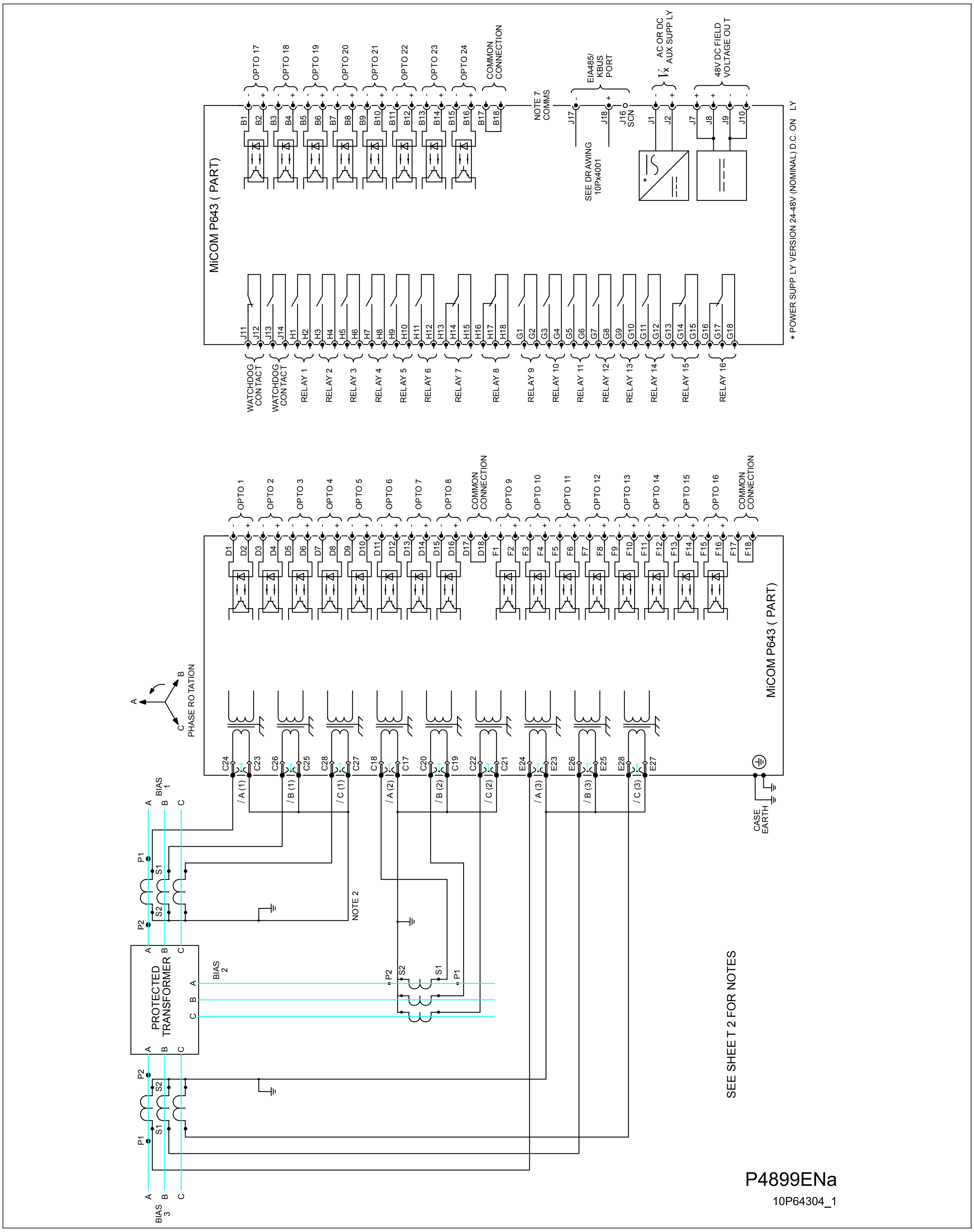
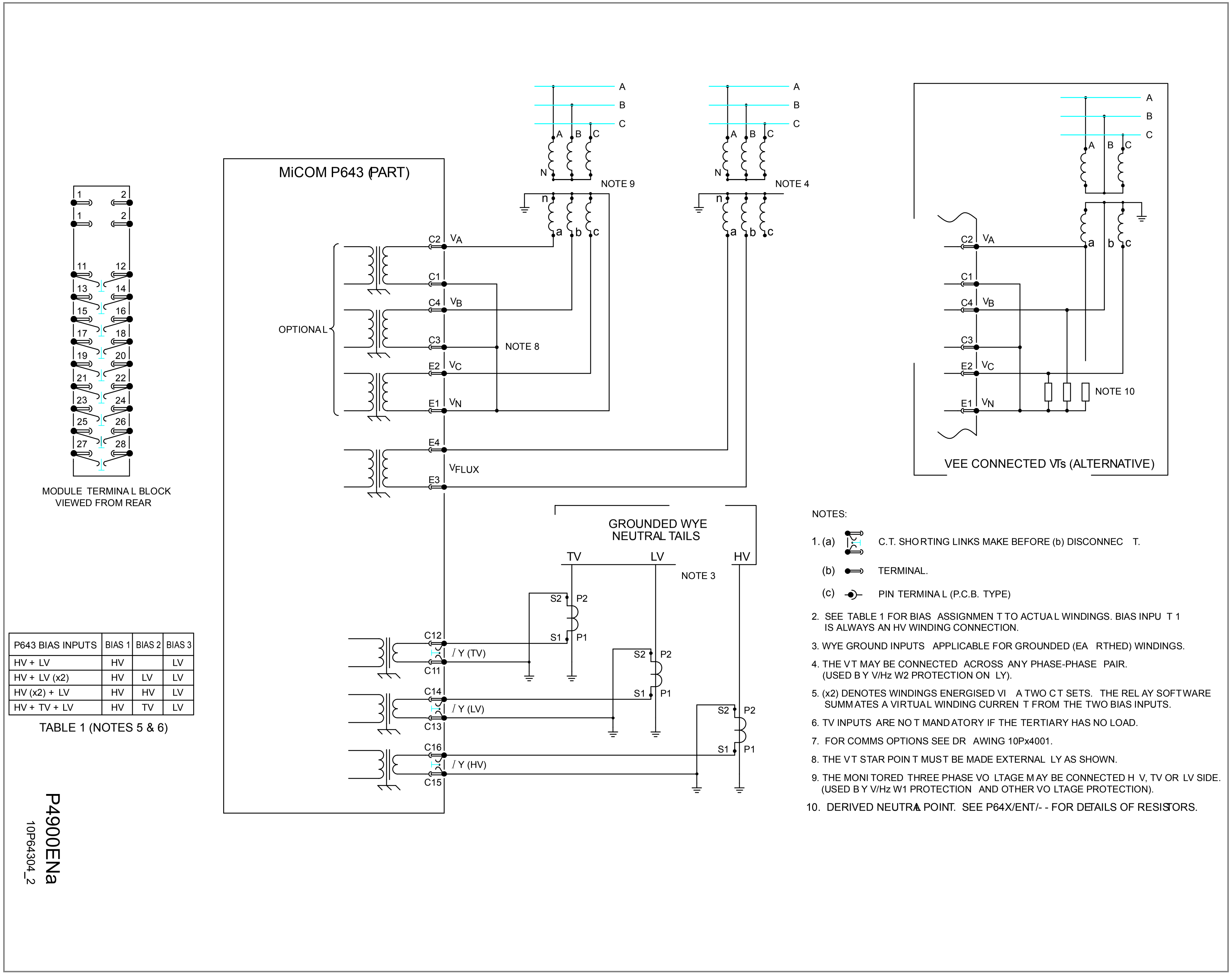

MiCOM P643 (PART)
OPTO 17
OPTO 18
OPTO 19
OPTO 20
OPTO 21
OPTO 22
OPTO 23
OPTO 24
COMMON CONNECTION
B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18
NOTE 7 COMMS
EIA485/ KBUS PORT
J17 J18 J16 SCN
SEE DRAWING 10Px4001
Vx AC OR DC AUX SUPPLY
J1 J2
48V DC FIELD VOLTAGE OUT
J7 J8 J9 J10
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
J11 J12 J13 J14 H1 H2 H3 H4 H5 H6 H7 H8 H9 H10 H11 H12 H13 H14 H15 H16 H17 H18 G1 G2 G3 G4 G5 G6 G7 G8 G9 G10 G11 G12 G13 G14 G15 G16 G17 G18
WATCHDOG CONTACT
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
RELAY 9
RELAY 10
RELAY 11
RELAY 12
RELAY 13
RELAY 14
RELAY 15
RELAY 16
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
OPTO 9
OPTO 10
OPTO 11
OPTO 12
OPTO 13
OPTO 14
OPTO 15
OPTO 16
COMMON CONNECTION
D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15 D16 D17 D18
F1 F2 F3 F4 F5 F6 F7 F8 F9 F10 F11 F12 F13 F14 F15 F16 F17 F18
MiCOM P643 (PART)
A
B
C
PHASE ROTATION
C24 C23 C26 C25 C28 C27 C18 C17 C20 C19 C22 C21 E24 E23 E26 E25 E28 E27
IA (1)
IB (1)
IC (1)
IA (2)
IB (2)
IC (2)
IA (3)
IB (3)
IC (3)
CASE EARTH
A B C BIAS 1
P1 S1 S2 P2
NOTE 2
PROTECTED TRANSFORMER
A B C
BIAS 2
P2 S2 S1 P1
A B C BIAS 3
SEE SHEET 2 FOR NOTES
P4899ENa
10P64304_1

Figure 23 - Three bias input transformer differential (24 I/P & 16 O/P) with 4 pole VT inputs (60TE)


MiCOM P643 (PART)
A
B
C
N
n
a
b
c
NOTE 9
NOTE 4
NOTE 8
NOTE 10
NOTE 3
C2
V_A
C1
C4
V_B
C3
E2
V_C
E1
V_N
E4
V_{FLUX}
E3
OPTIONAL
C12
/ Y (TV)
C11
C14
/ Y (LV)
C13
C16
/ Y (HV)
C15
S1
S2
P1
P2
GROUNDED WYE NEUTRAL TAILS
TV
LV
HV
VEE CONNECTED VTs (ALTERNATIVE)
MODULE TERMINAL BLOCK VIEWED FROM REAR
1
2
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
P4900ENa
10P64304_2

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
10. DERIVED NEUTRAL POINT. SEE P64X/ENT/- - FOR DETAILS OF RESISTORS.

P643 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3
HV + LV	HV		LV
HV + LV (x2)	HV	LV	LV
HV (x2) + LV	HV	HV	LV
HV + TV + LV	HV	TV	LV

TABLE 1 (NOTES 5 & 6)

Figure 24 - Three bias input transformer differential (24 I/P & 16 O/P) with 4 pole VT inputs (60TE)

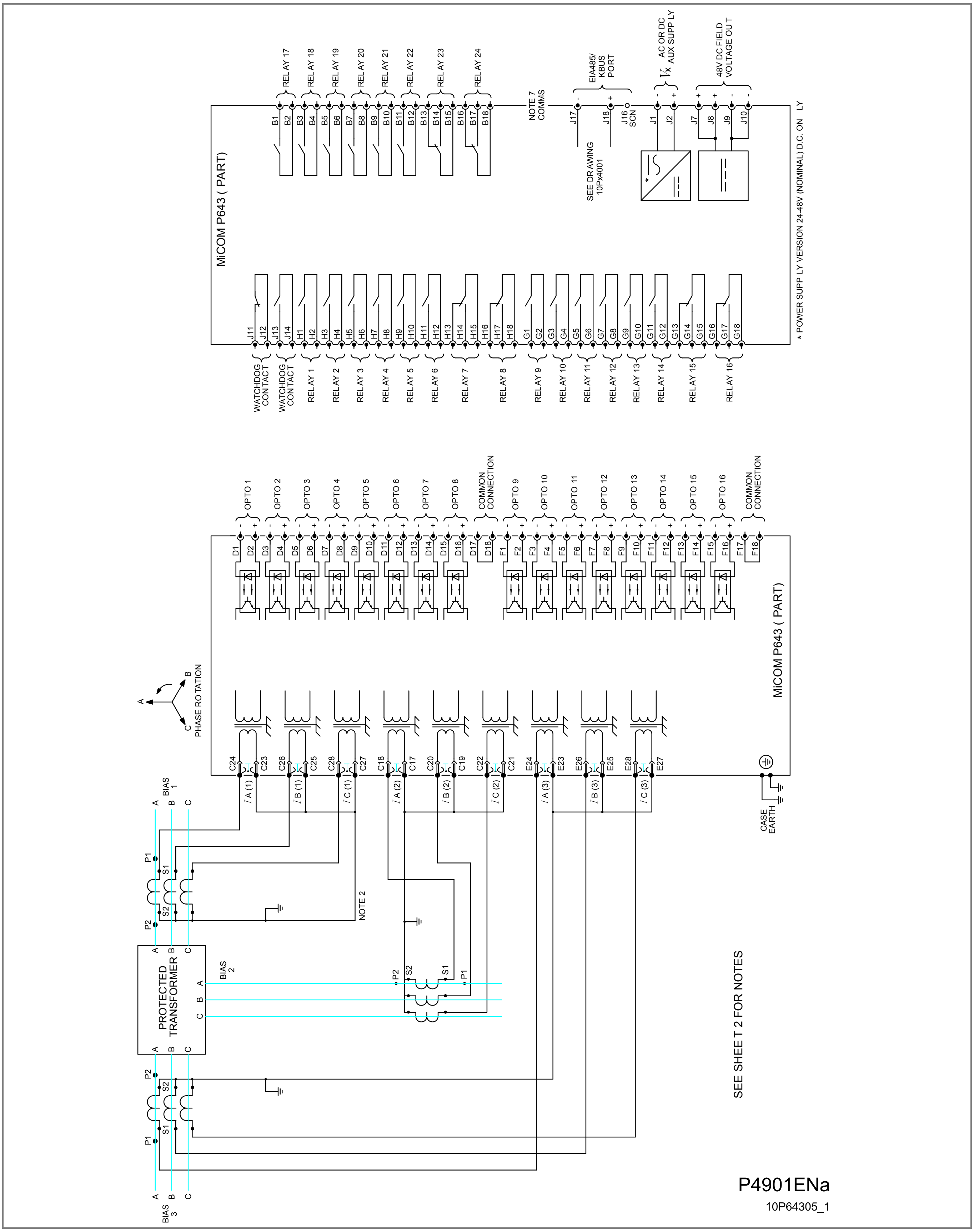
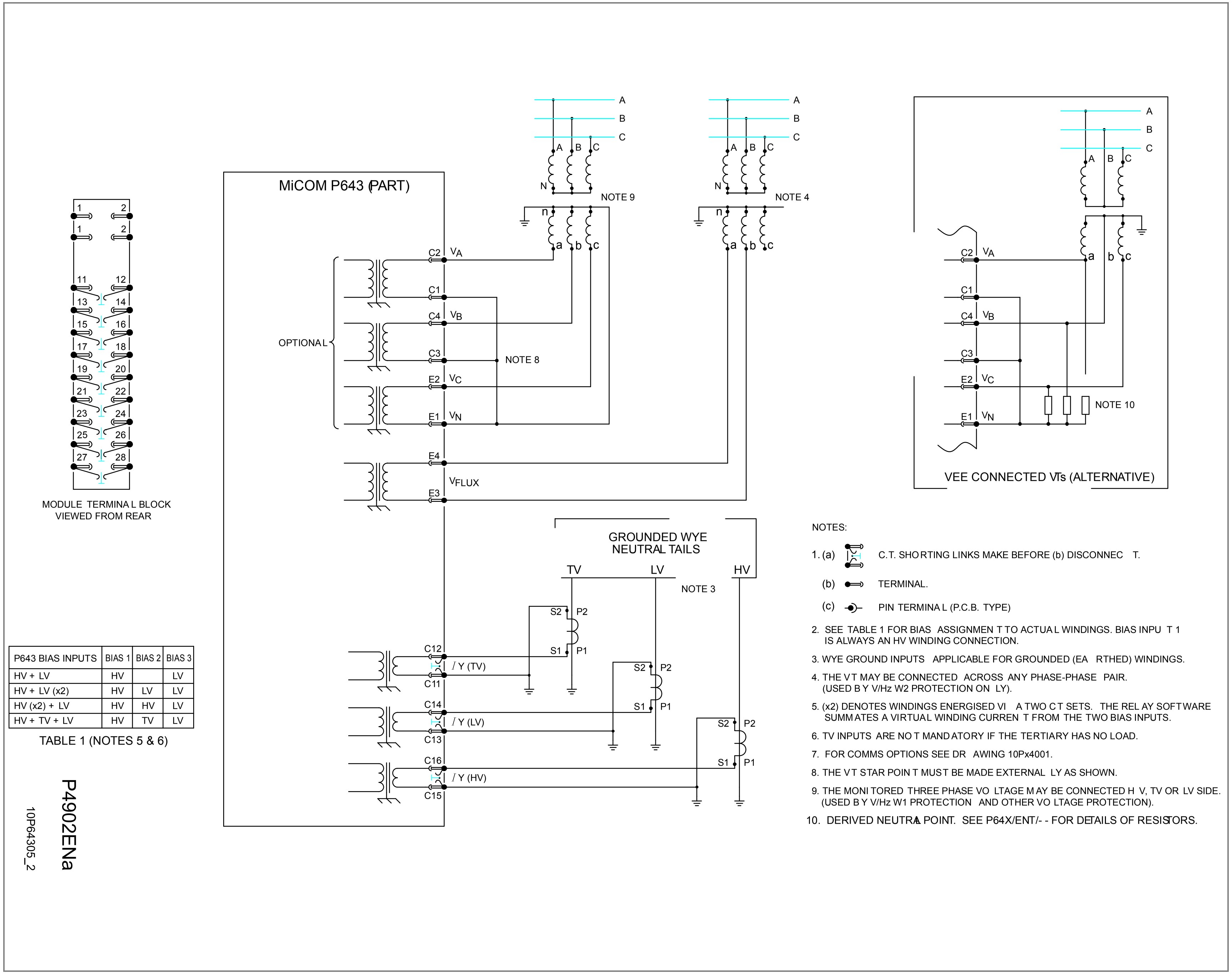

MiCOM P643 (PART)
WATCHDOG CONTACT
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
RELAY 9
RELAY 10
RELAY 11
RELAY 12
RELAY 13
RELAY 14
RELAY 15
RELAY 16
RELAY 17
RELAY 18
RELAY 19
RELAY 20
RELAY 21
RELAY 22
RELAY 23
RELAY 24
NOTE 7 COMMS
EIA485/ KBUS PORT
SEE DRAWING 10Px4001
J16 SCN
AC OR DC Vx AUX SUPPLY
48V DC FIELD VOLTAGE OUT
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
OPTO 9
OPTO 10
OPTO 11
OPTO 12
OPTO 13
OPTO 14
OPTO 15
OPTO 16
COMMON CONNECTION
MiCOM P643 (PART)
PHASE ROTATION
A
B
C
BIAS 1
BIAS 2
BIAS 3
I A (1)
I B (1)
I C (1)
I A (2)
I B (2)
I C (2)
I A (3)
I B (3)
I C (3)
P1
P2
S1
S2
NOTE 2
PROTECTED TRANSFORMER
CASE EARTH
SEE SHEET 2 FOR NOTES
P4901ENa
10P64305_1

Figure 25 - Three bias input transformer differential (16 I/P & 24 O/P) with 4 pole VT inputs (60TE)


MiCOM P643 (PART)
OPTIONAL
C2 VA
C1
C4 VB
C3
E2 VC
E1 VN
E4
VFLUX
E3
C12
/ Y (TV)
C11
C14
/ Y (LV)
C13
C16
/ Y (HV)
C15
NOTE 8
NOTE 9
NOTE 4
NOTE 3
NOTE 10
A
B
C
N
n
a
b
c
GROUNDED WYE NEUTRAL TAILS
TV
LV
HV
S1
S2
P1
P2
VEE CONNECTED VTs (ALTERNATIVE)
MODULE TERMINAL BLOCK VIEWED FROM REAR
1
2
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
P4902ENa
10P64305_2

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
10. DERIVED NEUTRAL POINT. SEE P64X/ENT/- - FOR DETAILS OF RESISTORS.

P643 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3
HV + LV	HV		LV
HV + LV (x2)	HV	LV	LV
HV (x2) + LV	HV	HV	LV
HV + TV + LV	HV	TV	LV

TABLE 1 (NOTES 5 & 6)

Figure 26 - Three bias input transformer differential (16 I/P & 24 O/P) with 4 pole VT inputs (60TE)

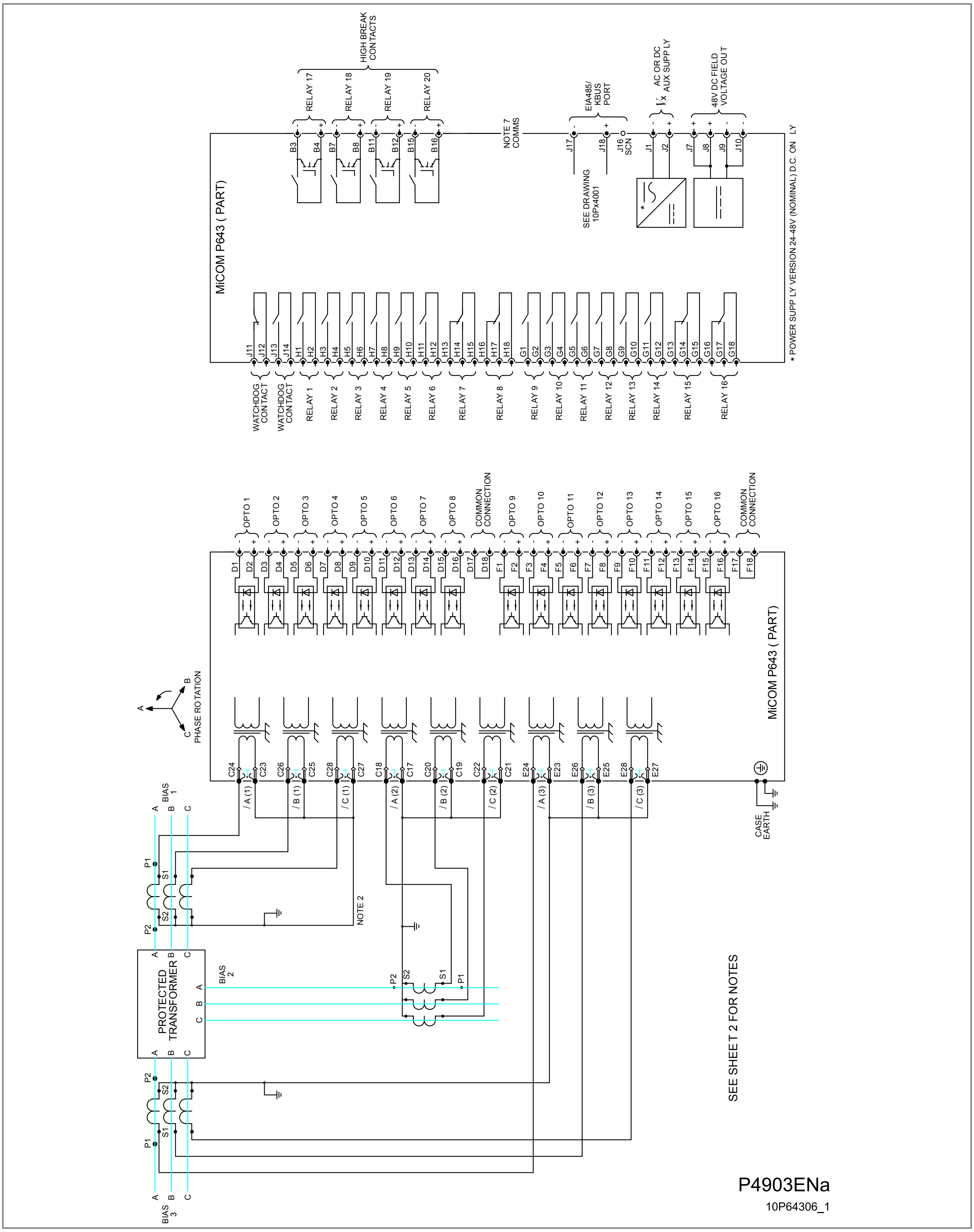
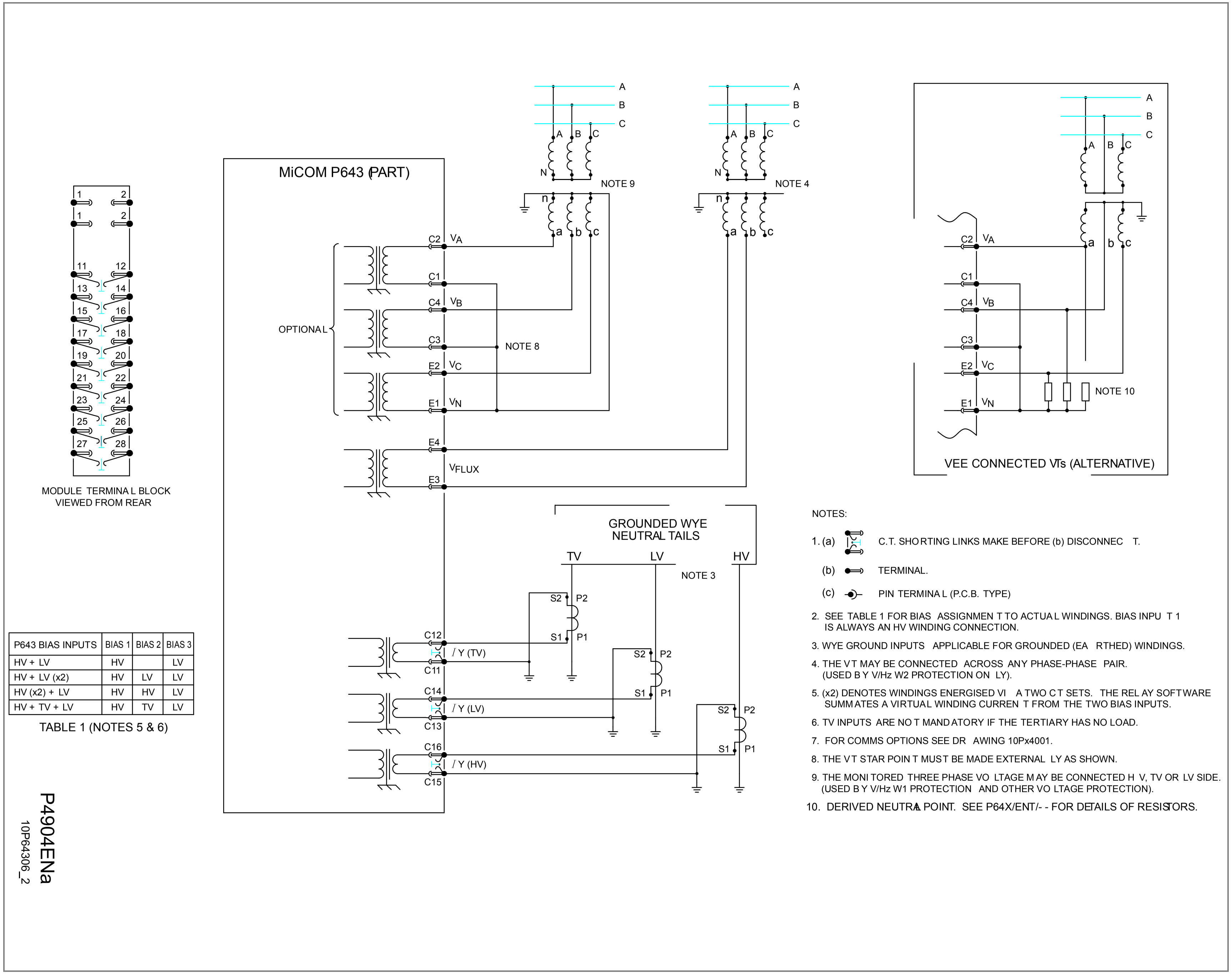

MiCOM P643 (PART)
HIGH BREAK CONTACTS
RELAY 17
RELAY 18
RELAY 19
RELAY 20
B3
B4
B7
B8
B11
B12
B15
B16
NOTE 7 COMMS
EIA485/ KBUS PORT
J17
J18
J16 SCN
SEE DRAWING 10Px4001
AC OR DC AUX SUPP LY
Vx
J1
J2
48V DC FIELD VOLTAGE OUT
J7
J8
J9
J10
* POWER SUPP LY VERSION 24-48V (NOMINAL) D.C. ON LY
WATCHDOG CONTACT
WATCHDOG CONTACT
J11
J12
J13
J14
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
RELAY 9
RELAY 10
RELAY 11
RELAY 12
RELAY 13
RELAY 14
RELAY 15
RELAY 16
H1
H2
H3
H4
H5
H6
H7
H8
H9
H10
H11
H12
H13
H14
H15
H16
H17
H18
G1
G2
G3
G4
G5
G6
G7
G8
G9
G10
G11
G12
G13
G14
G15
G16
G17
G18
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
OPTO 9
OPTO 10
OPTO 11
OPTO 12
OPTO 13
OPTO 14
OPTO 15
OPTO 16
COMMON CONNECTION
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
D18
F1
F2
F3
F4
F5
F6
F7
F8
F9
F10
F11
F12
F13
F14
F15
F16
F17
F18
MiCOM P643 (PART)
PHASE ROTATION
A
B
C
C24
C23
C26
C25
C28
C27
C18
C17
C20
C19
C22
C21
E24
E23
E26
E25
E28
E27
IA (1)
IB (1)
IC (1)
IA (2)
IB (2)
IC (2)
IA (3)
IB (3)
IC (3)
CASE EARTH
BIAS 1
BIAS 2
BIAS 3
P1
P2
S1
S2
NOTE 2
PROTECTED TRANSFORMER
SEE SHEET 2 FOR NOTES
P4903ENa
10P64306_1

Figure 27 - Three bias input transformer differential (16 I/P & 20 O/P) with 4 pole VT input (60TE)


MiCOM P643 (PART)
A
B
C
N
n
a
b
c
NOTE 9
NOTE 4
NOTE 8
NOTE 10
NOTE 3
C2
VA
C1
C4
VB
C3
E2
VC
E1
VN
E4
VFLUX
E3
OPTIONAL
VEE CONNECTED VTs (ALTERNATIVE)
GROUNDED WYE
NEUTRAL TAILS
TV
LV
HV
S1
S2
P1
P2
C12
/ Y (TV)
C11
C14
/ Y (LV)
C13
C16
/ Y (HV)
C15
MODULE TERMINAL BLOCK
VIEWED FROM REAR
1
2
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
P4904ENa
10P64306_2

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
10. DERIVED NEUTRAL POINT. SEE P64X/ENT/- - FOR DETAILS OF RESISTORS.

P643 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3
HV + LV	HV		LV
HV + LV (x2)	HV	LV	LV
HV (x2) + LV	HV	HV	LV
HV + TV + LV	HV	TV	LV

TABLE 1 (NOTES 5 & 6)

Figure 28 - Three bias input transformer differential (16 I/P & 20 O/P) with 4 pole VT input (60TE)

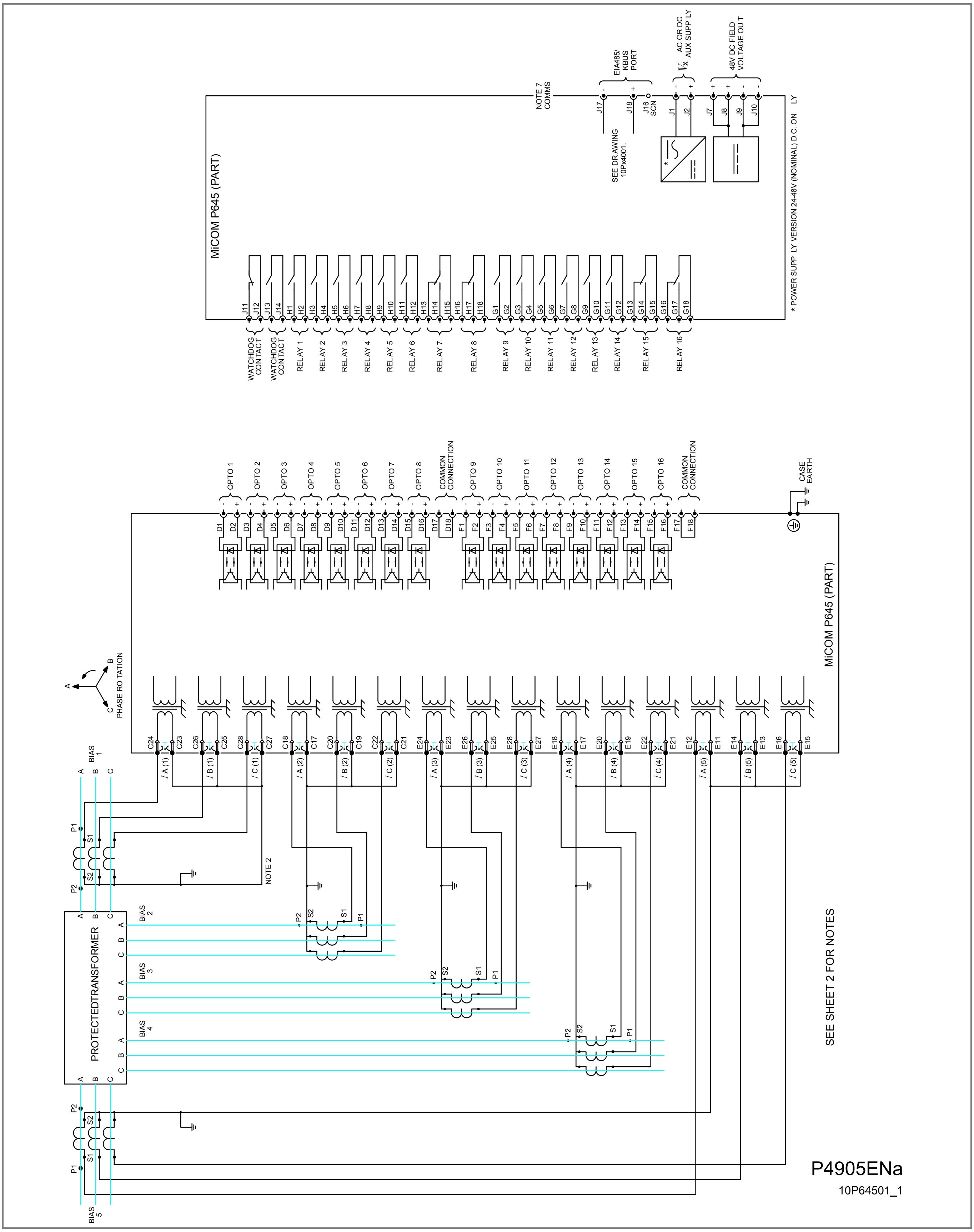
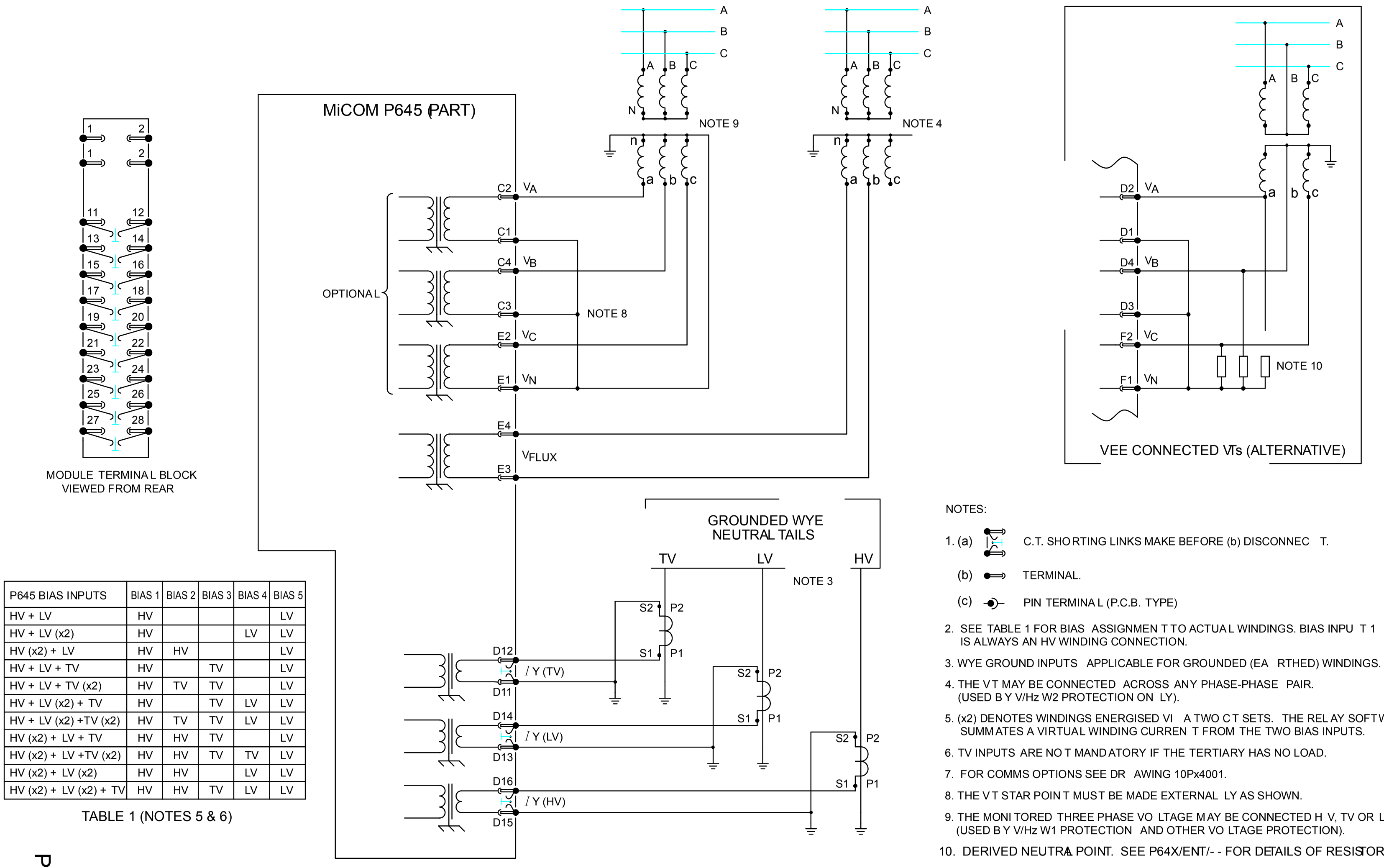

MiCOM P645 (PART)
NOTE 7
COMMS
EIA485/
KBUS
PORT
SEE DRAWING
10Px4001.
J17
J18
J16
SCN
AC OR DC
AUX SUPPLY
Vx
J1
J2
48V DC FIELD
VOLTAGE OUT
J7
J8
J9
J10
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
WATCHDOG CONTACT
J11
J12
WATCHDOG CONTACT
J13
J14
RELAY 1
H1
H2
RELAY 2
H3
H4
RELAY 3
H5
H6
RELAY 4
H7
H8
RELAY 5
H9
H10
RELAY 6
H11
H12
RELAY 7
H13
H14
H15
RELAY 8
H16
H17
H18
RELAY 9
G1
G2
RELAY 10
G3
G4
RELAY 11
G5
G6
RELAY 12
G7
G8
RELAY 13
G9
G10
RELAY 14
G11
G12
RELAY 15
G13
G14
G15
RELAY 16
G16
G17
G18
OPTO 1
D1
D2
OPTO 2
D3
D4
OPTO 3
D5
D6
OPTO 4
D7
D8
OPTO 5
D9
D10
OPTO 6
D11
D12
OPTO 7
D13
D14
OPTO 8
D15
D16
COMMON CONNECTION
D17
D18
OPTO 9
F1
F2
OPTO 10
F3
F4
OPTO 11
F5
F6
OPTO 12
F7
F8
OPTO 13
F9
F10
OPTO 14
F11
F12
OPTO 15
F13
F14
OPTO 16
F15
F16
COMMON CONNECTION
F17
F18
CASE EARTH
MiCOM P645 (PART)
A
B
C
PHASE ROTATION
C24
C23
I A (1)
C26
C25
I B (1)
C28
C27
I C (1)
C18
C17
I A (2)
C20
C19
I B (2)
C22
C21
I C (2)
E24
E23
I A (3)
E26
E25
I B (3)
E28
E27
I C (3)
E18
E17
I A (4)
E20
E19
I B (4)
E22
E21
I C (4)
E12
E11
I A (5)
E14
E13
I B (5)
E16
E15
I C (5)
BIAS 1
BIAS 2
BIAS 3
BIAS 4
BIAS 5
P1
P2
S1
S2
NOTE 2
PROTECTEDTRANSFORMER
SEE SHEET 2 FOR NOTES
P4905ENa
10P64501_1

Figure 29 - Five bias input transformer differential (16 I/P & 16 O/P) with 4 pole VT inputs (60TE)


A
B
C
A
B
C
N
n
a
b
c
NOTE 9
NOTE 4
VEE CONNECTED VTs (ALTERNATIVE)
D2
VA
D1
D4
VB
D3
F2
VC
F1
VN
NOTE 10
MiCOM P645 (PART)
C2
C1
C4
C3
E2
E1
E4
E3
VFLUX
NOTE 8
OPTIONAL
GROUNDED WYE NEUTRAL TAILS
TV
LV
HV
NOTE 3
S1
S2
P1
P2
D12
D11
/ Y (TV)
D14
D13
/ Y (LV)
D16
D15
/ Y (HV)
1
2
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
MODULE TERMINAL BLOCK VIEWED FROM REAR
P4906ENa
10P64501_2

P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +TV (x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV (x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

TABLE 1 (NOTES 5 & 6)

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
10. DERIVED NEUTRAL POINT. SEE P64X/ENT/- - FOR DETAILS OF RESISTORS.

Figure 30 - Five bias input transformer differential (16 I/P & 16 O/P) with 4 pole VT inputs (60TE)

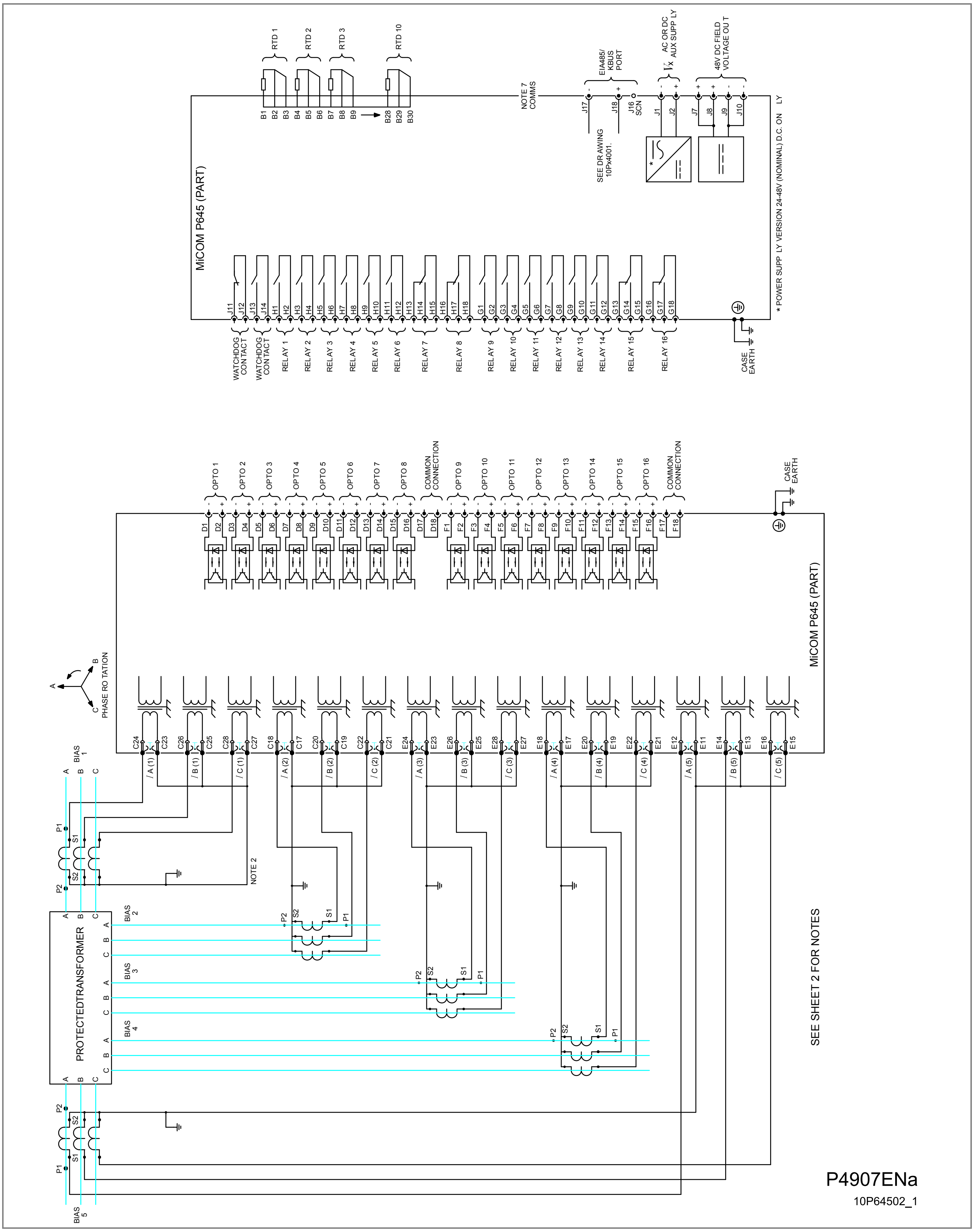
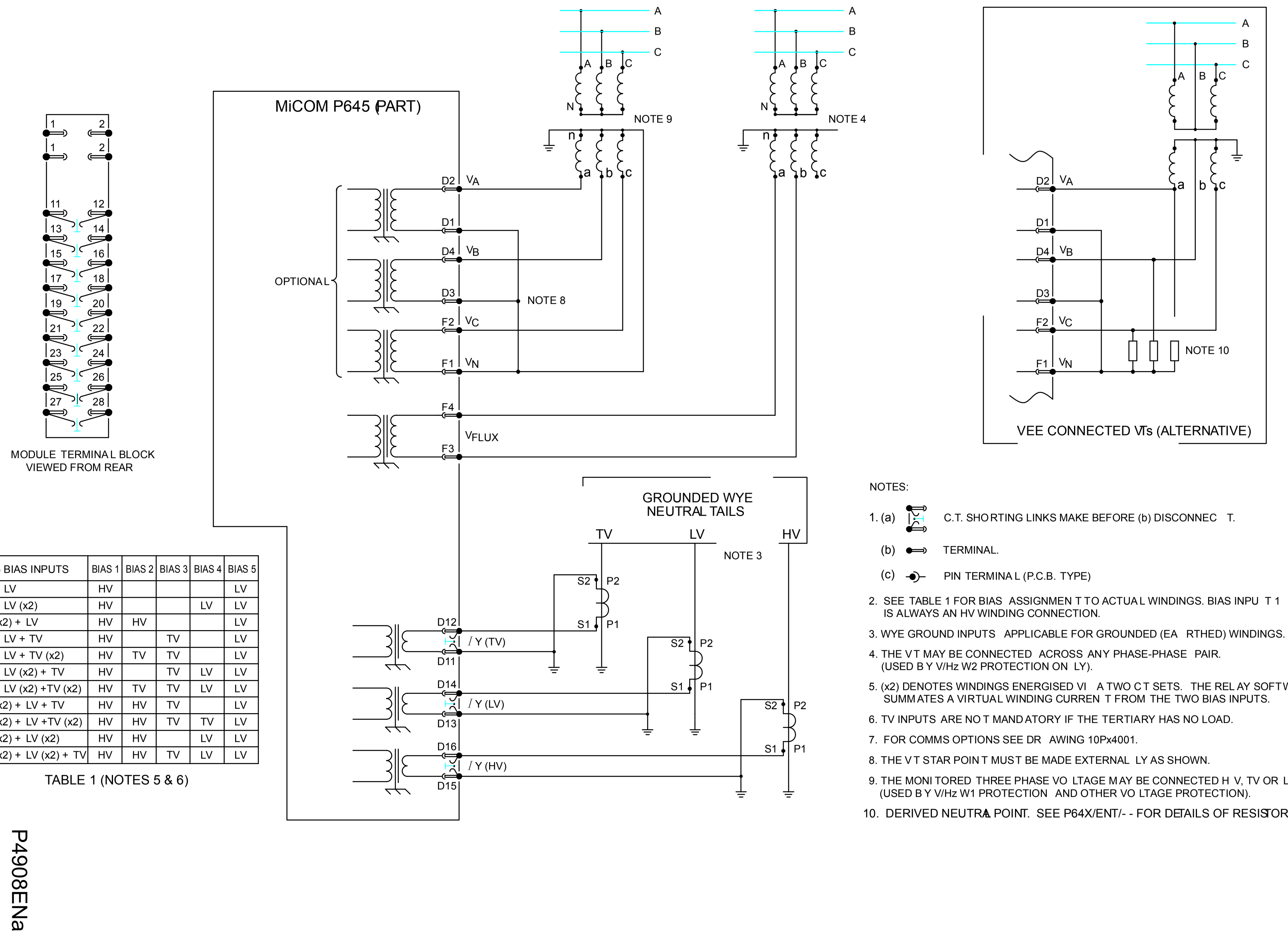

MiCOM P645 (PART)
RTD 1
RTD 2
RTD 3
RTD 10
B1 B2 B3 B4 B5 B6 B7 B8 B9 B28 B29 B30
NOTE 7 COMMS
EIA485/ KBUS PORT
SEE DRAWING 10Px4001.
J17 J18 J16 SCN
AC OR DC AUX SUPPLY
Vx
J1 J2
48V DC FIELD VOLTAGE OUT
J7 J8 J9 J10
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
WATCHDOG CONTACT
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
RELAY 9
RELAY 10
RELAY 11
RELAY 12
RELAY 13
RELAY 14
RELAY 15
RELAY 16
CASE EARTH
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
OPTO 9
OPTO 10
OPTO 11
OPTO 12
OPTO 13
OPTO 14
OPTO 15
OPTO 16
COMMON CONNECTION
CASE EARTH
MiCOM P645 (PART)
PHASE ROTATION
A B C
IA (1) IB (1) IC (1) IA (2) IB (2) IC (2) IA (3) IB (3) IC (3) IA (4) IB (4) IC (4) IA (5) IB (5) IC (5)
BIAS 1
BIAS 2
BIAS 3
BIAS 4
BIAS 5
P1 S1 S2 P2
NOTE 2
PROTECTEDTRANSFORMER
SEE SHEET 2 FOR NOTES
P4907ENa
10P64502_1

Figure 31 - Five bias input transformer differential (16 I/P & 16 O/P + RTD) with 4 pole VT inputs (60TE)


MiCOM P645 (PART)
A
B
C
N
n
a
b
c
NOTE 9
NOTE 4
NOTE 8
NOTE 10
NOTE 3
D2
VA
D1
D4
VB
D3
F2
VC
F1
VN
F4
VFLUX
F3
OPTIONAL
D12
D11
D14
D13
D16
D15
/ Y (TV)
/ Y (LV)
/ Y (HV)
S1
S2
P1
P2
GROUNDED WYE NEUTRAL TAILS
TV
LV
HV
VEE CONNECTED VTs (ALTERNATIVE)
1 2 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28
MODULE TERMINAL BLOCK VIEWED FROM REAR
P4908ENa
10P64502_2

P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +TV (x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV (x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

TABLE 1 (NOTES 5 & 6)

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
10. DERIVED NEUTRAL POINT. SEE P64X/ENT/- - FOR DETAILS OF RESISTORS.

Figure 32 - Five bias input transformer differential (16 I/P & 16 O/P + RTD) with 4 pole VT inputs (60TE)

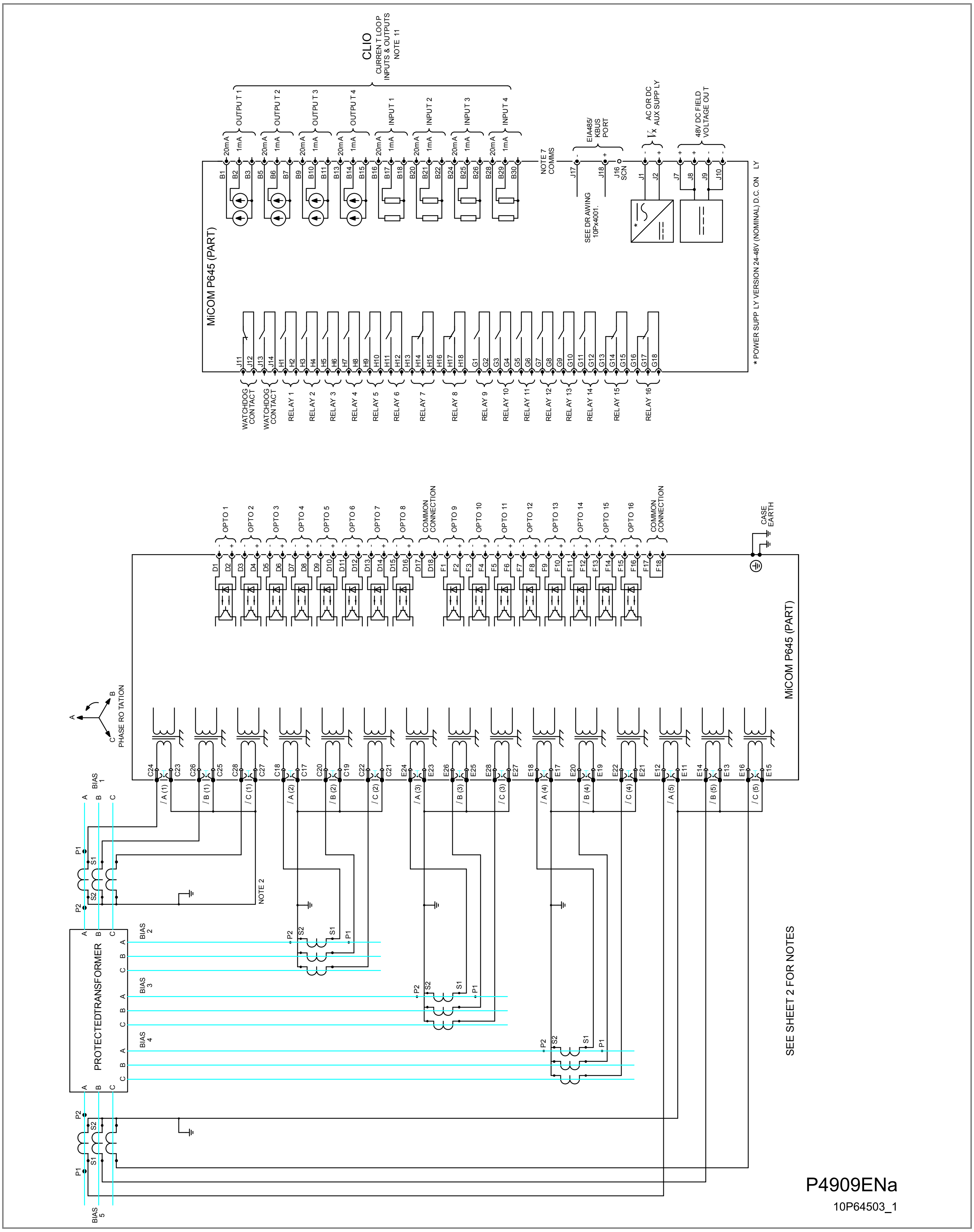
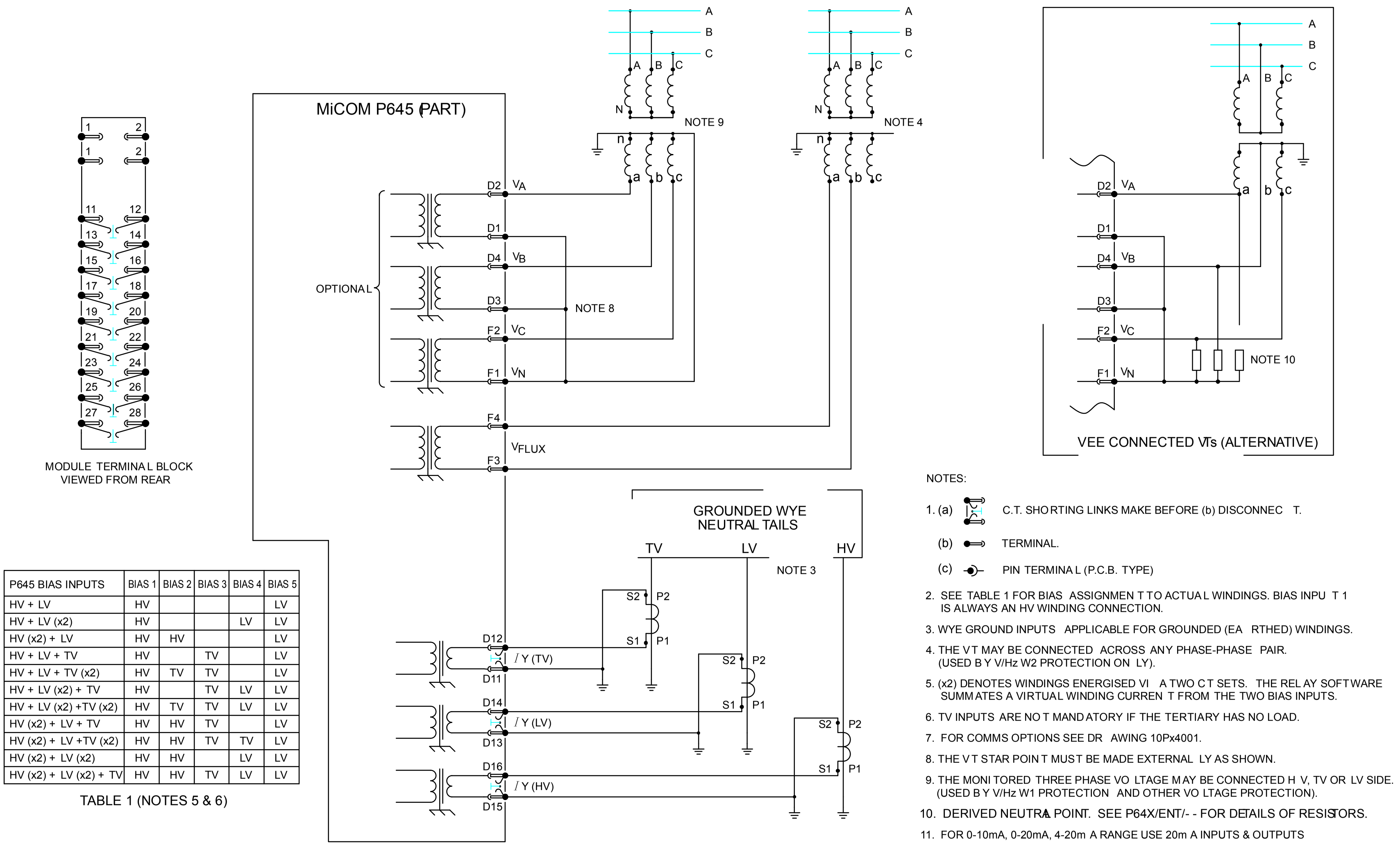

CLIO
CURRENT LOOP INPUTS & OUTPUTS NOTE 11
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
INPUT 1
INPUT 2
INPUT 3
INPUT 4
20mA
1mA
NOTE 7 COMMS
EIA485/ KBUS PORT
SCN
SEE DRAWING 10Px4001.
AC OR DC AUX SUPPLY
Vx
48V DC FIELD VOLTAGE OUT
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
MiCOM P645 (PART)
WATCHDOG CONTACT
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
RELAY 9
RELAY 10
RELAY 11
RELAY 12
RELAY 13
RELAY 14
RELAY 15
RELAY 16
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
OPTO 9
OPTO 10
OPTO 11
OPTO 12
OPTO 13
OPTO 14
OPTO 15
OPTO 16
COMMON CONNECTION
CASE EARTH
MiCOM P645 (PART)
PHASE ROTATION
A
B
C
BIAS 1
BIAS 2
BIAS 3
BIAS 4
BIAS 5
I A (1)
I B (1)
I C (1)
I A (2)
I B (2)
I C (2)
I A (3)
I B (3)
I C (3)
I A (4)
I B (4)
I C (4)
I A (5)
I B (5)
I C (5)
P1
P2
S1
S2
NOTE 2
PROTECTEDTRANSFORMER
SEE SHEET 2 FOR NOTES
P4909ENa
10P64503_1

Figure 33 - Five bias input transformer differential (16 I/P & 16 O/P + CLIO) with 4 pole VT inputs (60TE)


MiCOM P645 (PART)
A
B
C
N
n
a
b
c
NOTE 9
NOTE 4
NOTE 8
NOTE 10
NOTE 3
D2
VA
D1
D4
VB
D3
F2
VC
F1
VN
F4
VFLUX
F3
OPTIONAL
D12
D11
/ Y (TV)
D14
D13
/ Y (LV)
D16
D15
/ Y (HV)
S1
S2
P1
P2
GROUNDED WYE
NEUTRAL TAILS
TV
LV
HV
VEE CONNECTED VTs (ALTERNATIVE)
MODULE TERMINAL BLOCK
VIEWED FROM REAR
1
2
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
P4910ENa
10P64503_2

P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +TV (x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV (x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

TABLE 1 (NOTES 5 & 6)

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
10. DERIVED NEUTRAL POINT. SEE P64X/ENT/- - FOR DETAILS OF RESISTORS.
11. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
    FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

Figure 34 - Five bias input transformer differential (16 I/P & 16 O/P + CLIO) with 4 pole VT inputs (60TE)

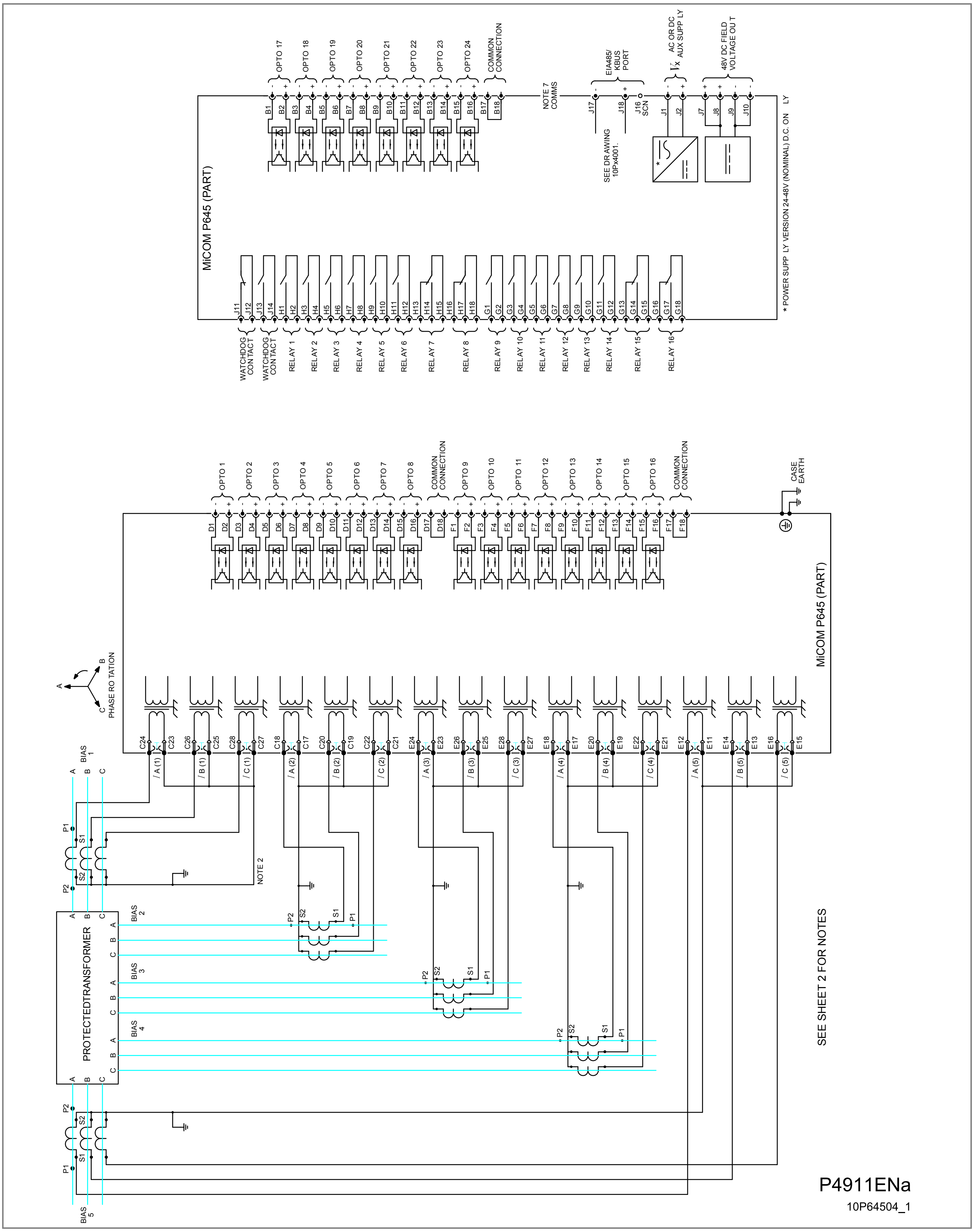
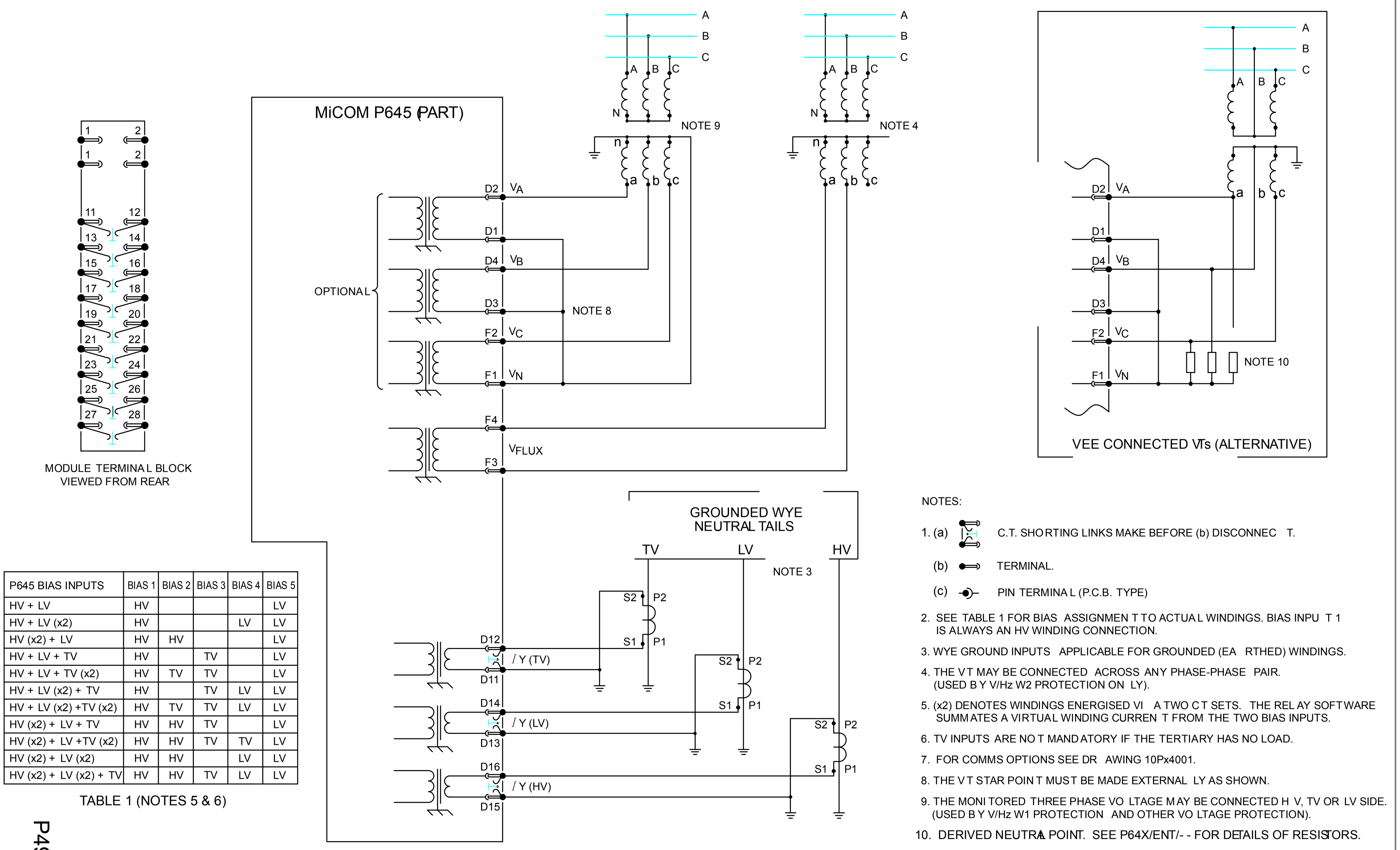

MiCOM P645 (PART)
OPTO 17
OPTO 18
OPTO 19
OPTO 20
OPTO 21
OPTO 22
OPTO 23
OPTO 24
COMMON CONNECTION
NOTE 7 COMMS
EIA485/ KBUS PORT
SEE DRAWING 10Px4001.
J16 SCN
AC OR DC AUX SUPPLY
Vx
48V DC FIELD VOLTAGE OUT
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
WATCHDOG CONTACT
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
RELAY 9
RELAY 10
RELAY 11
RELAY 12
RELAY 13
RELAY 14
RELAY 15
RELAY 16
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
OPTO 9
OPTO 10
OPTO 11
OPTO 12
OPTO 13
OPTO 14
OPTO 15
OPTO 16
COMMON CONNECTION
CASE EARTH
MiCOM P645 (PART)
PHASE ROTATION
A
B
C
BIAS 1
BIAS 2
BIAS 3
BIAS 4
BIAS 5
PROTECTED TRANSFORMER
NOTE 2
P1
P2
S1
S2
I A (1)
I B (1)
I C (1)
I A (2)
I B (2)
I C (2)
I A (3)
I B (3)
I C (3)
I A (4)
I B (4)
I C (4)
I A (5)
I B (5)
I C (5)
SEE SHEET 2 FOR NOTES
P4911ENa
10P64504_1

Figure 35 - Five bias input transformer differential (24 I/P & 16 O/P) with 4 pole VT inputs (60TE)


MiCOM P645 (PART)
OPTIONAL
D2 VA
D1
D4 VB
D3
F2 VC
F1 VN
F4
VFLUX
F3
NOTE 8
NOTE 9
NOTE 4
A
B
C
N
n
a
b
c
D12
D11
D14
D13
D16
D15
/ Y (TV)
/ Y (LV)
/ Y (HV)
GROUNDED WYE
NEUTRAL TAILS
TV
LV
HV
NOTE 3
S1
S2
P1
P2
VEE CONNECTED VTs (ALTERNATIVE)
NOTE 10
MODULE TERMINAL BLOCK
VIEWED FROM REAR
1
2
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
P4912ENa
10P64504_2

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
10. DERIVED NEUTRAL POINT. SEE P64X/ENT/- - FOR DETAILS OF RESISTORS.

P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +TV (x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV (x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

TABLE 1 (NOTES 5 & 6)

Figure 36 - Five bias input transformer differential (24 I/P & 16 O/P) with 4 pole VT inputs (60TE)

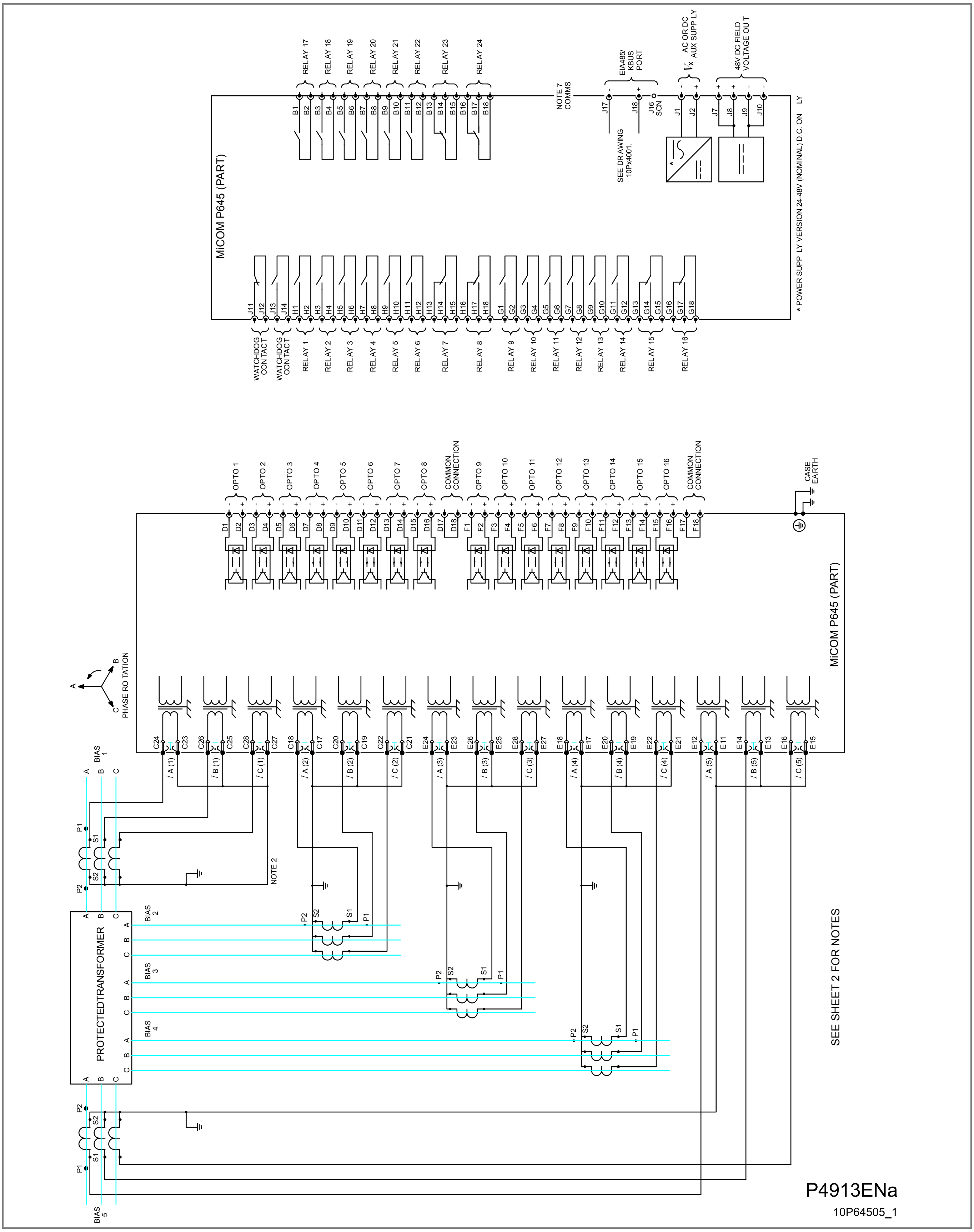
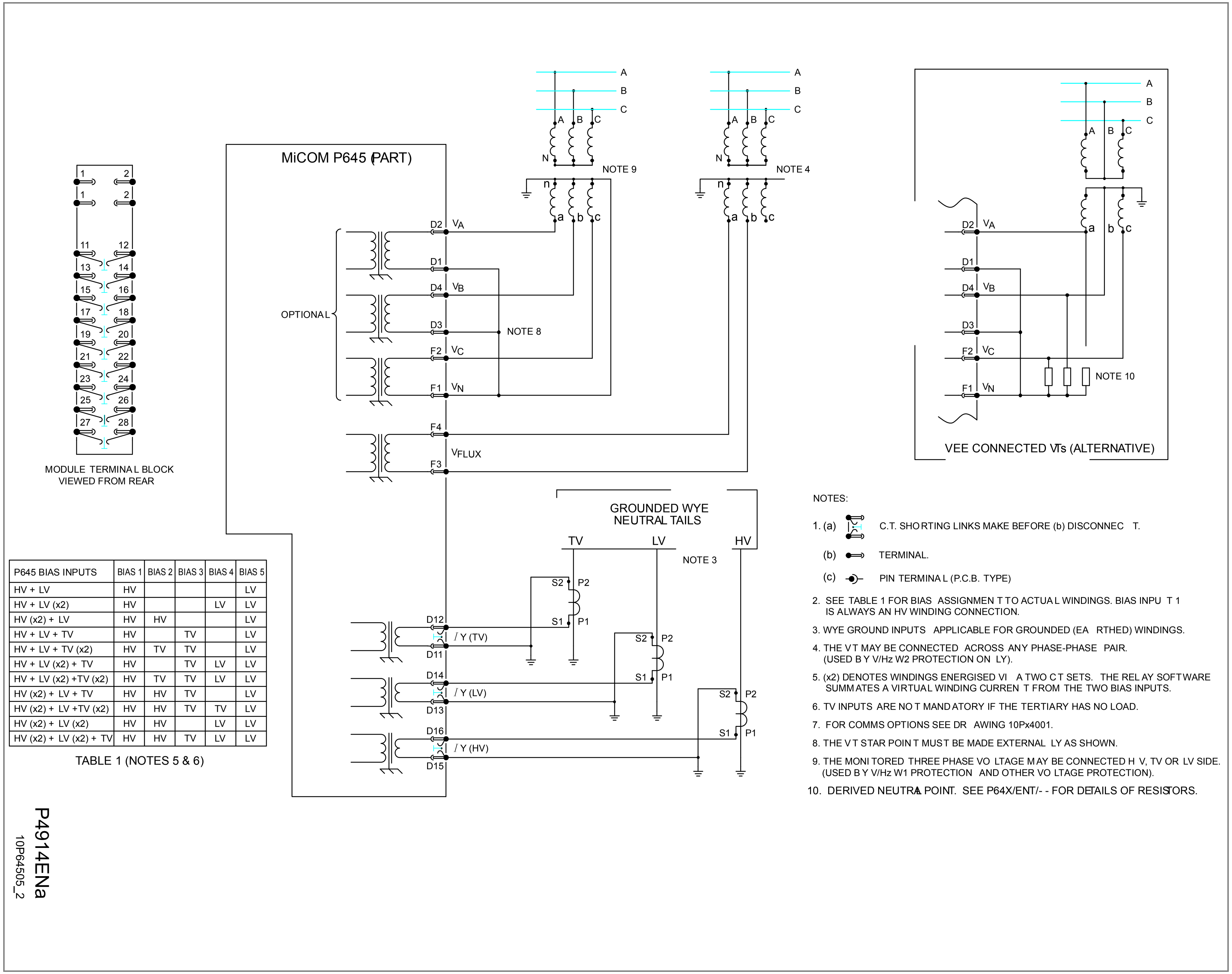

MiCOM P645 (PART)
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
RELAY 9
RELAY 10
RELAY 11
RELAY 12
RELAY 13
RELAY 14
RELAY 15
RELAY 16
RELAY 17
RELAY 18
RELAY 19
RELAY 20
RELAY 21
RELAY 22
RELAY 23
RELAY 24
NOTE 7 COMMS
EIA485/ KBUS PORT
SEE DRAWING 10Px4001
SCN
AC OR DC AUX SUPPLY Vx
48V DC FIELD VOLTAGE OUT
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
OPTO 9
OPTO 10
OPTO 11
OPTO 12
OPTO 13
OPTO 14
OPTO 15
OPTO 16
COMMON CONNECTION
CASE EARTH
PHASE ROTATION
BIAS 1
BIAS 2
BIAS 3
BIAS 4
BIAS 5
PROTECTEDTRANSFORMER
NOTE 2
P1
P2
S1
S2
SEE SHEET 2 FOR NOTES
P4913ENa
10P64505_1

Figure 37 - Five bias input transformer differential (16 I/O & 24 O/P) with 4 pole VT inputs (60TE)


A
B
C
N
n
a
b
c
NOTE 9
NOTE 4
MiCOM P645 (PART)
D2
V_A
D1
D4
V_B
D3
NOTE 8
F2
V_C
F1
V_N
OPTIONAL
F4
V_{FLUX}
F3
VEE CONNECTED VTs (ALTERNATIVE)
NOTE 10
GROUNDED WYE NEUTRAL TAILS
TV
LV
HV
NOTE 3
S2
P2
S1
P1
D12
D11
/ Y (TV)
D14
D13
/ Y (LV)
D16
D15
/ Y (HV)
MODULE TERMINAL BLOCK VIEWED FROM REAR
1
2
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
P4914ENa
10P64505_2

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.

   (b) TERMINAL.

   (c) PIN TERMINAL (P.C.B. TYPE)

2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
10. DERIVED NEUTRAL POINT. SEE P64X/ENT/- - FOR DETAILS OF RESISTORS.

P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +TV (x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV (x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

TABLE 1 (NOTES 5 & 6)

Figure 38 - Five bias input transformer differential (16 I/P & 24 O/P) with 4 pole VT inputs (60TE)

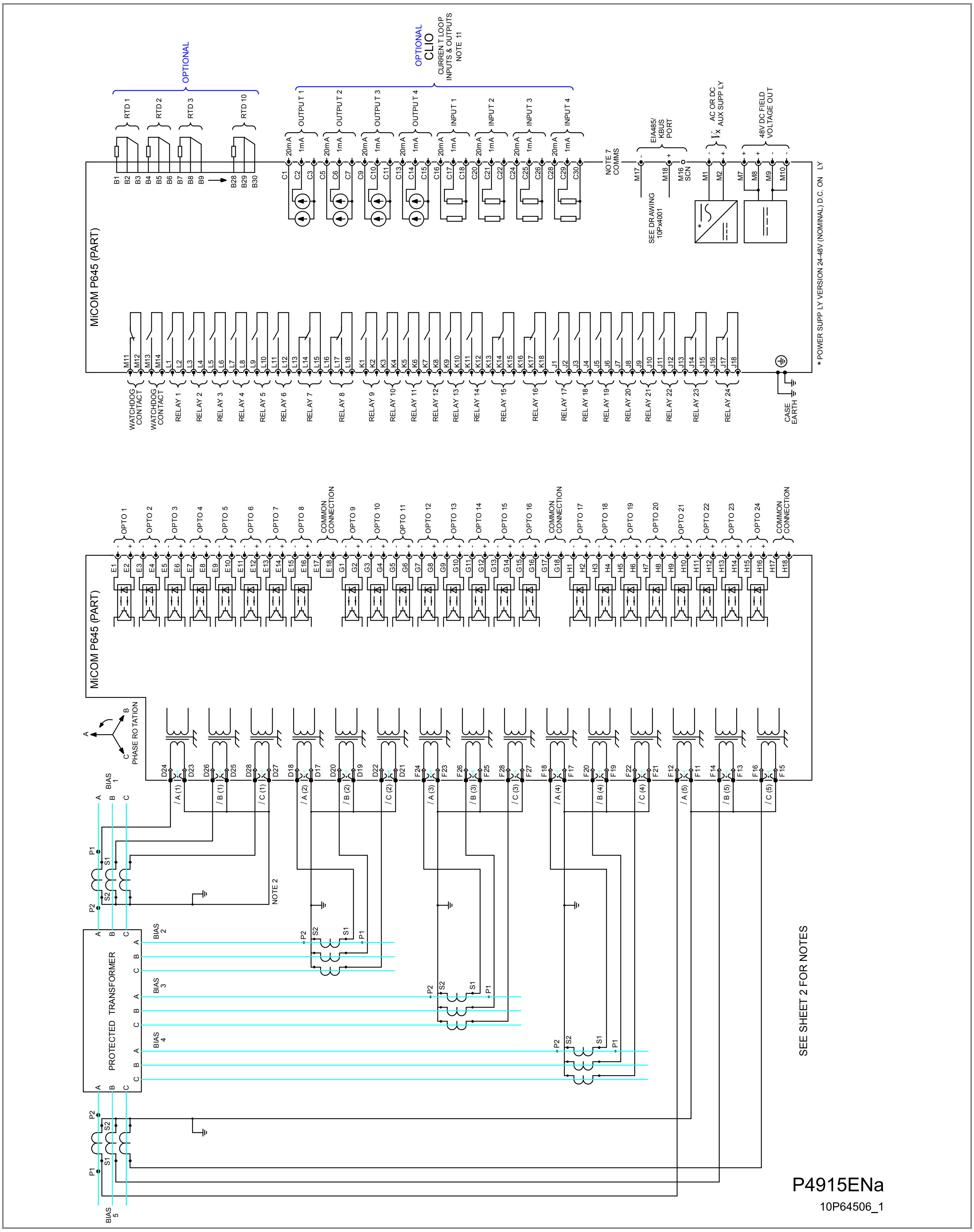
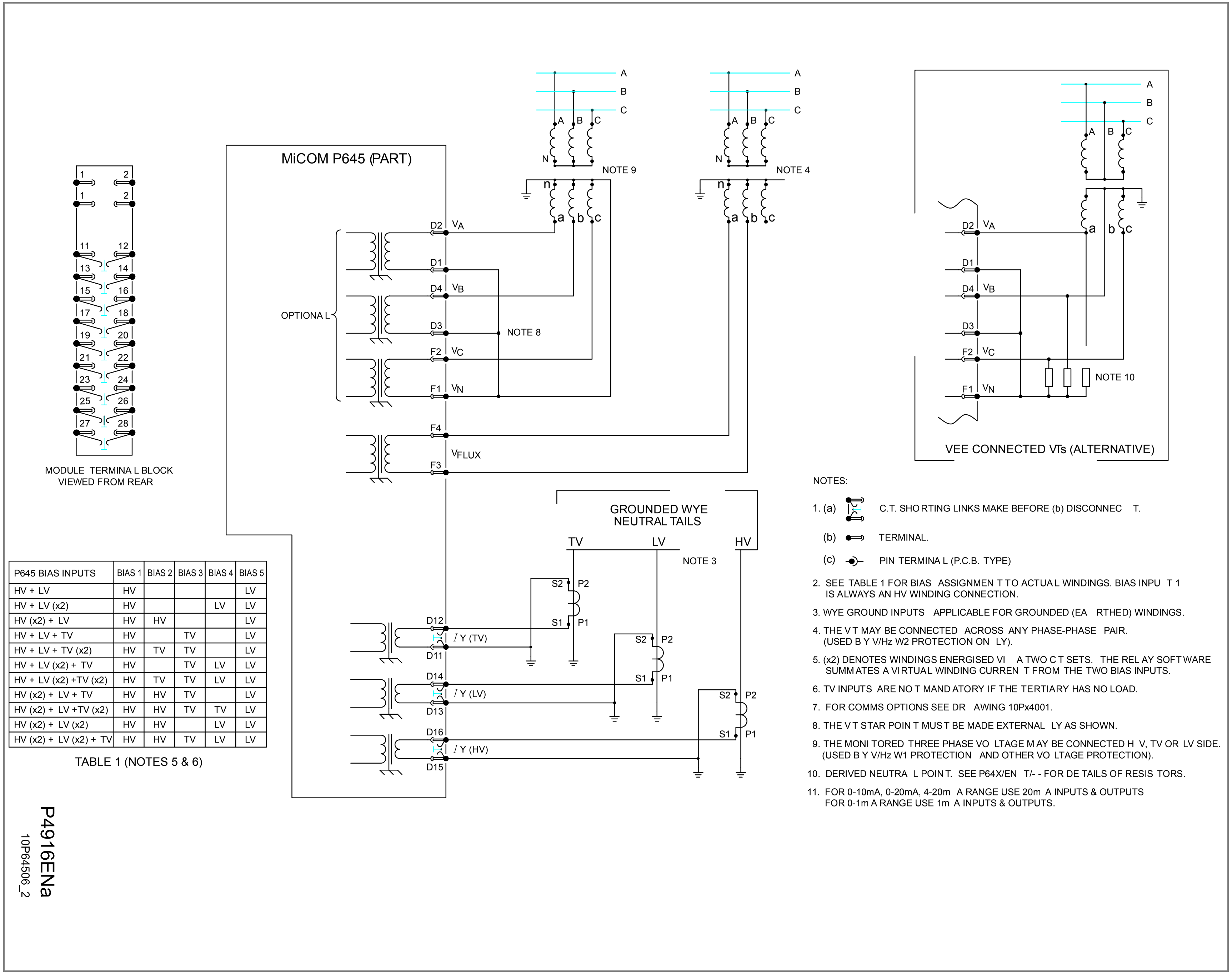

MiCOM P645 (PART)
OPTIONAL
RTD 1
RTD 2
RTD 3
RTD 10
OPTIONAL
CLIO
CURRENT LOOP
INPUTS & OUTPUTS
NOTE 11
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
INPUT 1
INPUT 2
INPUT 3
INPUT 4
20mA
1mA
NOTE 7
COMMS
EIA485/
KBUS
PORT
SEE DRAWING
10Px4001
M16
SCN
AC OR DC
AUX SUPP LY
48V DC FIELD
VOLTAGE OUT
* POWER SUPP LY VERSION 24-48V (NOMINAL) D.C. ON LY
WATCHDOG
CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
RELAY 9
RELAY 10
RELAY 11
RELAY 12
RELAY 13
RELAY 14
RELAY 15
RELAY 16
RELAY 17
RELAY 18
RELAY 19
RELAY 20
RELAY 21
RELAY 22
RELAY 23
RELAY 24
CASE
EARTH
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON
CONNECTION
OPTO 9
OPTO 10
OPTO 11
OPTO 12
OPTO 13
OPTO 14
OPTO 15
OPTO 16
OPTO 17
OPTO 18
OPTO 19
OPTO 20
OPTO 21
OPTO 22
OPTO 23
OPTO 24
PHASE ROTATION
BIAS 1
BIAS 2
BIAS 3
BIAS 4
BIAS 5
NOTE 2
PROTECTED TRANSFORMER
P1
P2
S1
S2
SEE SHEET 2 FOR NOTES
P4915ENa
10P64506_1

Figure 39 - Five bias input transformer differential (24 I/P & 24 O/P + CLIO & RTD) with 4 pole VT inputs (80TE)


MiCOM P645 (PART)
A
B
C
N
n
a
b
c
NOTE 9
NOTE 4
NOTE 8
NOTE 10
NOTE 3
D2
D1
D4
D3
F2
F1
F4
F3
VA
VB
VC
VN
VFLUX
OPTIONAL
D12
D11
D14
D13
D16
D15
/ Y (TV)
/ Y (LV)
/ Y (HV)
GROUNDED WYE
NEUTRAL TAILS
TV
LV
HV
S1
S2
P1
P2
VEE CONNECTED VTs (ALTERNATIVE)
MODULE TERMINAL BLOCK
VIEWED FROM REAR
1
2
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
P4916ENa
10P64506_2

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.

(b) TERMINAL.

(c) PIN TERMINAL (P.C.B. TYPE)

2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.

3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.

4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).

5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.

6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.

7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.

8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.

9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).

10. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.

11. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS
FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +TV (x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV (x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

TABLE 1 (NOTES 5 & 6)

Figure 40 - Five bias input transformer differential (24 I/O & 24 O/P + CLIO & RTD) with 4 pole VT inputs (80TE)

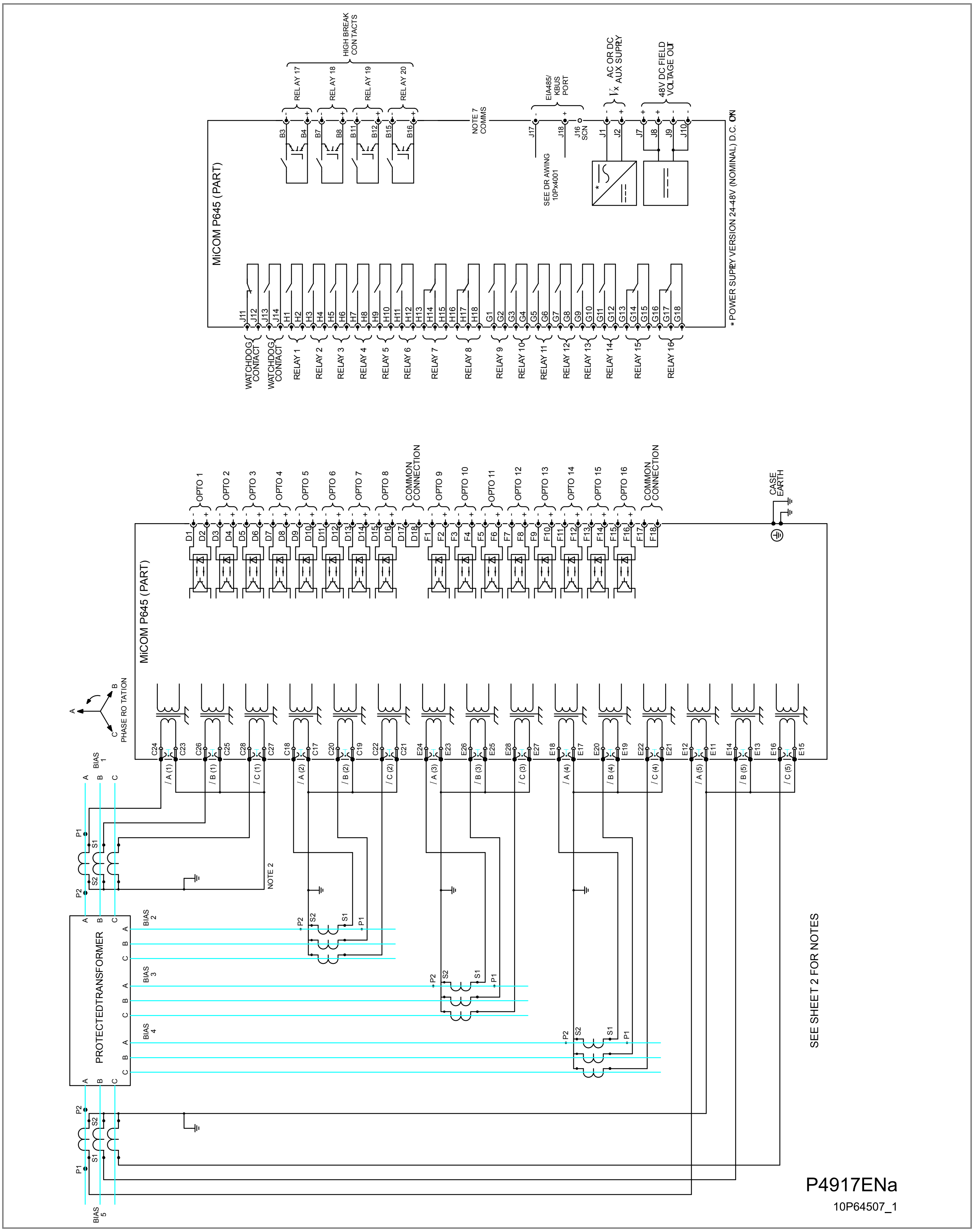
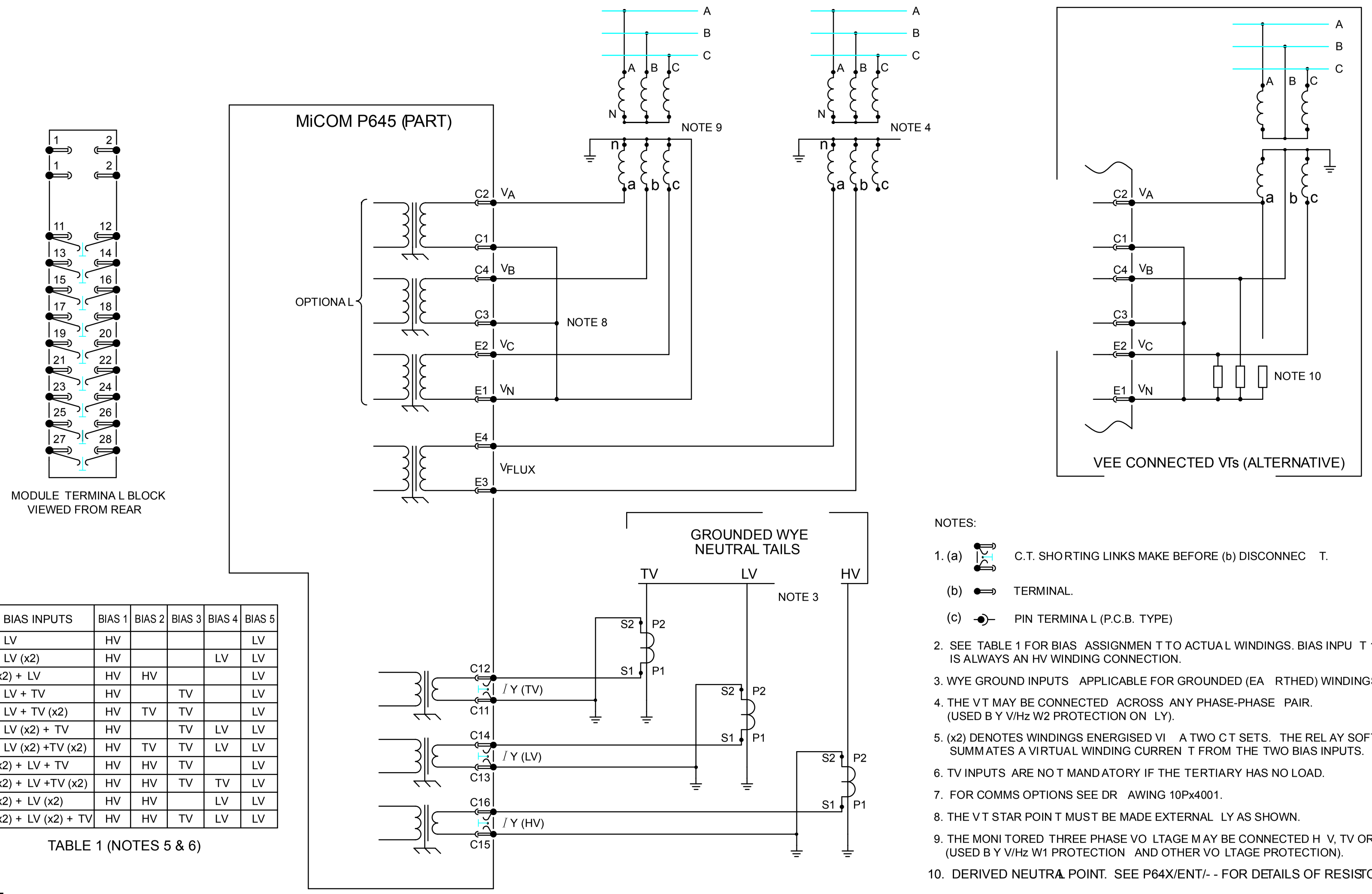

MiCOM P645 (PART)
HIGH BREAK CONTACTS
RELAY 17
RELAY 18
RELAY 19
RELAY 20
NOTE 7 COMMS
EIA485/ KBUS PORT
SEE DRAWING 10Px4001
J16 SCN
AC OR DC AUX SUPPLY
Vx
48V DC FIELD VOLTAGE OUT
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ONLY
WATCHDOG CONTACT
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
RELAY 9
RELAY 10
RELAY 11
RELAY 12
RELAY 13
RELAY 14
RELAY 15
RELAY 16
MiCOM P645 (PART)
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
OPTO 9
OPTO 10
OPTO 11
OPTO 12
OPTO 13
OPTO 14
OPTO 15
OPTO 16
COMMON CONNECTION
CASE EARTH
PHASE ROTATION
A B C
BIAS 1
BIAS 2
BIAS 3
BIAS 4
BIAS 5
PROTECTED TRANSFORMER
P1 P2 S1 S2
NOTE 2
SEE SHEET 2 FOR NOTES
P4917ENa
10P64507_1

Figure 41 - Five bias input transformer differential (24 I/P & 20 O/P) with 4 pole VT input (60TE)


MiCOM P645 (PART)
A
B
C
N
n
a
b
c
NOTE 9
NOTE 4
NOTE 8
NOTE 10
NOTE 3
C2
C1
C4
C3
E2
E1
E4
E3
V_A
V_B
V_C
V_N
V_{FLUX}
OPTIONAL
VEE CONNECTED VTs (ALTERNATIVE)
GROUNDED WYE NEUTRAL TAILS
TV
LV
HV
S2
P2
S1
P1
C12
C11
C14
C13
C16
C15
/ Y (TV)
/ Y (LV)
/ Y (HV)
1
2
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
MODULE TERMINAL BLOCK VIEWED FROM REAR

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
10. DERIVED NEUTRAL POINT. SEE P64X/ENT/- - FOR DETAILS OF RESISTORS.

P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +TV (x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV (x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

TABLE 1 (NOTES 5 & 6)

P4918ENa

10P64507_2

Figure 42 - Five bias input transformer differential (24 I/P & 20 O/P) with 4 pole VT input (60TE)

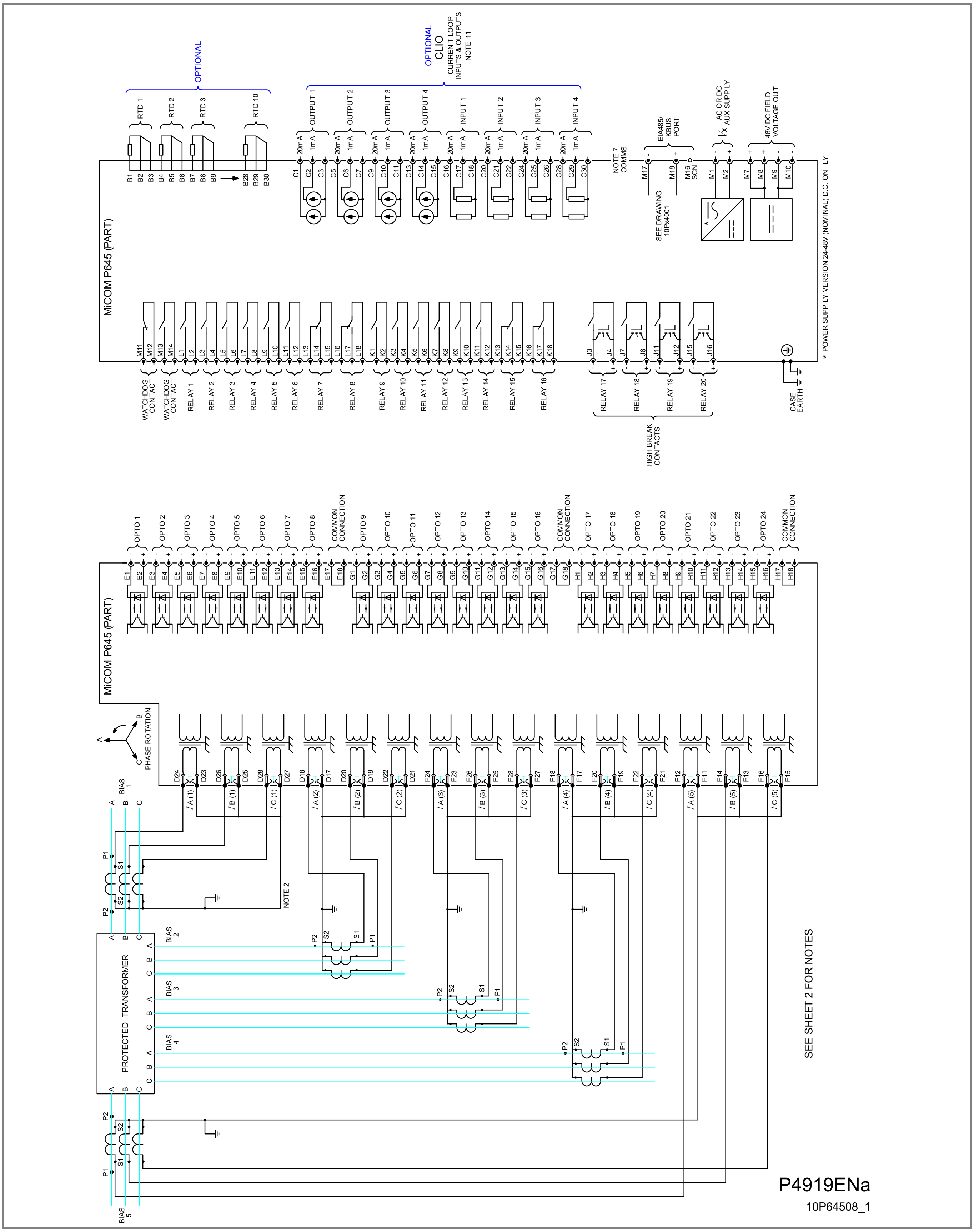
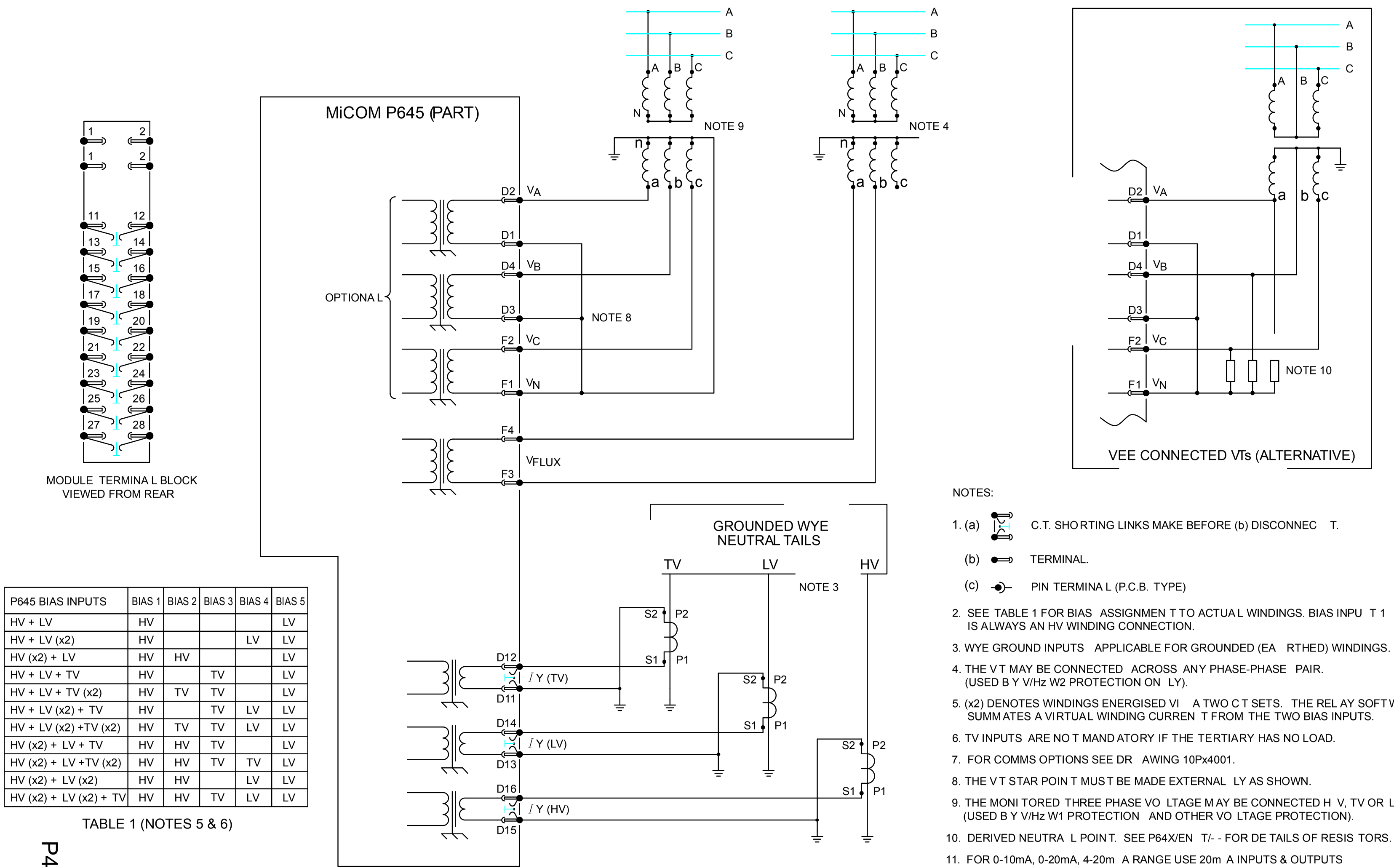

MiCOM P645 (PART)
OPTIONAL
RTD 1
RTD 2
RTD 3
RTD 10
OPTIONAL
CLIO
CURRENT LOOP INPUTS & OUTPUTS
NOTE 11
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
INPUT 1
INPUT 2
INPUT 3
INPUT 4
20mA
1mA
NOTE 7
COMMS
EIA485/ KBUS PORT
SEE DRAWING 10Px4001
M16 SCN
AC OR DC AUX SUPP LY
48V DC FIELD VOLTAGE OUT
* POWER SUPP LY VERSION 24-48V (NOMINAL) D.C. ON LY
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
RELAY 9
RELAY 10
RELAY 11
RELAY 12
RELAY 13
RELAY 14
RELAY 15
RELAY 16
RELAY 17
RELAY 18
RELAY 19
RELAY 20
HIGH BREAK CONTACTS
CASE EARTH
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
OPTO 9
OPTO 10
OPTO 11
OPTO 12
OPTO 13
OPTO 14
OPTO 15
OPTO 16
OPTO 17
OPTO 18
OPTO 19
OPTO 20
OPTO 21
OPTO 22
OPTO 23
OPTO 24
PHASE ROTATION
A
B
C
BIAS 1
BIAS 2
BIAS 3
BIAS 4
BIAS 5
I A (1)
I B (1)
I C (1)
I A (2)
I B (2)
I C (2)
I A (3)
I B (3)
I C (3)
I A (4)
I B (4)
I C (4)
I A (5)
I B (5)
I C (5)
P1
P2
S1
S2
NOTE 2
PROTECTED TRANSFORMER
SEE SHEET 2 FOR NOTES
P4919ENa
10P64508_1

Figure 43 - Five bias input transformer differential (24 I/P & 20 O/P + CLIO & RTD) with 4 pole VT input (80TE)


MiCOM P645 (PART)
A
B
C
N
n
a
b
c
NOTE 9
NOTE 4
D2
VA
D1
D4
VB
D3
F2
VC
F1
VN
F4
VFLUX
F3
OPTIONAL
NOTE 8
GROUNDED WYE NEUTRAL TAILS
TV
LV
HV
NOTE 3
S2
P2
S1
P1
D12
/ Y (TV)
D11
D14
/ Y (LV)
D13
D16
/ Y (HV)
D15
NOTE 10
VEE CONNECTED VTs (ALTERNATIVE)
1
2
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
MODULE TERMINAL BLOCK VIEWED FROM REAR

NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
10. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
11. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +TV (x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV (x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

TABLE 1 (NOTES 5 & 6)

P4920ENa
10P64508_2

Figure 44 - Five bias input transformer differential (24 I/P & 20 O/P + CLIO & RTD) with 4 pole VT input (80TE)

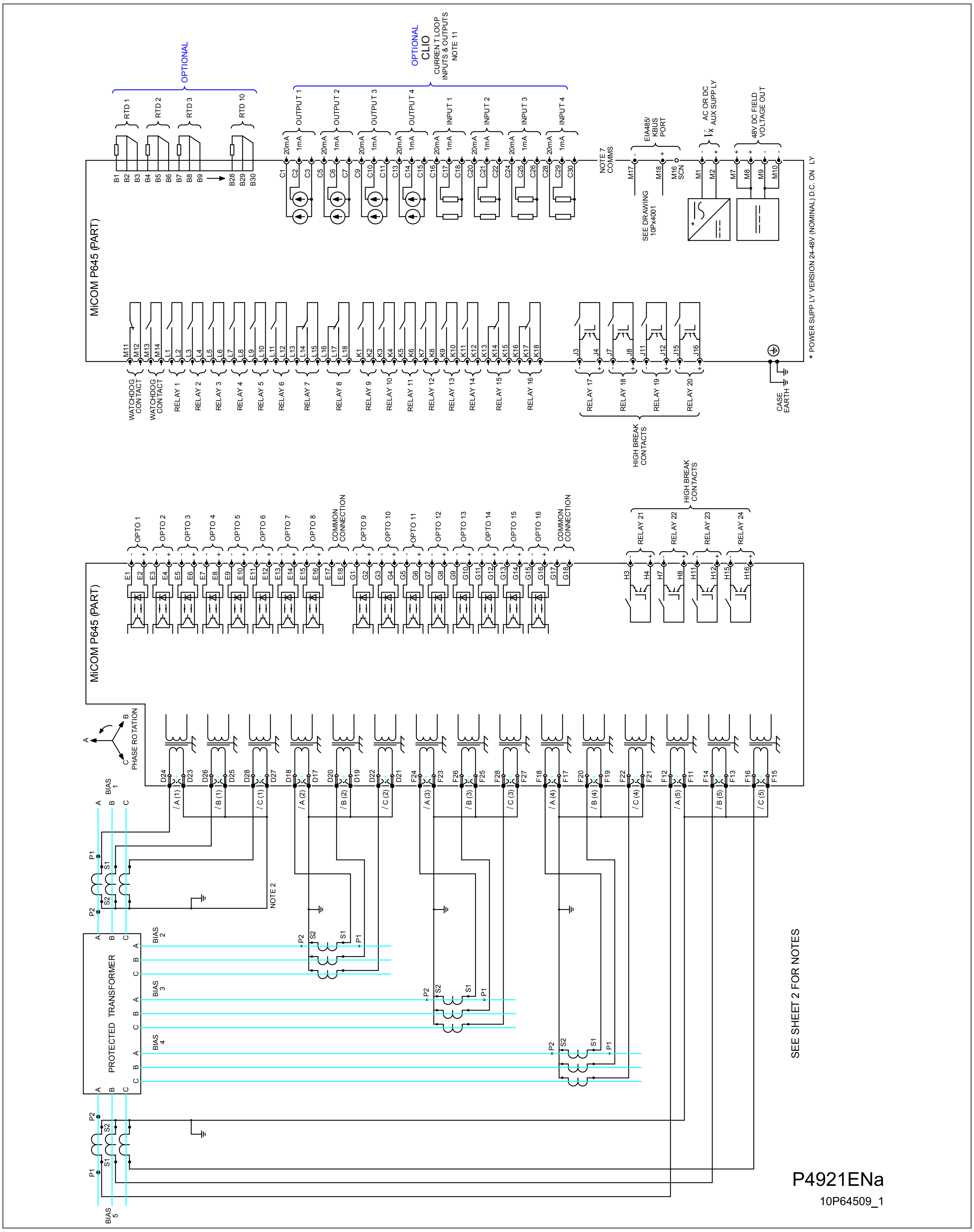
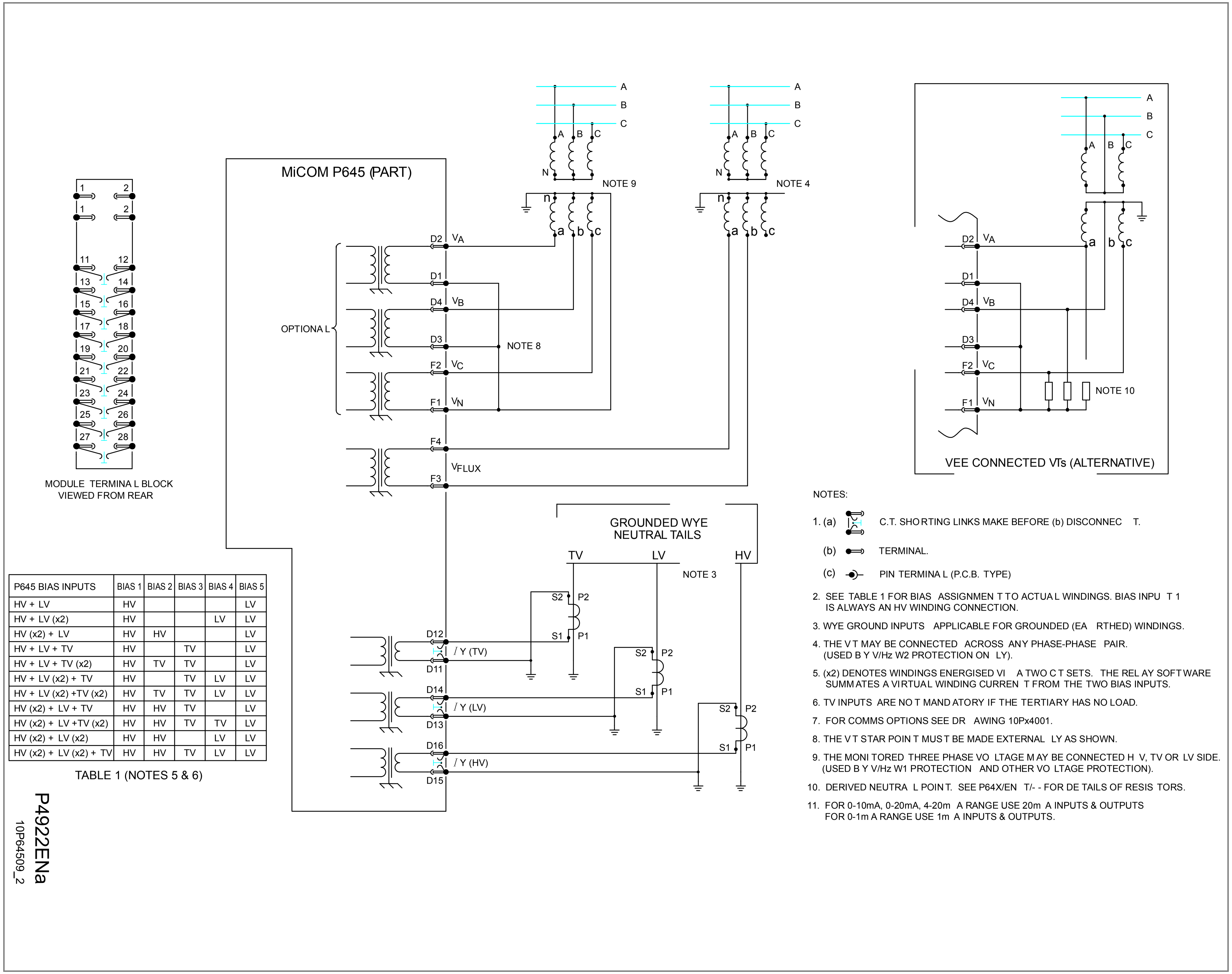

MiCOM P645 (PART)
OPTIONAL
RTD 1
RTD 2
RTD 3
RTD 10
OPTIONAL CLIO CURRENT LOOP INPUTS & OUTPUTS NOTE 11
OUTPUT 1
OUTPUT 2
OUTPUT 3
OUTPUT 4
INPUT 1
INPUT 2
INPUT 3
INPUT 4
20mA
1mA
NOTE 7 COMMS
EIA485/ KBUS PORT
SEE DRAWING 10Px4001
M16 SCN
AC OR DC AUX SUPPLY
48V DC FIELD VOLTAGE OUT
* POWER SUPPLY VERSION 24-48V (NOMINAL) D.C. ON LY
WATCHDOG CONTACT
RELAY 1
RELAY 2
RELAY 3
RELAY 4
RELAY 5
RELAY 6
RELAY 7
RELAY 8
RELAY 9
RELAY 10
RELAY 11
RELAY 12
RELAY 13
RELAY 14
RELAY 15
RELAY 16
RELAY 17
RELAY 18
RELAY 19
RELAY 20
HIGH BREAK CONTACTS
CASE EARTH
OPTO 1
OPTO 2
OPTO 3
OPTO 4
OPTO 5
OPTO 6
OPTO 7
OPTO 8
COMMON CONNECTION
OPTO 9
OPTO 10
OPTO 11
OPTO 12
OPTO 13
OPTO 14
OPTO 15
OPTO 16
RELAY 21
RELAY 22
RELAY 23
RELAY 24
PHASE ROTATION
A
B
C
BIAS 1
BIAS 2
BIAS 3
BIAS 4
BIAS 5
P1
P2
S1
S2
NOTE 2
PROTECTED TRANSFORMER
IA (1)
IB (1)
IC (1)
IA (2)
IB (2)
IC (2)
IA (3)
IB (3)
IC (3)
IA (4)
IB (4)
IC (4)
IA (5)
IB (5)
IC (5)
SEE SHEET 2 FOR NOTES
P4921ENa
10P64509_1

Figure 45 - Five bias input transformer differential (16 I/P & 24 O/P + CLIO & RTD) with 4 pole VT input (80TE)


MiCOM P645 (PART)
A
B
C
N
NOTE 9
NOTE 4
n
a
b
c
D2
VA
D1
D4
VB
D3
F2
VC
F1
VN
F4
VFLUX
F3
OPTIONAL
NOTE 8
VEE CONNECTED VTs (ALTERNATIVE)
NOTE 10
GROUNDED WYE NEUTRAL TAILS
TV
LV
HV
NOTE 3
S1
S2
P1
P2
D12
D11
D14
D13
D16
D15
/ Y (TV)
/ Y (LV)
/ Y (HV)
MODULE TERMINAL BLOCK VIEWED FROM REAR
1
2
11
12
13
14
15
16
17
18
19
20
21
22
23
24
25
26
27
28
P4922ENa
10P64509_2

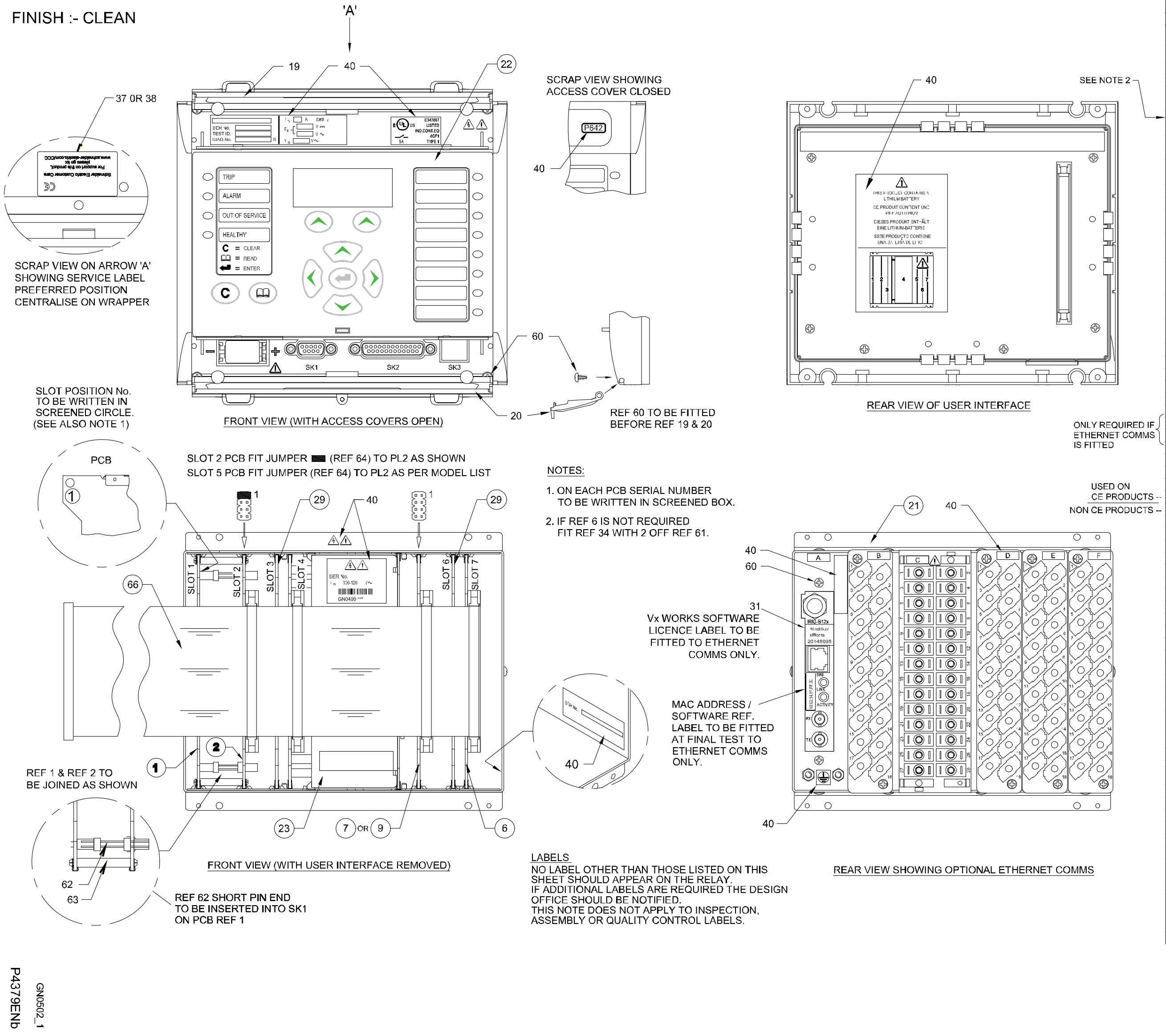
NOTES:

1. (a) C.T. SHORTING LINKS MAKE BEFORE (b) DISCONNECT.
   (b) TERMINAL.
   (c) PIN TERMINAL (P.C.B. TYPE)
2. SEE TABLE 1 FOR BIAS ASSIGNMENT TO ACTUAL WINDINGS. BIAS INPUT 1 IS ALWAYS AN HV WINDING CONNECTION.
3. WYE GROUND INPUTS APPLICABLE FOR GROUNDED (EARTHED) WINDINGS.
4. THE VT MAY BE CONNECTED ACROSS ANY PHASE-PHASE PAIR. (USED BY V/Hz W2 PROTECTION ONLY).
5. (x2) DENOTES WINDINGS ENERGISED VIA TWO CT SETS. THE RELAY SOFTWARE SUMMATES A VIRTUAL WINDING CURRENT FROM THE TWO BIAS INPUTS.
6. TV INPUTS ARE NOT MANDATORY IF THE TERTIARY HAS NO LOAD.
7. FOR COMMS OPTIONS SEE DRAWING 10Px4001.
8. THE VT STAR POINT MUST BE MADE EXTERNALLY AS SHOWN.
9. THE MONITORED THREE PHASE VOLTAGE MAY BE CONNECTED HV, TV OR LV SIDE. (USED BY V/Hz W1 PROTECTION AND OTHER VOLTAGE PROTECTION).
10. DERIVED NEUTRAL POINT. SEE P64X/EN T/- - FOR DETAILS OF RESISTORS.
11. FOR 0-10mA, 0-20mA, 4-20mA RANGE USE 20mA INPUTS & OUTPUTS FOR 0-1mA RANGE USE 1mA INPUTS & OUTPUTS.

P645 BIAS INPUTS	BIAS 1	BIAS 2	BIAS 3	BIAS 4	BIAS 5
HV + LV	HV				LV
HV + LV (x2)	HV			LV	LV
HV (x2) + LV	HV	HV			LV
HV + LV + TV	HV		TV		LV
HV + LV + TV (x2)	HV	TV	TV		LV
HV + LV (x2) + TV	HV		TV	LV	LV
HV + LV (x2) +TV (x2)	HV	TV	TV	LV	LV
HV (x2) + LV + TV	HV	HV	TV		LV
HV (x2) + LV +TV (x2)	HV	HV	TV	TV	LV
HV (x2) + LV (x2)	HV	HV		LV	LV
HV (x2) + LV (x2) + TV	HV	HV	TV	LV	LV

TABLE 1 (NOTES 5 & 6)

Figure 46 - Five bias input transformer differential (16 I/P & 24 O/P + CLIO & RTD) with 4 pole VT input (80TE)


FINISH :- CLEAN
'A'
19
40
22
37 0R 38
TRIP
ALARM
OUT OF SERVICE
HEALTHY
C = CLEAR
= READ
= ENTER
SK1
SK2
SK3
SCRAP VIEW ON ARROW 'A' SHOWING SERVICE LABEL PREFERRED POSITION CENTRALISE ON WRAPPER
FRONT VIEW (WITH ACCESS COVERS OPEN)
SCRAP VIEW SHOWING ACCESS COVER CLOSED
P642
40
60
20
REF 60 TO BE FITTED BEFORE REF 19 & 20
40
SEE NOTE 2
REAR VIEW OF USER INTERFACE
ONLY REQUIRED IF ETHERNET COMMS IS FITTED
USED ON CE PRODUCTS --
NON CE PRODUCTS --
SLOT POSITION No. TO BE WRITTEN IN SCREENED CIRCLE. (SEE ALSO NOTE 1)
PCB
1
SLOT 2 PCB FIT JUMPER (REF 64) TO PL2 AS SHOWN
SLOT 5 PCB FIT JUMPER (REF 64) TO PL2 AS PER MODEL LIST
29
40
SLOT 1
SLOT 2
SLOT 3
SLOT 4
SLOT 6
SLOT 7
66
1
2
REF 1 & REF 2 TO BE JOINED AS SHOWN
62
63
REF 62 SHORT PIN END TO BE INSERTED INTO SK1 ON PCB REF 1
23
7 OR 9
6
FRONT VIEW (WITH USER INTERFACE REMOVED)
40
21
40
60
31
Vx WORKS SOFTWARE LICENCE LABEL TO BE FITTED TO ETHERNET COMMS ONLY.
MAC ADDRESS / SOFTWARE REF. LABEL TO BE FITTED AT FINAL TEST TO ETHERNET COMMS ONLY.
A
B
C
D
E
F
40
REAR VIEW SHOWING OPTIONAL ETHERNET COMMS
GN0502_1
P4379ENb

NOTES:

1. ON EACH PCB SERIAL NUMBER TO BE WRITTEN IN SCREENED BOX.
2. IF REF 6 IS NOT REQUIRED FIT REF 34 WITH 2 OFF REF 61.

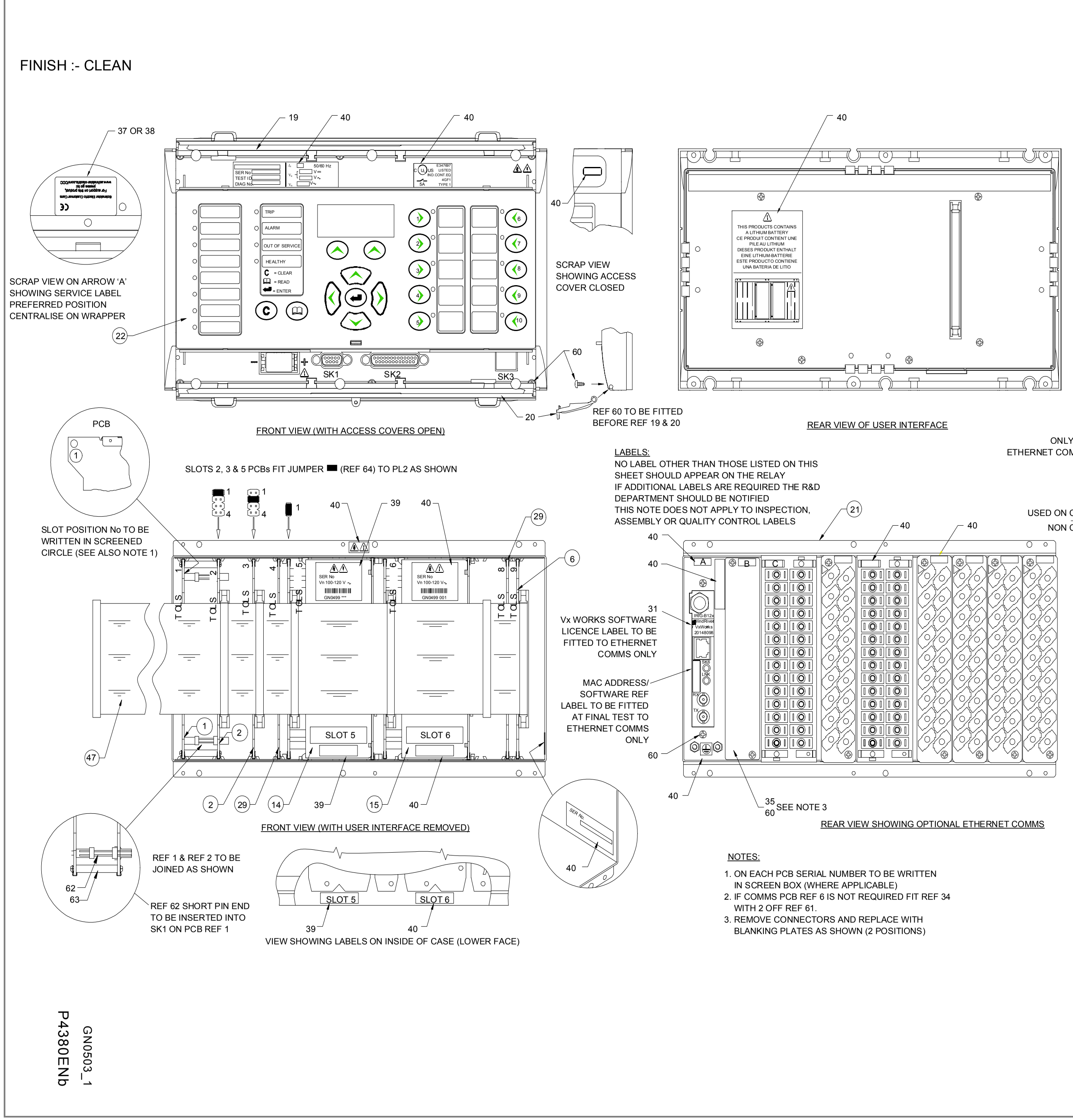
LABELS

NO LABEL OTHER THAN THOSE LISTED ON THIS SHEET SHOULD APPEAR ON THE RELAY. IF ADDITIONAL LABELS ARE REQUIRED THE DESIGN OFFICE SHOULD BE NOTIFIED. THIS NOTE DOES NOT APPLY TO INSPECTION, ASSEMBLY OR QUALITY CONTROL LABELS.

	PART	DESCRIPTION OF ASSEMBLY	
	***	P642 TRANSFORMER PROTECTION RELAY	
QTY	REF	DESCRIPTION	MATERIAL
1	1	ASSY POWER SUPPLY	2071964 ***
1	2	ASSY RELAY OUTPUT	2071962A01
	3		
	4		
	5		
*	6	ASSY PCB (COMMS)	ZN **** ***
*	7	ASSY RELAY OUTPUT/OPTO INPUT	ZN0028 011
	8		
*	9	ASSY HIGH BREAK RELAY OUTPUT	ZN0042 001
	10		
	11		
	12		
	13		
	14		
	15		
	16		
	17		
	18		
1	19	TOP ACCESS COVER	GN6003 003
1	20	BOTTOM ACCESS COVER	GN6003 002
1	21	ASSY CASE	GN0495 002
1	22	ASSY USER INTERFACE	2072033 ***
1	23	ASSY STANDARD INPUT MODULE	2072043 ***
	24		
	25		
	26		
	27		
	27		
2	29	ASSEMBLY SCREEN PLATE	GN0058 001
	30		
*	31	Vx WORKS SOFTWARE	ZB9800 801
*	32	MMS-EASE LITE SOFTWARE	ZB9800 802
	33		
*	34	BLANKING PLATE	GN2037 001
	35		
	36		
1 OR	37	WORLDWIDE SERVICE LABEL CE M'KED	ZF8560 001-S
1	38	WORLDWIDE SERVICE LABEL NON CE	ZF8560 002-S
	39		
1	40	LABEL SHEET - 40TE	GN9011 003
	41		
	42		
	43		
	44		
	45		
	46		
	47		
	48		
	49		
	50		
	51		
	52		
	53		
	54		
	55		
	56		
	57		
	58		
	59		
*	60	SELF-TAPPING PAN HEAD No4x1/4"	ZB4018 110
*	61	SELF-TAPPING PAN HEAD No6x1/4"	ZB4018 215
1	62	HEADER	ZB9031 985
4	63	SPACER	ZB8011 213
*	64	JUMPER	ZB9031 759
	65		
1	66	ASSY RIBBON CABLE	GN0009 002
	67		
1	68	CUSTOM LED INDICATOR LABEL	GN9025 015
1	69	BAGGED ITEMS - LABELS	GN9002 001-S
4	70	BAGGED ITEMS - TERMINAL SCREWS	ZA0005 060
1	71	BAGGED ITEMS - FIXING SCREWS	ZA0005 105
	72		
	73		

Figure 47 - P642 assembly relay (40TE)

FINISH :- CLEAN


37 OR 38
19
40
40
40
SCRAP VIEW ON ARROW 'A'
SHOWING SERVICE LABEL
PREFERRED POSITION
CENTRALISE ON WRAPPER
22
TRIP
ALARM
OUT OF SERVICE
HEALTHY
C = CLEAR
= READ
= ENTER
SK1
SK2
SK3
60
20
SCRAP VIEW
SHOWING ACCESS
COVER CLOSED
REF 60 TO BE FITTED
BEFORE REF 19 & 20
FRONT VIEW (WITH ACCESS COVERS OPEN)
REAR VIEW OF USER INTERFACE
THIS PRODUCTS CONTAINS A LITHIUM BATTERY
CE PRODUIT CONTIENT UNE PILE AU LITHIUM
DIESES PRODUKT ENTHALT EINE LITHIUM-BATTERIE
ESTE PRODUCTO CONTIENE UNA BATERIA DE LITIO
PCB
1
SLOT POSITION No TO BE
WRITTEN IN SCREENED
CIRCLE (SEE ALSO NOTE 1)
SLOTS 2, 3 & 5 PCBs FIT JUMPER ■ (REF 64) TO PL2 AS SHOWN
1
4
39
29
6
SER No
Vn 100-120 V
GN0499 001
SLOT 5
SLOT 6
47
2
29
14
15
REF 1 & REF 2 TO BE
JOINED AS SHOWN
62
63
REF 62 SHORT PIN END
TO BE INSERTED INTO
SK1 ON PCB REF 1
FRONT VIEW (WITH USER INTERFACE REMOVED)
VIEW SHOWING LABELS ON INSIDE OF CASE (LOWER FACE)
LABELS:
NO LABEL OTHER THAN THOSE LISTED ON THIS
SHEET SHOULD APPEAR ON THE RELAY
IF ADDITIONAL LABELS ARE REQUIRED THE R&D
DEPARTMENT SHOULD BE NOTIFIED
THIS NOTE DOES NOT APPLY TO INSPECTION,
ASSEMBLY OR QUALITY CONTROL LABELS
21
A
B
C
31
Vx WORKS SOFTWARE
LICENCE LABEL TO BE
FITTED TO ETHERNET
COMMS ONLY
MAC ADDRESS/
SOFTWARE REF
LABEL TO BE FITTED
AT FINAL TEST TO
ETHERNET COMMS
ONLY
35
60 SEE NOTE 3
REAR VIEW SHOWING OPTIONAL ETHERNET COMMS
SER No
GN0503_1
P4380ENb

NOTES:

1. ON EACH PCB SERIAL NUMBER TO BE WRITTEN IN SCREEN BOX (WHERE APPLICABLE)
2. IF COMMS PCB REF 6 IS NOT REQUIRED FIT REF 34 WITH 2 OFF REF 61.
3. REMOVE CONNECTORS AND REPLACE WITH BLANKING PLATES AS SHOWN (2 POSITIONS)

SEE NOTE 2 → (REF 6)

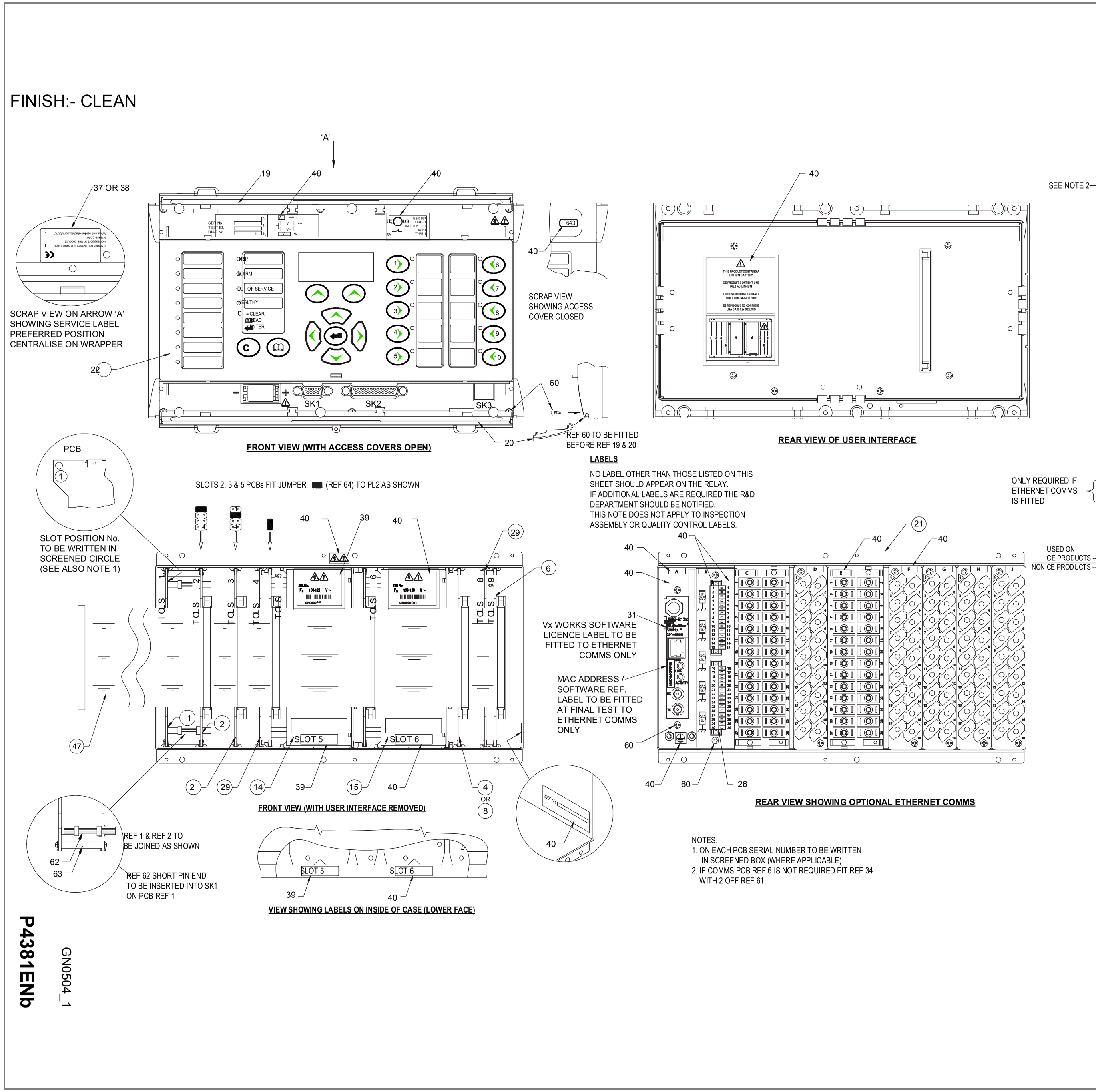
ONLY REQUIRED IF ETHERNET COMMS IS FITTED (REF 31, 32)

USED ON CE PRODUCTS - (REF 37)

NON CE PRODUCTS - (REF 38)

	PART	DESCRIPTION OF ASSEMBLY	
QTY	REF	DESCRIPTION	MATERIAL
1	1	ASSY POWER SUPPLY	2071964 ***
2	2	ASSY POWER SUPPLY	2071962A01
	3		
	4		
	5		
*	6	ASSY POWER SUPPLY	ZN **** ***
	7		
	8		
	9		
	10		
	11		
	12		
	13		
1	14	SIGMA DELTA INPUT MODULE (SLOT 5)	2072043 ***
1	15	SIGMA DELTA INPUT MODULE (SLOT 6)	2072043A01
	16		
	17		
	18		
1	19	TOP ACCESS COVER	GN6007 003
1	20	BOTTOM ACCESS COVER	GN6007 002
1	21	ASSY CASE	GN0496 002
1	22	ASSY USER INTERFACE	2072035 ***
	23		
	24		
	25		
	26		
	27		
	28		
2	29	ASSEMBLY SCREEN PLATE	GN0058 001
	30		
*	31	Vx WORKS SOFTWARE	ZB9800 801
*	32	MMS-EASE LITE SOFTWARE	ZB9800 801
	33		
*	34	BLANKING PLATE (COMMS)	GN2037 001
1	35	BLANKING PLATE	GN2037 001
	36		
1 or	37	WORLDWIDE SERVICE LABEL CE M'KED	ZF8560 001-S
1	38	WORLDWIDE SERVICE LABEL NON CE	ZF8560 002-S
1	39	LABEL SHEET (MODULE)	GN9011 059
1	40	LABEL SHEET – 60TE	GN9011 058
	41		
	42		
	43		
	44		
	45		
	46		
	47		
	48		
	49		
	50		
	51		
1	52	ASSY RIBBON CABLE	GN0009 034
	53		
	54		
	55		
	56		
	57		
	58		
	59		
*	60	SELF-TAPPING PAN HEAD No4*¼"	ZB4018 110
*	61	SELF-TAPPING PAN HEAD No6*¼"	ZB4018 215
1	62	HEADER	ZB9031 985
4	63	SPACER	ZB8011 213
3	64	JUMPER	ZB9031 759
	65		
	66		
1	67	CUSTOM PUSHBUTTON INDICATOR LABEL	GN9094 003
1	68	CUSTOM LED INDICATOR LABEL	GN9025 016
1	69	BAGGED ITEMS - LABELS	GN9091 001-S
7	70	BAGGED ITEMS – TERMINAL SCREWS	ZA0005 060
2	71	BAGGED ITEMS – FIXING SCREWS	ZA0005 105
	72		

Figure 48 - P643 and P645 assembly relay (60TE


FINISH:- CLEAN
'A'
19
40
40
37 OR 38
SCRAP VIEW ON ARROW 'A'
SHOWING SERVICE LABEL
PREFERRED POSITION
CENTRALISE ON WRAPPER
22
P643
40
SCRAP VIEW
SHOWING ACCESS
COVER CLOSED
60
20
REF 60 TO BE FITTED
BEFORE REF 19 & 20
SK1
SK2
SK3
FRONT VIEW (WITH ACCESS COVERS OPEN)
REAR VIEW OF USER INTERFACE
PCB
1
SLOT POSITION No.
TO BE WRITTEN IN
SCREENED CIRCLE
(SEE ALSO NOTE 1)
SLOTS 2, 3 & 5 PCBs FIT JUMPER (REF 64) TO PL2 AS SHOWN
40
39
40
29
6
47
1
2
2
29
14
39
15
40
4
OR
8
SLOT 5
SLOT 6
FRONT VIEW (WITH USER INTERFACE REMOVED)
REF 1 & REF 2 TO
BE JOINED AS SHOWN
62
63
REF 62 SHORT PIN END
TO BE INSERTED INTO SK1
ON PCB REF 1
SLOT 5
SLOT 6
39
40
VIEW SHOWING LABELS ON INSIDE OF CASE (LOWER FACE)
40
31
Vx WORKS SOFTWARE
LICENCE LABEL TO BE
FITTED TO ETHERNET
COMMS ONLY
MAC ADDRESS /
SOFTWARE REF.
LABEL TO BE FITTED
AT FINAL TEST TO
ETHERNET COMMS
ONLY
60
40
60
26
40
21
40
REAR VIEW SHOWING OPTIONAL ETHERNET COMMS
SEE NOTE 2
ONLY REQUIRED IF
ETHERNET COMMS
IS FITTED
USED ON
CE PRODUCTS
NON CE PRODUCTS
GN0504_1
P4381ENb

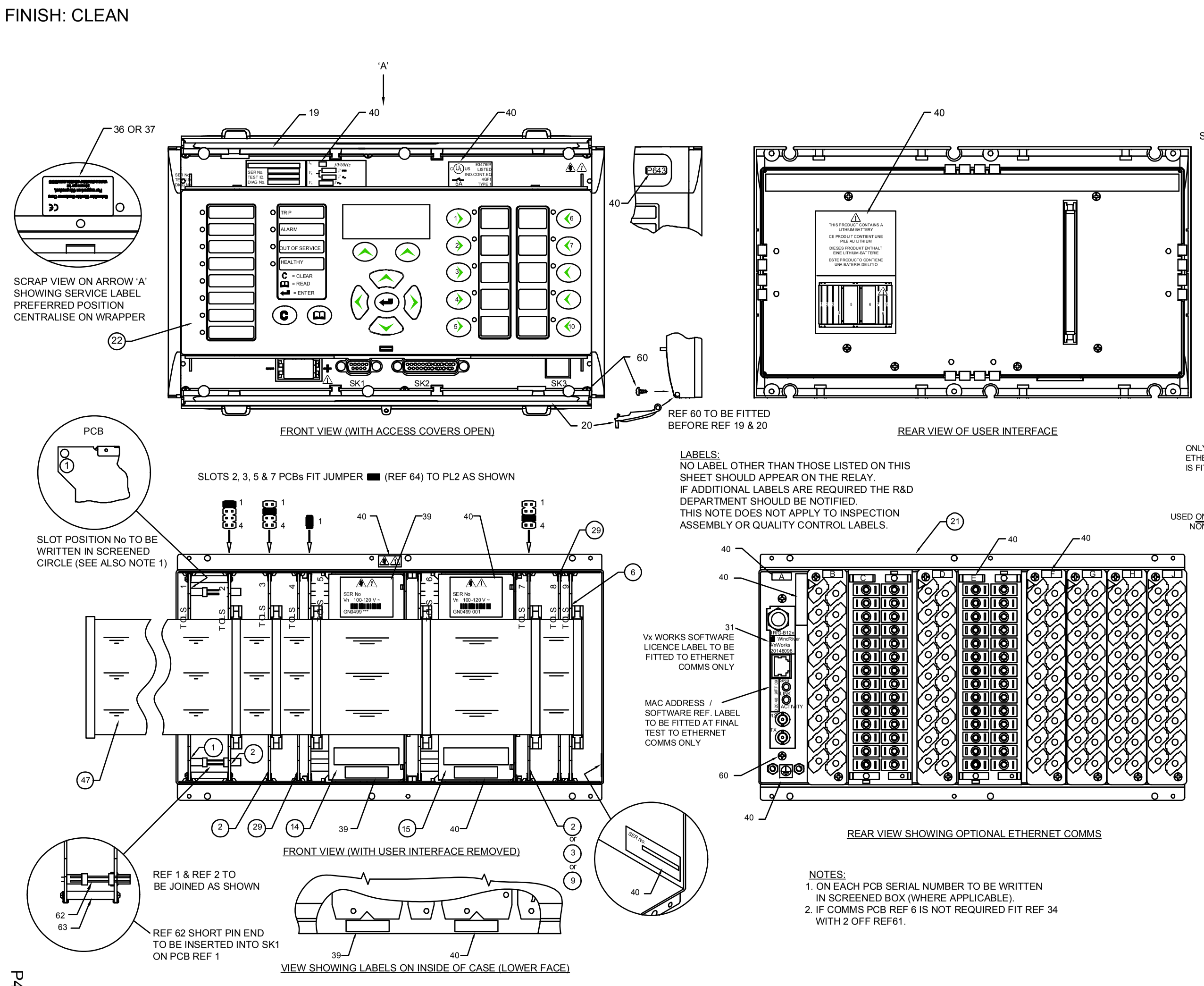
LABELS

NO LABEL OTHER THAN THOSE LISTED ON THIS SHEET SHOULD APPEAR ON THE RELAY.
IF ADDITIONAL LABELS ARE REQUIRED THE R&D DEPARTMENT SHOULD BE NOTIFIED.
THIS NOTE DOES NOT APPLY TO INSPECTION ASSEMBLY OR QUALITY CONTROL LABELS.

NOTES:
1. ON EACH PCB SERIAL NUMBER TO BE WRITTEN IN SCREENED BOX (WHERE APPLICABLE)
2. IF COMMS PCB REF 6 IS NOT REQUIRED FIT REF 34 WITH 2 OFF REF 61.

	PART	DESCRIPTION OF ASSEMBLY	
	***	P643/P645 TRANSFORMER PROTECTION	
QTY	REF	DESCRIPTION	MATERIAL
1	1	ASSY POWER SUPPLY	2071964 ***
2	2	ASSY RELAY OUTPUT	2071962A01
	3		
*	4	ASSY RTD	ZN0044 001
	5		
*	6	ASSY PCB (COMMS)	ZN **** ***
	7		
*	8	ASSY CLIO	ZN0018 001
	9		
	10		
	11		
	12		
	13		
1	14	SIGMA DELTA INPUT MODULE (SLOT 5)	2072043
1	15	SIGMA DELTA INPUT MODULE (SLOT 6)	2072043A01
	16		
	17		
	18		
1	19	TOP ACCESS COVER	GN6007 0003
1	20	BOTTOM ACCESS COVER	GN6007 002
1	21	ASSY CASE	GN0496 001
1	22	ASSY USER INTERFACE	2072035 ***
	23		
	24		
	25		
2	26	CONNECTOR	ZB9112 541
	27		
	28		
2	29	ASSEMBLY SCREEN PLATE	GN0058 001
	30		
*	31	Vx WORKS SOFTWARE	ZB9800 801
*	32	MMS-EASE LITE SOFTWARE	ZB9800 802
	33		
*	34	BLANKING PLATE (COMMS)	GN2037 001
	35		
	36		
1 or	37	WORLDWIDE SERVICE LABEL CE M'KED	ZF8560 001-S
1	38	WORLDWIDE SERVICE LABEL NON CE	ZF8560 002-S
1	39	LABEL SHEET (MODULE)	GN9011 059
1	40	LABEL SHEET – 60TE	GN9011 058
	41		
	42		
	43		
	44		
	45		
	46		
	47		
	48		
	49		
	50		
	51		
1	52	ASSY RIBBON CABLE	GN0009 034
	53		
	54		
	55		
	56		
	57		
	58		
	59		
*	60	SELF-TAPPING PAN HEAD No4x¼"	ZB4018 110
*	61	SELF-TAPPING PAN HEAD No6x¼"	ZB4018 215
1	62	HEADER	ZB9031 985
4	63	SPACER	ZB8011 213
3	64	JUMPER	ZB9031 759
	65		
	66		
1	67	CUSTOM PUSHBUTTON INDICATOR LABEL	GN9094 003
1	68	CUSTOM LED INDICATOR LABEL	GN9025 016
1	69	BAGGED ITEMS – LABELS	GN9091 001-S
7	70	BAGGED ITEMS – TERMINAL SCREWS	ZA0005 060
2	71	AGGED ITEMS – FIXING SCREWS	ZA0005 105
	72		

Figure 49 - P643 and P645 assembly relay (60TE)


FINISH: CLEAN
'A'
19
40
36 OR 37
SCRAP VIEW ON ARROW 'A' SHOWING SERVICE LABEL PREFERRED POSITION CENTRALISE ON WRAPPER
22
TRIP
ALARM
OUT OF SERVICE
HEALTHY
C = CLEAR
= READ
= ENTER
SK1
SK2
SK3
P643
60
20
FRONT VIEW (WITH ACCESS COVERS OPEN)
REF 60 TO BE FITTED BEFORE REF 19 & 20
REAR VIEW OF USER INTERFACE
THIS PRODUCT CONTAINS A LITHIUM BATTERY
PCB
SLOTS 2, 3, 5 & 7 PCBs FIT JUMPER (REF 64) TO PL2 AS SHOWN
SLOT POSITION No TO BE WRITTEN IN SCREENED CIRCLE (SEE ALSO NOTE 1)
39
29
6
47
2
14
15
2 or 3 or 9
FRONT VIEW (WITH USER INTERFACE REMOVED)
REF 1 & REF 2 TO BE JOINED AS SHOWN
62
63
REF 62 SHORT PIN END TO BE INSERTED INTO SK1 ON PCB REF 1
VIEW SHOWING LABELS ON INSIDE OF CASE (LOWER FACE)
21
31
Vx WORKS SOFTWARE LICENCE LABEL TO BE FITTED TO ETHERNET COMMS ONLY
MAC ADDRESS / SOFTWARE REF. LABEL TO BE FITTED AT FINAL TEST TO ETHERNET COMMS ONLY
A
B
C
D
E
F
G
H
J
REAR VIEW SHOWING OPTIONAL ETHERNET COMMS
SER No

LABELS:
NO LABEL OTHER THAN THOSE LISTED ON THIS SHEET SHOULD APPEAR ON THE RELAY.
IF ADDITIONAL LABELS ARE REQUIRED THE R&D DEPARTMENT SHOULD BE NOTIFIED.
THIS NOTE DOES NOT APPLY TO INSPECTION ASSEMBLY OR QUALITY CONTROL LABELS.

NOTES:
1. ON EACH PCB SERIAL NUMBER TO BE WRITTEN IN SCREENED BOX (WHERE APPLICABLE).
2. IF COMMS PCB REF 6 IS NOT REQUIRED FIT REF 34 WITH 2 OFF REF61.

	PART	DESCRIPTION OF ASSEMBLY	
		P643/P645 TRANSFORMER PROTECTION	
QTY	REF	DESCRIPTION	MATERIAL
1	1	ASSY POWER SUPPLY	2071964 ***
*	2	ASSY RELAY OUTPUT	2071962A01
*	3	ASSY OPTO INPUT	2071960A22
	4		
	5		
*	6	ASSY PCB (COMMS)	ZN **** ***
	7		
	8		
*	9	ASSY HIGH BREAK RELAY OUTPUT	ZN0042 001
	10		
	11		
	12		
	13		
1	14	SIGMA DELTA INPUT MODULE (SLOT 5)	2070043 ***
1	15	SIGMA DELTA INPUT MODULE (SLOT 6)	2072043A01
	16		
	17		
	18		
1	19	TOP ACCESS COVER	GN6007 003
1	20	BOTTOM ACCESS COVER	GN6007 002
1	21	ASSY CASE	GN0496 002
1	22	ASSY USER INTERFACE	2072035 ***
	23		
	24		
	25		
	26		
	27		
	28		
2	29	ASSEMBLY SCREEN PLATE	GN0058 001
	30		
*	31	Vx WORKS SOFTWARE	ZB9800 801
*	32	MMS-EASE LITE SOFTWARE	ZB9800 802
	33		
*	34	BLANKING PLATE (COMMS)	GN2037 001
	35		
1 or	36	WORLDWIDE SERVICE LABEL CE M'KED	ZF8560 001-S
1	37	WORLDWIDE SERVICE LABEL NON CE	ZF8560 002-S
	38		
1	39	LABEL SHEET (MODULE)	GN9011 059
1	40	LABEL SHEET – 60TE	GN9011 058
	41		
	42		
	43		
	44		
	45		
	46		
	47		
	48		
	49		
	50		
	51		
1	52	ASSY RIBBON CABLE	GN0009 034
	53		
	54		
	55		
	56		
	57		
	58		
	59		
*	60	SELF-TAPPING PAN HEAD No4x1/4"	ZB4018 110
*	61	SELF-TAPPING PAN HEAD No6x1/4"	ZB4018 215
1	62		ZB9031 985
4	63		ZB8011 213
4	64		ZB9031 759
	65		
	66		
1	67	CUSTOM PUSHBUTTON INDICATOR LABEL	GN9094 003
1	68	CUSTOM LED INDICATOR LABEL	GN9025 016
1	69	BAGGED ITEMS - LABELS	GN9091 001-S
8	70	BAGGED ITEMS - TERMINAL SCREWS	ZA0005 060
2	71	BAGGED ITEMS - FIXING SCREWS	ZA0005 105
	72		

SEE NOTE 2 — (REF 6)

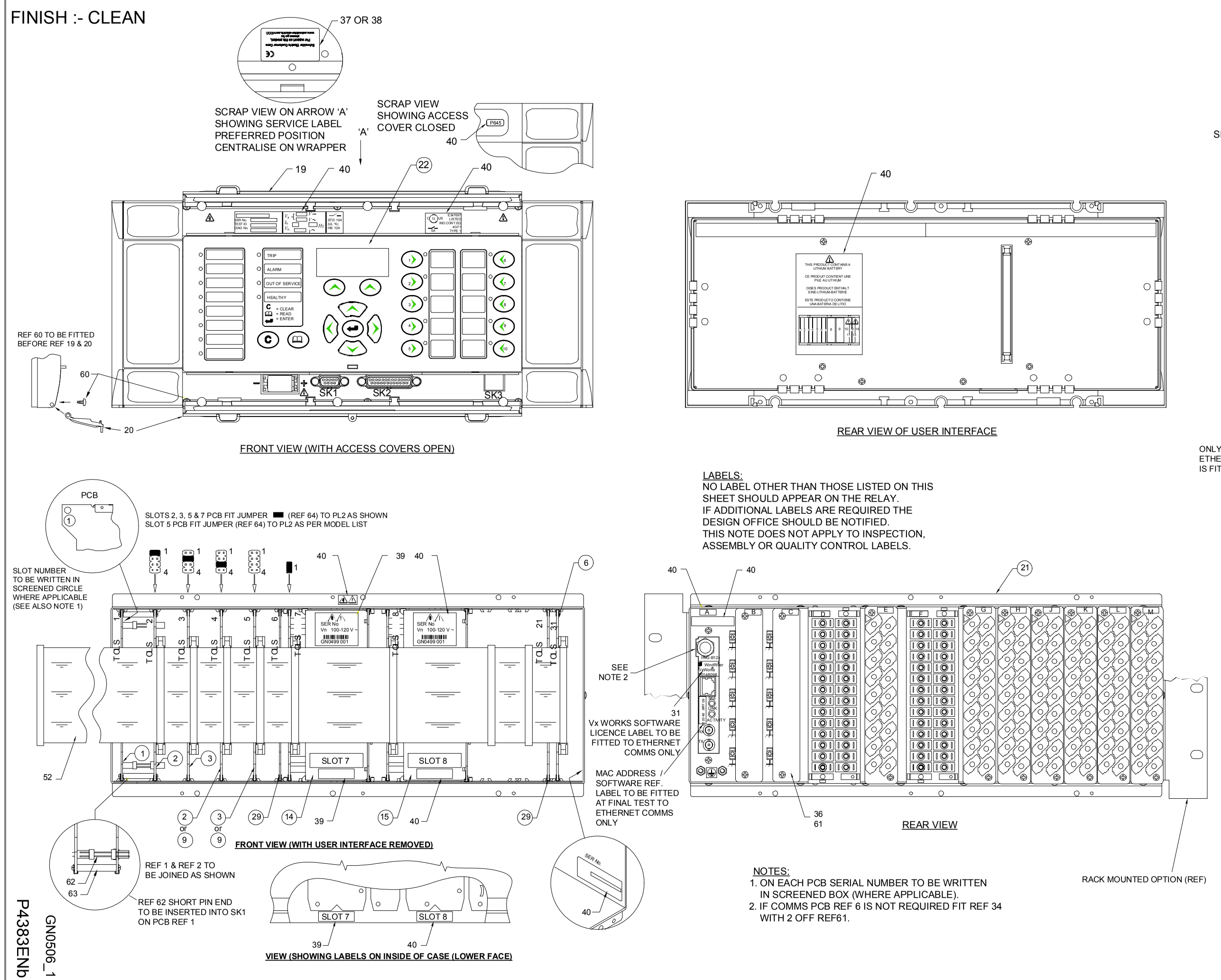
ONLY REQUIRED IF ETHERNET COMMS IS FITTED (REF 31, 32)

USED ON CE PRODUCTS - (REF 36)
NON CE PRODUCTS - (REF 37)

GN0505_1

P4382ENb

Figure 50 - P643 and P645 assembly relay (60TE)


FINISH :- CLEAN
37 OR 38
SCRAP VIEW ON ARROW 'A' SHOWING SERVICE LABEL PREFERRED POSITION CENTRALISE ON WRAPPER
SCRAP VIEW SHOWING ACCESS COVER CLOSED
'A'
P645
19
40
22
REF 60 TO BE FITTED BEFORE REF 19 & 20
60
20
TRIP
ALARM
OUT OF SERVICE
HEALTHY
= CLEAR
= READ
= ENTER
SK1
SK2
SK3
FRONT VIEW (WITH ACCESS COVERS OPEN)
REAR VIEW OF USER INTERFACE
PCB
SLOTS 2, 3, 5 & 7 PCB FIT JUMPER (REF 64) TO PL2 AS SHOWN
SLOT 5 PCB FIT JUMPER (REF 64) TO PL2 AS PER MODEL LIST
SLOT NUMBER TO BE WRITTEN IN SCREENED CIRCLE WHERE APPLICABLE (SEE ALSO NOTE 1)
39
6
SER No
Vn 100-120 V ~
GN0499 001
SLOT 7
SLOT 8
52
14
15
29
REF 1 & REF 2 TO BE JOINED AS SHOWN
62
63
REF 62 SHORT PIN END TO BE INSERTED INTO SK1 ON PCB REF 1
FRONT VIEW (WITH USER INTERFACE REMOVED)
VIEW (SHOWING LABELS ON INSIDE OF CASE (LOWER FACE)
SEE NOTE 2
31
Vx WORKS SOFTWARE LICENCE LABEL TO BE FITTED TO ETHERNET COMMS ONLY
MAC ADDRESS / SOFTWARE REF. LABEL TO BE FITTED AT FINAL TEST TO ETHERNET COMMS ONLY
21
36
61
REAR VIEW
RACK MOUNTED OPTION (REF)
GN0506_1
P4383ENb

LABELS:
NO LABEL OTHER THAN THOSE LISTED ON THIS SHEET SHOULD APPEAR ON THE RELAY.
IF ADDITIONAL LABELS ARE REQUIRED THE DESIGN OFFICE SHOULD BE NOTIFIED.
THIS NOTE DOES NOT APPLY TO INSPECTION, ASSEMBLY OR QUALITY CONTROL LABELS.

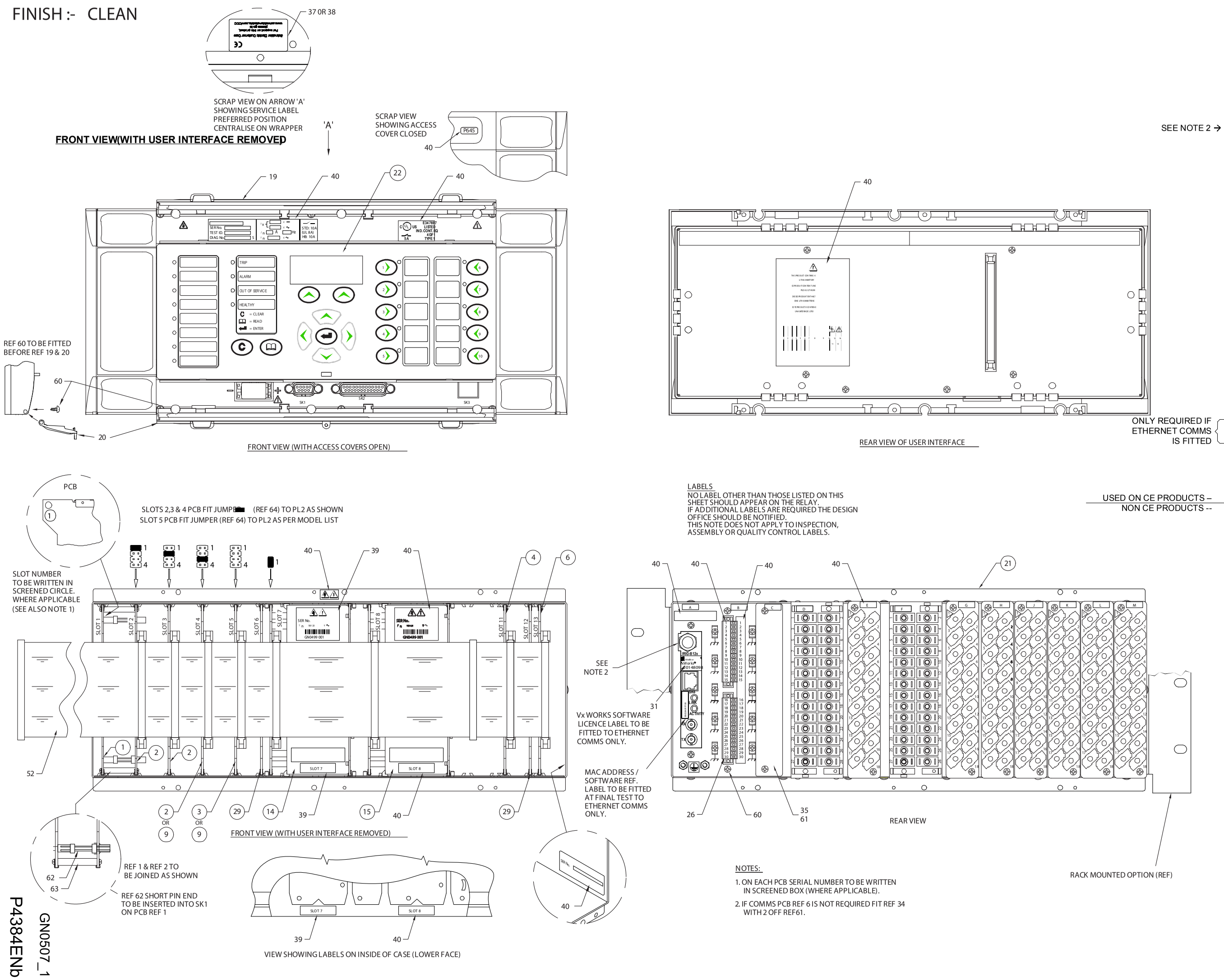
NOTES:
1. ON EACH PCB SERIAL NUMBER TO BE WRITTEN IN SCREENED BOX (WHERE APPLICABLE).
2. IF COMMS PCB REF 6 IS NOT REQUIRED FIT REF 34 WITH 2 OFF REF61.

	PART	DESCRIPTION OF ASSEMBLY	
		P645 TRANSFORMER PROTECTION	
QTY	REF	DESCRIPTION	MATERIAL
1	1	ASSY POWER SUPPLY	2071964A01
*	2	ASSY RELAY OUTPUT	2071962A01
*	3	ASSY OPTO INPUT	2071960A22
	4		
	5		
*	6	ASSY PCB (COMMS)	ZN **** ***
	7		
	8		
*	9	ASSY HIGH BREAK RELAY OUTPUT	ZN0042 001
	10		
	11		
	12		
	13		
1	14	SIGMA DELTA INPUT MODULE (SLOT 7)	2072043A01
1	15	SIGMA DELTA INPUT MODULE (SLOT 8)	2072043A01
	16		
	17		
	18		
1	19	TOP ACCESS COVER	GN6007 003
1	20	BOTTOM ACCESS COVER	GN6007 002
1	21	ASSY CASE	GN0497 ***
1	22	ASSY USER INTERFACE	2072037 ***
	23		
	24		
	25		
	26		
	27		
	28		
2	29	ASSEMBLY SCREEN PLATE	GN0058 001
	30		
*	31	Vx WORKS SOFTWARE	ZB9800 801
*	32	MMS-EASE LITE SOFTWARE	ZB9800 802
	33		
*	34	BLANKING PLATE (COMMS)	GN2037 001
	35		
1 or	36	BLANKING PLATE	GN2040 001
1	37	WORLDWIDE SERVICE LABEL CE M'KED	ZF8560 001-S
1	38	WORLDWIDE SERVICE LABEL NON CE	ZF8560 002-S
1	39	LABEL SHEET (MODULE)	GN9011 055
1	40	LABEL SHEET – 80TE	GN9011 054
	41		
	42		
	43		
	44		
	45		
	46		
	47		
	48		
	49		
	50		
	51		
1	52	ASSY RIBBON CABLE	GN0009 030
	53		
	54		
	55		
	56		
	57		
	58		
	59		
*	60	SELF-TAPPING PAN HEAD No4x1/4''	ZB4018 110
*	61	SELF-TAPPING PAN HEAD No6x1/4''	ZB4018 215
1	62	HEADER	ZB9031 985
4	63	SPACER	ZB8011 213
5	64	JUMPER	ZB9031 759
	65		
	66		
1	67	CUSTOM PUSHBUTTON INDICATOR LABEL	GN9094 003
1	68	CUSTOM LED INDICATOR LABEL	GN9025 016
1	69	BAGGED ITEMS - LABELS	GN9091 001-S
9	70	BAGGED ITEMS - TERMINAL SCREWS	ZA0005 060
2	71	BAGGED ITEMS - FIXING SCREWS	ZA0005 105
	72		

SEE NOTE 2 → (REF 6)

ONLY REQUIRED IF ETHERNET COMMS IS FITTED (REF 31, 32)

Figure 51 - P645 assembly relay (80TE)


FINISH :- CLEAN
37 OR 38
SCRAP VIEW ON ARROW 'A' SHOWING SERVICE LABEL PREFERRED POSITION CENTRALISE ON WRAPPER
'A'
SCRAP VIEW SHOWING ACCESS COVER CLOSED
P645
FRONT VIEW(WITH USER INTERFACE REMOVED
REF 60 TO BE FITTED BEFORE REF 19 & 20
FRONT VIEW (WITH ACCESS COVERS OPEN)
REAR VIEW OF USER INTERFACE
TRIP
ALARM
OUT OF SERVICE
HEALTHY
C = CLEAR
= READ
= ENTER
SK1
SK2
SK3
PCB
SLOT NUMBER TO BE WRITTEN IN SCREENED CIRCLE. WHERE APPLICABLE (SEE ALSO NOTE 1)
SLOTS 2,3 & 4 PCB FIT JUMPER (REF 64) TO PL2 AS SHOWN
SLOT 5 PCB FIT JUMPER (REF 64) TO PL2 AS PER MODEL LIST
SLOT 1
SLOT 2
SLOT 3
SLOT 4
SLOT 5
SLOT 6
SLOT 7
SLOT 8
SLOT 11
SLOT 12
SLOT 13
2 OR 9
3 OR 9
FRONT VIEW (WITH USER INTERFACE REMOVED)
REF 1 & REF 2 TO BE JOINED AS SHOWN
REF 62 SHORT PIN END TO BE INSERTED INTO SK1 ON PCB REF 1
VIEW SHOWING LABELS ON INSIDE OF CASE (LOWER FACE)
SEE NOTE 2
Vx WORKS SOFTWARE LICENCE LABEL TO BE FITTED TO ETHERNET COMMS ONLY.
MAC ADDRESS / SOFTWARE REF. LABEL TO BE FITTED AT FINAL TEST TO ETHERNET COMMS ONLY.
REAR VIEW
RACK MOUNTED OPTION (REF)
1
2
4
6
14
15
19
20
21
22
26
29
31
35
39
40
52
60
61
62
63
GN0507_1
P4384ENb

LABELS
NO LABEL OTHER THAN THOSE LISTED ON THIS SHEET SHOULD APPEAR ON THE RELAY.
IF ADDITIONAL LABELS ARE REQUIRED THE DESIGN OFFICE SHOULD BE NOTIFIED.
THIS NOTE DOES NOT APPLY TO INSPECTION, ASSEMBLY OR QUALITY CONTROL LABELS.

NOTES:
1. ON EACH PCB SERIAL NUMBER TO BE WRITTEN IN SCREENED BOX (WHERE APPLICABLE).
2. IF COMMS PCB REF 6 IS NOT REQUIRED FIT REF 34 WITH 2 OFF REF61.

SEE NOTE 2 → (REF 6)

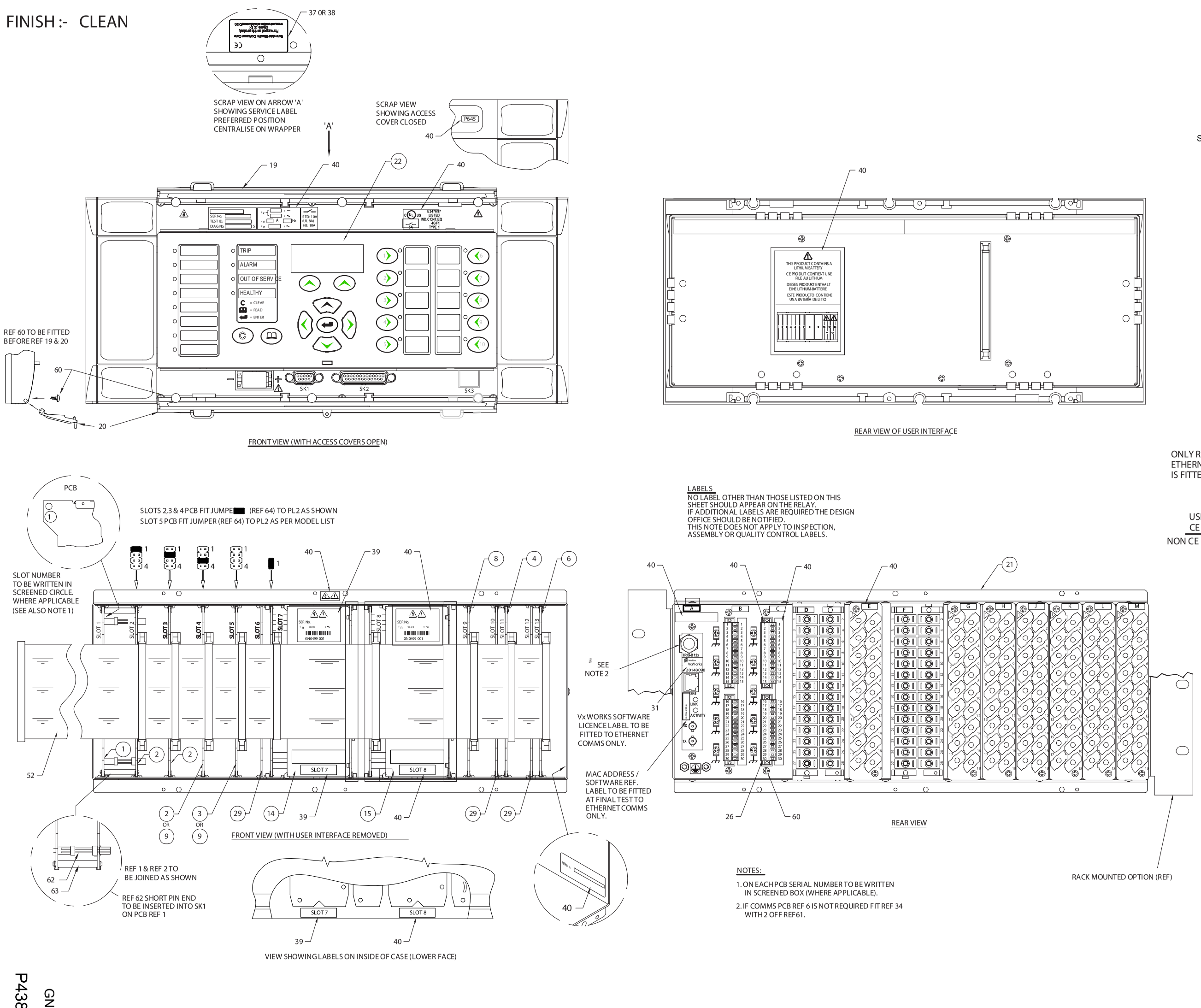
ONLY REQUIRED IF ETHERNET COMMS IS FITTED (REF 31, 32)

USED ON CE PRODUCTS – (REF 37)
NON CE PRODUCTS -- (REF 38)

	PART	DESCRIPTION OF ASSEMBLY	
	***	P645 TRANSFORMER PROTECTION	
QTY	REF	DESCRIPTION	MATERIAL
1	1	ASSY POWER SUPPLY	2071964 ***
*	2	ASSY RELAY OUTPUT	2071962A01
*	3	ASSY OPTO INPUT	2071960A22
1	4	ASSY RTD	ZN0044 001
	5		
*	6	ASSY PCB (COMMS)	ZN**** ***
	7		
	8		
*	9	ASSY HIGH BREAK RELAY OUTPUT	ZN0042 001
	10		
	11		
	12		
	13		
1	14	SIGMA DELTA INPUT MODULE (SLOT 7)	2072043A01
1	15	SIGMA DELTA INPUT MODULE (SLOT 8)	2072043A01
	16		
	17		
	18		
1	19	TOP ACCESS COVER	GN6007 003
1	20	BOTTOM ACCESS COVER	GN6007 002
1	21	ASSY CASE	GN0497 ***
1	22	ASSY USER INTERFACE	2072037 ***
	23		
	24		
	25		
2	26	CONNECTOR	ZB9112 541
	27		
	28		
2	29	ASSEMBLY SCREEN PLATE	GN0058 001
	30		
*	31	VxWORKS SOFTWARE	ZB9800 801
*	32	MMS-EASE LITE SOFTWARE	ZB9800 802
	33		
*	34	BLANKING PLATE (COMMS)	GN2037 001
	35		
1	36	BLANKING PLATE	GN2040 001
1 OR	37	WORLDWIDE SERVICE LABEL CE M'KED	ZF8560 001-S
1	38	WORLDWIDE SERVICE LABEL NON CE	ZF8560 002-S
1	39	LABEL SHEET (MODULE)	GN9011 055
1	40	LABEL SHEET – 80TE	GN9011 054
	41		
	42		
	43		
	44		
	45		
	46		
	47		
	48		
	49		
	50		
	51		
1	52	ASSY RIBBON CABLE	GN0009 030
	53		
	54		
	55		
	56		
	57		
	58		
	59		
*	60	SELF-TAPPING PAN HEAD No 4 x ¼"	ZB4018 110
*	61	SELF-TAPPING PAN HEAD No 6 x ¼"	ZB4018 215
1	62	HEADER	ZB9031 985
4	63	SPACER	ZB8011 213
5	64	JUMPER	ZB9031 759
	65		
	66		
1	67	CUSTOM PUSHBUTTON INDICATOR LABEL	GN9094 003
1	68	CUSTOM LED INDICATOR LABEL	GN9025 016
1	69	BAGGED ITEMS - LABELS	GN9091 001-S
9	70	BAGGED ITEMS – TERMINAL SCREWS	ZA0005 060
2	71	BAGGED ITEMS – FIXING SCREWS	ZA0005 105
	72		

Figure 52 - P645 assembly relay (80TE)

FINISH :- CLEAN


37 OR 38
SCRAP VIEW ON ARROW 'A' SHOWING SERVICE LABEL PREFERRED POSITION CENTRALISE ON WRAPPER
'A'
SCRAP VIEW SHOWING ACCESS COVER CLOSED
P645
19
40
22
TRIP
ALARM
OUT OF SERVICE
HEALTHY
C = CLEAR
= READ
= ENTER
SK1
SK2
SK3
REF 60 TO BE FITTED BEFORE REF 19 & 20
60
20
FRONT VIEW (WITH ACCESS COVERS OPEN)
REAR VIEW OF USER INTERFACE
PCB
SLOTS 2,3 & 4 PCB FIT JUMPER (REF 64) TO PL2 AS SHOWN
SLOT 5 PCB FIT JUMPER (REF 64) TO PL2 AS PER MODEL LIST
SLOT NUMBER TO BE WRITTEN IN SCREENED CIRCLE WHERE APPLICABLE (SEE ALSO NOTE 1)
39
8
4
6
SLOT 1
SLOT 2
SLOT 3
SLOT 4
SLOT 5
SLOT 6
SLOT 7
SLOT 8
SLOT 9
SLOT 10
SLOT 11
SLOT 12
SLOT 13
52
1
2
3
OR
9
29
14
15
FRONT VIEW (WITH USER INTERFACE REMOVED)
REF 1 & REF 2 TO BE JOINED AS SHOWN
REF 62 SHORT PIN END TO BE INSERTED INTO SK1 ON PCB REF 1
62
63
VIEW SHOWING LABELS ON INSIDE OF CASE (LOWER FACE)
SEE NOTE 2
31
Vx WORKS SOFTWARE LICENCE LABEL TO BE FITTED TO ETHERNET COMMS ONLY.
MAC ADDRESS / SOFTWARE REF. LABEL TO BE FITTED AT FINAL TEST TO ETHERNET COMMS ONLY.
A
B
C
D
E
F
G
H
J
K
L
M
21
26
60
REAR VIEW
RACK MOUNTED OPTION (REF)
SEE NOTE 2
ONLY REQUIRED IF ETHERNET COMMS IS FITTED
USED ON CE PRODUCTS --
NON CE PRODUCTS --

LABELS
NO LABEL OTHER THAN THOSE LISTED ON THIS SHEET SHOULD APPEAR ON THE RELAY.
IF ADDITIONAL LABELS ARE REQUIRED THE DESIGN OFFICE SHOULD BE NOTIFIED.
THIS NOTE DOES NOT APPLY TO INSPECTION, ASSEMBLY OR QUALITY CONTROL LABELS.

NOTES:

1. ON EACH PCB SERIAL NUMBER TO BE WRITTEN IN SCREENED BOX (WHERE APPLICABLE).
2. IF COMMS PCB REF 6 IS NOT REQUIRED FIT REF 34 WITH 2 OFF REF61.

	PART	DESCRIPTION OF ASSEMBLY	
☒	***	P645 TRANSFORMER PROTECTION	
QTY	REF	DESCRIPTION	MATERIAL
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*	2	ASSY RELAY OUTPUT	2071962A01
*	3	ASSY OPTO INPUT	2071960A22
1	4	ASSY RTD	ZN0044 001
	5		
*	6	ASSY PCB (COMMS)	ZN **** ***
	7		
1	8	ASSY CLIO	ZN0018 001
*	9	ASSY HIGH BREAK RELAY OUTPUT	ZN0042 001
	10		
	11		
	12		
	13		
1	14	SIGMA DELTA INPUT MODULE (SLOT 7)	2072043A01
1	15	SIGMA DELTA INPUT MODULE (SLOT 8)	2072043A01
	16		
	17		
	18		
1	19	TOP ACCESS COVER	GN6007 003
1	20	BOTTOM ACCESS COVER	GN6007 002
1	21	ASSY CASE	GN0497 ***
1	22	ASSY USER INTERFACE	2072037 ***
	23		
	24		
	25		
4	26	CONNECTOR	ZB9112 541
	27		
	27		
3	29	ASSEMBLY SCREEN PLATE	GN0058 001
	30		
*	31	Vx WORKS SOFTWARE	ZB9800 801
*	32	MMS-EASE LITE SOFTWARE	ZB9800 802
	33		
*	34	BLANKING PLATE (COMMS)	GN2037 001
	35		
	36		
1 OR	37	WORLDWIDE SERVICE LABEL CE M'KED	ZF8560 001-S
1	38	WORLDWIDE SERVICE LABEL NON CE	ZF8560 002-S
1	39	LABEL SHEET (MODULE)	GN9011 055
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	44		
	45		
	46		
	47		
	48		
	49		
	50		
	51		
1	52	ASSY RIBBON CABLE	GN0009 030
	53		
	54		
	55		
	56		
	57		
	58		
	59		
*	60	SELF-TAPPING PAN HEAD No4x1/4"	ZB4018 110
*	61	SELF-TAPPING PAN HEAD No6x1/4"	ZB4018 215
1	62	HEADER	ZB9031 985
4	63	SPACER	ZB8011 213
5	64	JUMPER	ZB9031 759
	65		
	66		
1	67	CUSTOM PUSHBUTTON INDICATOR LABEL	GN9094 003
1	68	CUSTOM LED INDICATOR LABEL	GN9025 016
1	69	BAGGED ITEMS - LABELS	GN9091 001-S
9	70	BAGGED ITEMS - TERMINAL SCREWS	ZA0005 060
2	71	BAGGED ITEMS - FIXING SCREWS	ZA0005 105
	72		
	73		

GN0509_1
P4386ENb

Figure 53 - P645 assembly relay (80TE)

CYBER SECURITY

CHAPTER 16

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1 OVERVIEW

In the past, substation networks were traditionally isolated and the protocols and data formats used to transfer information between devices were more often than not proprietary.

For these reasons, the substation environment was very secure against cyber attacks. The terms used for this inherent type of security are:

- Security by isolation (if the substation network is not connected to the outside world, it can’t be accessed from the outside world).
- Security by obscurity (if the formats and protocols are proprietary, it is very difficult, to interpret them.

The increasing sophistication of protection schemes coupled with the advancement of technology and the desire for vendor interoperability has resulted in standardization of networks and data interchange within substations. Today, devices within substations use standardized protocols for communication. Furthermore, substations can be interconnected with open networks, such as the internet or corporate-wide networks, which use standardized protocols for communication. This introduces a major security risk making the grid vulnerable to cyber-attacks, which could in turn lead to major electrical outages.

Clearly, there is now a need to secure communication and equipment within substation environments. This chapter describes the security measures that have been put in place for Schneider Electric's range of Intelligent Electronic Devices (IEDs).

2 THE NEED FOR CYBER SECURITY

Cyber-security provides protection against unauthorized disclosure, transfer, modification, or destruction of information and/or information systems, whether accidental or intentional. To achieve this, there are several security requirements:

- Confidentiality (preventing unauthorized access to information)
- Integrity (preventing unauthorized modification)
- Availability / Authentication (preventing the denial of service and assuring authorized access to information)
- Non-Repudiation (preventing the denial of an action that took place)
- Traceability/Detection (monitoring and logging of activity to detect intrusion and analyze incidents)

The threats to cyber security may be unintentional (e.g. natural disasters, human error), or intentional (e.g. cyber attacks by hackers).

Good cyber security can be achieved with a range of measures, such as closing down vulnerability loopholes, implementing adequate security processes and procedures and providing technology to help achieve this.

Examples of vulnerabilities are:

- Indiscretions by personnel (e.g. users keep passwords on their computer)
- Bypassing of controls (e.g. users turn off security measures)
- Bad practice (users do not change default passwords, or everyone uses the same password to access all substation equipment)
- Inadequate technology (e.g. substation is not firewalled)

Examples of availability issues are:

- Equipment overload, resulting in reduced or no performance
- Expiry of a certificate prevents access to equipment.

To help tackle these issues, standards organizations have produced various standards, by which compliance significantly reduces the threats associated with lack of cyber security.

3 STANDARDS

There are several standards, which apply to substation cyber security (see Table 1).

	Country	
NERC CIP (North American Electric Reliability Corporation)	USA	Framework for the protection of the grid critical Cyber Assets
BDEW (German Association of Energy and Water Industries)	Germany	Requirements for Secure Control and Telecommunication Systems
ANSI ISA 99	USA	ICS oriented then Relevant for EPU completing existing standard and identifying new topics such as patch management
IEEE 1686	International	International Standard for substation IED cyber security capabilities
IEC 62351	International	Power system data and Comm. protocol
ISO/IEC 27002	International	Framework for the protection of the grid critical Cyber Assets
NIST SP800-53 (National Institute of Standards and Technology)	USA	Complete framework for SCADA SP800-82and ICS cyber security
CPNI Guidelines (Centre for the Protection of National Infrastructure)	UK	Clear and valuable good practices for Process Control and SCADA security

Table 1 - Standards applicable to cyber security

The standards currently applicable to Schneider Electric IEDs is NERC and IEEE1686.

3.1 NERC Compliance

The North American Electric Reliability Corporation (NERC) created a set of standards for the protection of critical infrastructure. These are known as the CIP standards (Critical Infrastructure Protection). These were introduced to ensure the protection of Critical Cyber Assets, which control or have an influence on the reliability of North America’s bulk electric systems.

These standards have been compulsory in the USA for several years now. Compliance auditing started in June 2007, and utilities face extremely heavy fines for non-compliance.

The group of CIP standards is listed in Table 2.

CIP standard	Description
CIP-002-1 Critical Cyber Assets	Define and document the Critical Assets and the Critical Cyber Assets
CIP-003-1 Security Management Controls	Define and document the Security Management Controls required to protect the Critical Cyber Assets
CIP-004-1 Personnel and Training	Define and Document Personnel handling and training required protecting Critical Cyber Assets
CIP-005-1 Electronic Security	Define and document logical security perimeter where Critical Cyber Assets reside and measures to control access points and monitor electronic access
CIP-006-1 Physical Security	Define and document Physical Security Perimeters within which Critical Cyber Assets reside
CIP-007-1 Systems Security Management	Define and document system test procedures, account and password management, security patch management, system vulnerability, system logging, change control and configuration required for all Critical Cyber Assets

CIP standard	Description
CIP-008-1 Incident Reporting and Response Planning	Define and document procedures necessary when Cyber Security Incidents relating to Critical Cyber Assets are identified
CIP-009-1 Recovery Plans	Define and document Recovery plans for Critical Cyber Assets

Table 2 - NERC CIP standards

The following sections provide further details about each of these standards, describing the associated responsibilities of the utility company and where the IED manufacturer can help the utilities with the necessary compliance to these standards.

3.1.1 CIP 002

CIP 002 concerns itself with the identification of:

- Critical assets, such as overhead lines and transformers
- Critical cyber assets, such as IEDs that use routable protocols to communicate outside or inside the Electronic Security Perimeter; or are accessible by dial-up.

Power utility responsibilities:	Schneider Electric's contribution:
Create the list of the assets	We can help the power utilities to create this asset register automatically. We can provide audits to list the Cyber assets

3.1.2 CIP 003

CIP 003 requires the implementation of a cyber security policy, with associated documentation, which demonstrates the management’s commitment and ability to secure its Critical Cyber Assets.

The standard also requires change control practices whereby all entity or vendor-related changes to hardware and software components are documented and maintained

Power utility responsibilities:	Schneider Electric's contribution:
To create a Cyber Security Policy	We can help the power utilities to have access control to its critical assets by providing centralized Access control. We can help the customer with its change control by providing a section in the documentation where it describes changes affecting the hardware and software.

3.1.3 CIP 004

CIP 004 requires that personnel having authorized cyber access or authorized physical access to Critical Cyber Assets, (including contractors and service vendors), have an appropriate level of training.

Power utility responsibilities:	Schneider Electric's contribution:
To provide appropriate training of its personnel	We can provide cyber security training

3.1.4 CIP 005

CIP 005 requires the establishment of an Electronic Security Perimeter (ESP), which provides:

- The disabling of ports and services that are not required

- Permanent monitoring and access to logs (24x7x365)
- Vulnerability Assessments (yearly at a minimum)
- Documentation of Network Changes

Power utility responsibilities:	Schneider Electric's contribution:
To monitor access to the ESP To perform the vulnerability assessments To document network changes	To disable all ports not used in the IED To monitor and record all access to the IEDthe access at all access points of the ESP

3.1.5 CIP 006

CIP 006 states that Physical Security controls, providing perimeter monitoring and logging along with robust access controls, must be implemented and documented. All cyber assets used for Physical Security are considered critical and should be treated as such:

Power utility responsibilities:	Schneider Electric's contribution:
Provide physical security controls and perimeter monitoring. Ensure that people who have access to critical cyber assets don’t have criminal records Schneider Electric's contribution.	Schneider Electric cannot provide additional help with this aspect.

3.1.6 CIP 007

CIP 007 covers the following points:

- Test procedures
- Ports and services
- Security patch management
- Antivirus
- Account management
- Monitoring
- An annual vulnerability assessment should be performed

Power utility responsibilities:	Schneider Electric's contribution:
To provide an incident response team and have appropriate processes in place	Test procedures; We can provide advice and help on testing. Ports and services; Our devices can disable unused ports and services Security patch management; We can provide assistance Antivirus; We can provide advise and assistance Account management; We can provide advice and assistance Monitoring; Our equipment monitors and logs access

3.1.7 CIP 008

CIP 008 requires that an incident response plan be developed, including the definition of an incident response team, their responsibilities and associated procedures.

Power utility responsibilities:	Schneider Electric's contribution:
To provide an incident response team and have appropriate processes in place.	Schneider Electric cannot provide additional help with this aspect.

3.1.8 CIP 009

CIP 009 states that a disaster recovery plan should be created and tested with annual drills.

Power utility responsibilities:	Schneider Electric's contribution:
To implement a recovery plan	To provide guidelines on recovery plans and backup/restore documentation

3.2 IEEE 1686-2007

IEEE 1686-2007 is an IEEE Standard for substation IEDs cyber security capabilities. It proposes practical and achievable mechanisms to achieve secure operations.

The following features described in this standard apply to Schneider Electric Px40 relays:

- Passwords are 8 characters long and can contain upper-case, lower-case, numeric and special characters.
- Passwords are never displayed or transmitted to a user.
- IED functions and features are assigned to different password levels. The assignment is fixed.
- Record of an audit trail listing events in the order in which they occur, held in a circular buffer.
- Records contain all defined fields from the standard and record all defined function event types where the function is supported.
- No password defeat mechanism exists. Instead a secure recovery password scheme is implemented.
- Unused ports (physical and logical) may be disabled.

4 PX40 CYBER SECURITY IMPLEMENTATION

The Schneider Electric IEDs have always been and will continue to be equipped with state-of-the-art security measures. Due to the ever-evolving communication technology and new threats to security, this requirement is not static. Hardware and software security measures are continuously being developed and implemented to mitigate the associated threats and risks.

This section describes the current implementation of cyber security, valid for the release of platform software to which this manual pertains. This current cyber security implementation is known as Cyber Security Phase 1.

At the IED level, these cyber security measures have been implemented:

- Four-level Access
- Password strengthening
- Disabling of unused application and physical ports
- Inactivity timer
- Storage of security events (logs) in the IED
- NERC-compliant default display

External to the IEDs, the following cyber security measures have been implemented:

- Antivirus
- Security patch management

4.1 Four-level Access

The menu structure contains four levels of access three of which are password protected. These are summarized in Table 3.

Level	Meaning	Read Operation	Write Operation
0	Read Some Write Minimal	SYSTEM DATA column: Description Plant Reference Model Number Serial Number S/W Ref. Access Level Security Feature SECURITY CONFIG column: User Banner Attempts Remain Blk Time Remain Fallback PW level Security Code (UI only)	Password Entry LCD Contrast (UI only)
1	Read All Write Few	All data and settings are readable. Poll Measurements	All items writeable at level 0. Level 1 Password setting Select Event, Main and Fault (upload) Extract Events (e.g. via MiCOM S1 Studio)

Level	Meaning	Read Operation	Write Operation
2	Read All Write Some	All data and settings are readable. Poll Measurements	All items writeable at level 1. Setting Cells that change visibility (Visible/Invisible). Setting Values (Primary/Secondary) selector Commands: Reset Indication Reset Demand Reset Statistics Reset CB Data / counters Level 2 Password setting
3	Read All Write All	All data and settings are readable. Poll Measurements	All items writeable at level 2. Change all Setting cells Operations: Extract and download Setting file. Extract and download PSL Extract and download MCL61850 (IED Config - IEC61850) Extraction of Disturbance Recorder Courier/Modbus Accept Event (auto event extraction, e.g. via A2R) Commands: Change Active Group setting Close / Open CB Change Comms device address. Set Date & Time Switch MCL banks / Switch Conf. Bank in UI (IED Config - IEC61850) Enable / Disable Device ports (in SECURITY CONFIG column) Level 3 password setting

Table 3 - Password levels

4.1.1 Default Passwords

Default passwords are blank for Level 1 and AAAA for Levels 2 and 3.

4.1.2 Password Rules

- Passwords may be any length between 0 and 8 characters long
- Passwords may or may not be NERC compliant
- Passwords may contain any ASCII character in the range ASCII code 33 (21 Hex) to ASCII code 122 (7A Hex) inclusive
- Only one password is required for all the IED interfaces

4.1.3 Access Level DDBs

In additional to having the 'Access level' cell in the 'System data' column (address 00D0), the current level of access for each interface is also available for use in the Programming Scheme Logic (PSL) by mapping to these Digital Data Bus (DDB) signals:

- HMI Access Lvl 1
- HMI Access Lvl 2
- FPort AccessLvl1
- FPort AccessLvl2
- RPrt1 AccessLvl1
- RPrt1 AccessLvl2
- RPrt2 AccessLvl1
- RPrt2 AccessLvl2

  Where:

  HMI is the Human Machine Interface.

Each pair of DDB signals indicates the access level as follows:

- Lvl 1 off, Lvl 2 off = 0
- Lvl 1 on, Lvl 2 off = 1
- Lvl 1 off, Lvl 2 on = 2
- Lvl 1 on, Lvl 2 on = 3

4.2 Password Strengthening

NERC compliant passwords result in a minimum level of complexity, and include these requirements:

- At least one upper-case alpha character
- At least one lower-case alpha character
- At least one numeric character
- At least one special character (%,$...)
- At least six characters long

4.3 Password validation

The IED checks for NERC compliance. If the password is entered through the front panel then this is reflected on the panel Liquid Crystal Display (LCD) display.

If the entered password is NERC compliant, the following text is displayed

```
NERC COMPLIANT
P/WORD WAS SAVED
```

The IED does not enforce NERC compliance. It is the responsibility of the user to ensure that compliance is adhered to as and when necessary. In the case that the password entered is not NERC-compliant, the user is required to actively confirm this, in which case the non-compliance is logged.

If the entered password is not NERC compliant, the following text is displayed:

```
NERC COMPLIANCE
NOT MET CONFIRM?
```

On confirmation, the non-compliant password is stored and the following acknowledgement message is displayed for 2 seconds.

```
NON-NERC P/WORD
SAVED OK
```

If the action is cancelled, the password is rejected and the following message displayed for 2 seconds.

```
NON-NERC P/WORD
NOT SAVE
```

If the password is entered through a communications port using Courier or Modbus protocols the IED will store the password, irrespective of whether it is or isn't NERC-compliant, and then uses appropriate response codes to inform the client that the password was NERC-compliant or not. The client then can choose if he/she wishes to enter a new password that is NERC-compliant or leave the entered one in place.

4.3.1 Blank Passwords

A blank password is effectively a zero-length password. Through the front panel it is entered by confirming the password entry without actually entering any password characters. Through a communications port the Courier and Modbus protocols each have a means of writing a blank password to the IED. A blank password disables the need for a password at the level that this password applied.

Blank passwords have a slightly different validation procedure. If a blank password is entered through the front panel, the following text is displayed, after which the procedure is the same as already described:

```
BLANK PASSWORD
ENTERED CONFIRM
```

Blank Passwords cannot be configured if lower level password is not blank.

Blank Passwords affect fall back level after inactivity timeout or logout.

The 'fallback level' is the password level adopted by the IED after an inactivity timeout, or after the user logs out. This will be either the level of the highest level password that is blank, or level 0 if no passwords are blank.

4.4 Password Management

The user is locked out temporarily, after a defined number of failed password entry attempts. The number of password entry attempts, and the blocking periods are configurable. These settings are shown in Table 4.

The first invalid password entry sets the attempts count (actual text here) to 1 and initiates an 'attempts timer'. Further invalid passwords during the timed period increments the attempts count. When the maximum number of attempts has been reached, access is blocked. If the attempts timer expires, or the correct password is entered *before* the 'attempt count' reaches the maximum number, then the 'attempts count' is reset to 0.

Once the password entry is blocked, a 'blocking timer' is initiated. Attempts to access the interface whilst the 'blocking timer' is running results in an error message, irrespective of whether the correct password is entered or not. Only after the 'blocking timer' has expired will access to the interface be unblocked, whereupon the attempts counter is reset to zero.

Attempts to write to the password entry whilst it is blocked results in the following message, which is displayed for 2 seconds.

```
NOT ACCEPTED
ENTRY IS BLOCKED
```

Appropriate responses achieve the same result if the password is written through a communications port.

The attempts count, attempts timer and blocking timer can be configured, as shown in Table 4.

Setting	Cell col row	Units	Default Setting	Available Setting
Attempts Limit	25 02		3	0 to 3 step 1
Attempts Timer	25 03	Minutes	2	1 to 3 step 1
Blocking Timer	25 04	Minutes	5	1 to 30 step 1

Table 4 - Password blocking configuration

4.5 Password Recovery

Password recovery is the means by which the passwords can be recovered on a device if the customer should mislay the configured passwords. To obtain the recovery password the customer must contact the Schneider Electric Contact Center and supply two pieces of information from the IED – namely the *Serial Number* and its *Security Code*. The Contact Centre will use these items to generate a Recovery Password which is then provided to the customer.

The security code is a 16-character string of upper case characters. It is a read-only parameter. The IED generates its own security code randomly. A new code is generated under the following conditions:

- On power up
- Whenever settings are set back to default
- On expiry of validity timer (see below)
- When the recovery password is entered

As soon as the security code is displayed on the LCD display, a validity timer is started. This validity timer is set to 72 hours and is not configurable. This provides enough time for the contact centre to manually generate and send a recovery password. The Service Level Agreement (SLA) for recovery password generation is one working day, so 72 hours is sufficient time, even allowing for closure of the contact centre over weekends and bank holidays.

To prevent accidental reading of the IED security code the cell will initially display a warning message:

```
PRESS ENTER TO
READ SEC. CODE
```

The security code will be displayed on confirmation, whereupon the validity timer will be started. Note that the security code can only be read from the front panel.

4.5.1 Entry of the Recovery Password

The recovery password is intended for recovery only. It is not a replacement password that can be used continually. It can only be used once – for password recovery.

Entry of the recovery password causes the IED to reset all passwords back to default. This is all it is designed to do. After the passwords have been set back to default, it is up to the user to enter new passwords appropriate for the function for which they are intended, ensuring NERC compliance, if required.

On this action, the following message is displayed:

```
PASSWORDS HAVE
BEEN SET TO DEFAULT
```

The recovery password can be applied through any interface, local or remote. It will achieve the same result irrespective of which interface it is applied through.

4.5.2 Password Encryption

The IED supports encryption for passwords entered remotely. The encryption key can be read from the IED through a specific cell available only through communication interfaces, not the front panel. Each time the key is read the IED generates a new key that is valid only for the next password encryption write. Once used, the key is invalidated and a new key must be read for the next encrypted password write. The encryption mechanism is otherwise transparent to the user.

4.6 Port Disablement

4.6.1 Disabling Physical Ports

It is possible to disable unused physical ports. A level 3 password is needed to perform this action.

To prevent accidental disabling of a port, a warning message is displayed according to whichever port is required to be disabled. For example if rear port 1 is to be disabled, the following message appears:

```
REAR PORT 1 TO BE
DISABLED.CONFIRM
```

There are between two and four ports eligible for disablement:

- Front port
- Rear port 1
- Rear port 2 (not implemented on all models)
- Ethernet port (not implemented on all models)

Note *It is not possible to disable a port from which the disabling port command originates.*

4.6.2 Disabling Logical Ports

It is possible to disable unused logical ports. A level 3 password is needed to perform this action.

Note *The port disabling setting cells are not provided in the settings file*

Caution **Disabling the Ethernet port will disable all Ethernet based communications.**

If it is not desirable to disable the Ethernet port, it is possible to disable selected protocols on the Ethernet card and leave others functioning.

Three protocols can be disabled:

- IEC61850

- DNP3 Over Ethernet
- Courier Tunnelling

Note	*If any of these protocols are enabled or disabled, the Ethernet card will reboot.*

4.7 Logging out

If you have been configuring the IED, you should 'log out'. You do this by going up to the top of the menu tree. When you are at the Column Heading level and you press the Up button, you may be prompted to log out with the following display:

```
DO YOU WANT TO
LOG OUT?
```

You will only be asked this question if your password level is higher than the fallback level.

If you confirm, the following message is displayed for 2 seconds:

```
LOGGED OUT
Access Level <x>
```

Where x is the current fallback level.

If you decide not to log out (i.e. you cancel), the following message is displayed for 2 seconds.

```
LOGOUT CANCELLED
Access Level <x>
```

Where x is the current access level.

4.8 Events

The implementation of NERC-compliant cyber security necessitates the generation of a range of Event records, which log security issues such as the entry of a non-NERC-compliant password, or the selection of a non-NERC-compliant default display. Table 6 lists all Security events.

Event Value	Display
PASSWORD LEVEL UNLOCKED	USER LOGGED IN ON <int> LEVEL <n>
PASSWORD LEVEL RESET	USER LOGGED OUT ON <int> LEVEL <n>
PASSWORD SET BLANK	P/WORD SET BLANK BY <int> LEVEL <p>
PASSWORD SET NON-COMPLIANT	P/WORD NOT-NERC BY <int> LEVEL <p>
PASSWORD MODIFIED	PASSWORD CHANGED BY <int> LEVEL <p>
PASSWORD ENTRY BLOCKED	PASSWORD BLOCKED ON <int>
PASSWORD ENTRY UNBLOCKED	P/WORD UNBLOCKED ON <int>
INVALID PASSWORD ENTERED	INV P/W ENTERED ON <int>

Event Value	Display
PASSWORD EXPIRED	P/WORD EXPIRED ON <int>
PASSWORD ENTERED WHILE BLOCKED	P/W ENT WHEN BLK ON <int>
RECOVERY PASSWORD ENTERED	RCVY P/W ENTERED ON <int>
IED SECURITY CODE READ	IED SEC CODE RD ON <int>
IED SECURITY CODE TIMER EXPIRED	IED SEC CODE EXP -
PORT DISABLED	PORT DISABLED BY <int> PORT <prt>
PORT ENABLED	PORT ENABLED BY <int> PORT <prt>
DEF. DISPLAY NOT NERC COMPLIANT	DEF DSP NOT-NERC
PSL SETTINGS DOWNLOADED	PSL STNG D/LOAD BY <int> GROUP <grp>
DNP SETTINGS DOWNLOADED	DNP STNG D/LOAD BY <int>
TRACE DATA DOWNLOADED	TRACE DAT D/LOAD BY <int>
IEC61850 CONFIG DOWNLOADED	IED CONFG D/LOAD BY <int>
USER CURVES DOWNLOADED	USER CRV D/LOAD BY <int> GROUP <crv>
PSL CONFIG DOWNLOADED	PSL CONFG D/LOAD BY <int> GROUP <grp>
SETTINGS DOWNLOADED	SETTINGS D/LOAD BY <int> GROUP <grp>
PSL SETTINGS UPLOADED	PSL STNG UPLOAD BY <int> GROUP <grp>
DNP SETTINGS UPLOADED	DNP STNG UPLOAD BY <int>
TRACE DATA UPLOADED	TRACE DAT UPLOAD BY <int>
IEC61850 CONFIG UPLOADED	IED CONFG UPLOAD BY <int>
USER CURVES UPLOADED	USER CRV UPLOAD BY <int> GROUP <crv>
PSL CONFIG UPLOADED	PSL CONFG UPLOAD BY <int> GROUP <grp>
SETTINGS UPLOADED	SETTINGS UPLOAD BY <int> GROUP <grp>
EVENTS HAVE BEEN EXTRACTED	EVENTS EXTRACTED BY <int> <nov> EVNTS
ACTIVE GROUP CHANGED	ACTIVE GRP CHNGE BY <int> GROUP <grp>
CS SETTINGS CHANGED	C & S CHANGED BY <int>
DR SETTINGS CHANGED	DR CHANGED BY <int>

Event Value	Display
SETTING GROUP CHANGED	SETTINGS CHANGED BY <int> GROUP <grp>
POWER ON	POWER ON -
SOFTWARE_DOWNLOADED	S/W DOWNLOADED -

Table 5 - Security event values

Where:

int is the interface definition (UI, FP, RP1, RP2, TNL, TCP)
prt is the port ID (FP, RP1, RP2, TNL, DNP3, IEC, ETHR)
grp is the group number (1, 2, 3, 4)
crv is the Curve group number (1, 2, 3, 4)
n is the new access level (0, 1, 2, 3)
p is the password level (1, 2, 3)
nov is the number of events (1 – nnn)

Each event is identified with a unique number that is incremented for each new event so that it is possible to detect missing events as there will be a ‘gap’ in the sequence of unique identifiers. The unique identifier forms part of the event record that is read or uploaded from the IED.

Note	*It is no longer possible to clear Event, Fault, Maintenance, and Disturbance Records*

4.9 Cyber Security Settings

Cyber Security is important enough to warrant its own IED column called SECURITY CONFIGURATION, located at column number 25. In addition to this new group, settings are affected in the SYSTEM DATA, COMMS SYS DATA and VIEW RECORDS columns.

A summary of the relevant columns is shown in Table 6. A complete listing of the settings criteria is described in the Settings and Records chapter.

Parameter	Cell col row	Default Setting	Available Setting	Interface Applicability	In Setting file?
Password	00 02		ASCII 33 to 122	All	Yes, ~~~~~~~~
Access Level	00 D0		0 = Read Some, 1 = Read All, 2 = Read All + Write Some, 3 = Read All + Write All	All	Yes, Not Settable
Password Level 1	00 D2		ASCII 33 to 122	All	Yes
Password Level 2	00 D3		ASCII 33 to 122	All	Yes
Password Level 3	00 D4		ASCII 33 to 122	All	Yes
Security Feature	00 DF		1	All	Yes, Not Settable
SECURITY CONFIG	25 00			All	Yes
Use Banner	25 01	ACCESS ONLY FOR AUTHORISED USERS	ASCII 32 to 163	All	Yes
Attempts Limit	25 02	3	0 to 3 step 1	All	Yes
Attempts Timer	25 03	2	1 to 3 step 1	All	Yes
Blocking Timer	25 04	5	1 to 30 step 1	All	Yes

Parameter	Cell col row	Default Setting	Available Setting	Interface Applicability	In Setting file?
Front Port	25 05	Enabled	0 = Disabled or 1 = Enabled	All	No
Rear Port 1	25 06	Enabled	0 = Disabled or 1 = Enabled	All	No
Rear Port 2	25 07	Enabled	0 = Disabled or 1 = Enabled	All	No
Ethernet Port*	25 08	Enabled	0 = Disabled or 1 = Enabled	All	No
Courier Tunnel*†	25 09	Enabled	0 = Disabled or 1 = Enabled	All	No
IEC61850*†	25 0A	Enabled	0 = Disabled or 1 = Enabled	All	No
DNP3 OE*†	25 0B	Enabled	0 = Disabled or 1 = Enabled	All	No
Attempts Remain	25 11			All	Yes, Not Settable
Blk Time Remain	25 12			All	Yes, Not Settable
Fallbck PW Level	25 20	0	0 = Password Level 0, 1 = Password Level 1, 2 = Password Level 2, 3 = Password Level 3	All	Yes, Not Settable
Security Code	25 FF			UI Only	No
Evt Unique Id (Normal Extraction)	01 FE			All	No
Evt Iface Source ± (Bits 0 – 7 of Event State)	01 FA			All	No
Evt Access Level ± (Bits 15 – 8 of Event State)	01 FB			All	No
Evt Extra Info 1 ± (Bits 23 – 16 of Event State)	01 FC			All	No
Evt Extra Info 2 ±Ω (Bits 31 – 24 of Event State)	01 FD			All	No

Table 6 - Security cells summary

Where:
* - These cells will not be present in a non-Ethernet product
†- These cells will be invisible if the Ethernet port is disabled.
± - These cells invisible if event is not a Security event
Ω – This cell is invisible in current phase as it does not contain any data. Reserved for future use.

DUAL REDUNDANT ETHERNET BOARD (UPGRADE)

CHAPTER 17

Date:	12/2013
Software Version & Hardware Suffix:	Data Pack G, I, J, H
Connection Diagrams:	10Px4001

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1 INTRODUCTION

The redundant Ethernet board assures redundancy at IED level. It is fitted into the following IEDs.

- P141, P142, P143, P144, P145
- P241, P242, P243
- P341, P342, P343, P344, P345
- P442, P443, P444, P445, P446
- P543, P544, P545, P546
- P642, P643, P645
- P741, P743, P746
- P841

1.1 Standard Safety Statements

For safety information please see the Safety Information chapter of the relevant Px4x Technical Manual.

2 HARDWARE DESCRIPTION

IEC 61850 and DNP3 work over Ethernet. Two boards are available, the single Ethernet board and the Redundant Ethernet board (ZN0071). Both are required for communications but the redundant Ethernet board allows an alternative path to be always available, providing bumpless redundancy.

Industrial network failure can be disastrous. Redundancy provides increased security and reliability, but also devices can be added to or removed from the network without network downtime.

The following list shows Schneider Electric's implementation of Ethernet redundancy, which has six variants with embedded IEC 61850 or DNP3 over Ethernet, plus SHP, RSTP and DHP redundancy protocols.

- Self Healing Protocol (SHP) with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (ST connector) and **modulated** IRIG-B input. Part number ZN0071 001.
- SHP with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (ST connector) and **unmodulated** IRIG-B input. Part number ZN0071 002.

Note *Both of these boards offer compatibility with C264-SWR202 and MiCOM H35x multi-mode switches. Self Healing Protocol is a Schneider Electric proprietary solution providing extremely fast recovery time.*

- Rapid Spanning Tree Protocol (RSTP IEEE 802.1D 2004) with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (ST connector) and **modulated** IRIG-B input. Part number ZN0071 005.
- RSTP (RSTP IEEE 802.1D 2004) with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (ST connector) and **unmodulated** IRIG-B input. Part number ZN0071 006.

Note *Both of these boards offer compatibility with any RSTP device.*

- Dual Homing Protocol (DHP) with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (ST connector) and **modulated** IRIG-B input. Part number ZN0071 007.
- DHP with 1300 nm multi mode 100BaseFx fiber optic Ethernet ports (ST connector) and **unmodulated** IRIG-B input. Part number ZN0071 008.

Note *Both of these boards offer compatibility with C264-SWD202 and H36x multi-mode switches. Dual Homing Protocol is a Schneider Electric solution providing bumpless redundancy to the IED.*

The redundant Ethernet board is fitted into Slot A of the IED, which is the optional communications slot. Each Ethernet board has two MAC addresses, one for the managed embedded switch and one for the IED. The MAC address of the IED is printed on the rear panel of the IED.

For information concerning installation, refer to the Best Practice document *GP02 Ethernet Wiring*.

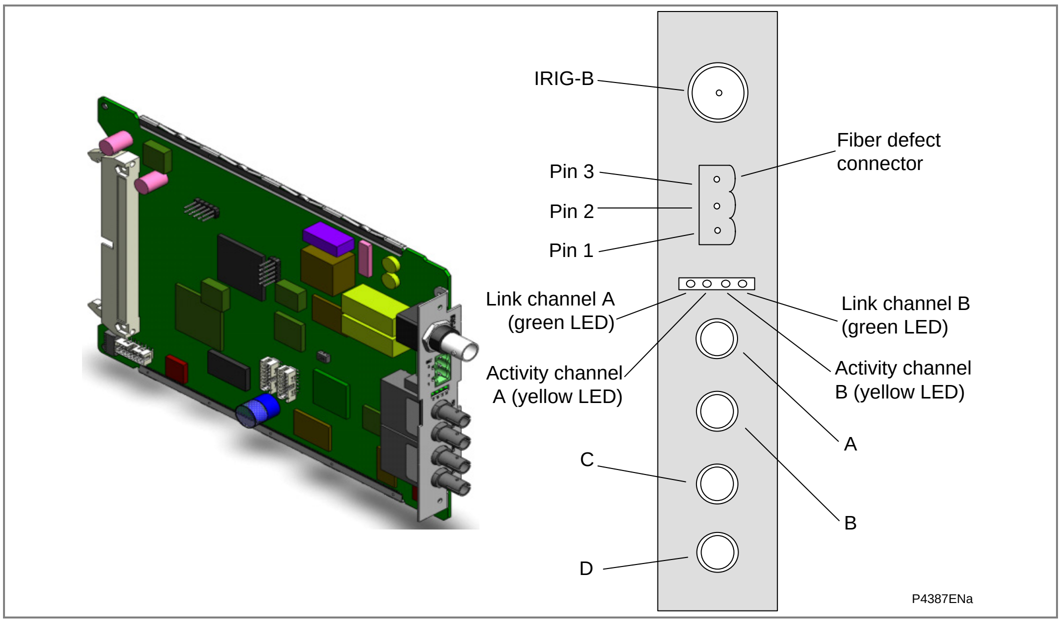

IRIG-B
Fiber defect connector
Pin 3
Pin 2
Pin 1
Link channel A (green LED)
Link channel B (green LED)
Activity channel A (yellow LED)
Activity channel B (yellow LED)
A
C
B
D
P4387ENa

Figure 1 - Redundant Ethernet board connectors

2.1 IRIG-B Connector

Available as a modulated or demodulated input. See section 6.1.

2.2 Fiber Defect Connector (Watchdog Relay)

Pin	Closed	Open
1-2	Link fail Channel 1 (A)	Link ok Channel 1 (A)
2-3	Link fail Channel 2 (B)	Link ok Channel 2 (B)

Table 1 - RSTP configuration parameters range and default values

2.3 LEDs

LED	Function	On	Off	Flashing
Green	Link	Link ok	Link broken	
Yellow	Activity	SHP running		RSTP or DHP traffic

Table 2 - LED functionality

2.4 Optical Fiber Connectors

Uses 1300 nm multi mode 100BaseFx and ST connectors. See Figure 1 and section 6.1.

Connector	DHP	RSTP	SHP
A	R_{XA}	R_{X1}	R_{P}
B	T_{XA}	T_{X1}	E_{S}
C	R_{XB}	R_{X2}	R_{S}
D	T_{XB}	T_{X2}	E_{P}

Table 3 - Optical fiber connector functionality

3 REDUNDANCY PROTOCOLS

There are three redundancy protocols available:

- RSTP (Rapid Spanning Tree Protocol)
- SHP (Self Healing Protocol)
- DHP (Dual Homing Protocol)

3.1 Rapid Spanning Tree Protocol (RSTP)

Rapid Spanning Tree Protocol (RSTP) is a standard used to quickly reconnect a network fault by finding an alternative path, allowing loop-free network topology. Although RSTP can recover network faults quickly, the fault recovery time depends on the number of devices and the topology. The recovery time also depends on the time taken by the devices to determine the root bridge and compute the port roles (discarding, learning, forwarding). The devices do this by exchanging Bridge Protocol Data Units (BPDUs) containing information about bridge IDs and root path costs. See the IEEE 802.1D 2004 standard for further information.

The Px4x redundant Ethernet board uses the RSTP protocol (802.1w), so a Px4x can attach onto a network as shown in Figure 2.

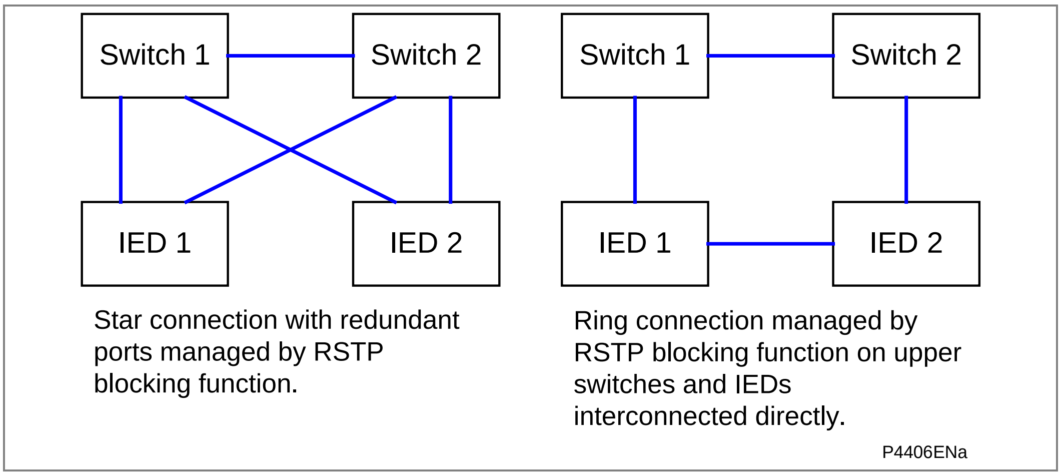

Switch 1
Switch 2
IED 1
IED 2
Star connection with redundant ports managed by RSTP blocking function.
Switch 1
Switch 2
IED 1
IED 2
Ring connection managed by RSTP blocking function on upper switches and IEDs interconnected directly.
P4406ENa

Figure 2 - Px4x attached to a redundant Ethernet star or ring circuit

The RSTP solution is based on open standards. It is therefore compatible with other IEDs that use the RSTP protocol. The RSTP recovery time is typically 300 ms but it increases with network size. However, the Schneider Electric Dual Homing Protocol (DHP) and Self Healing Protocol (SHP) solutions respond to the constraints of critical time applications such as GOOSE.

3.2 Self Healing Protocol (SHP)

Self Healing Protocol (SHP) is applied to double ring network topologies. When a fiber is broken, both end stations detect the break. Using both the primary and redundant networks the ring is automatically reclosed.

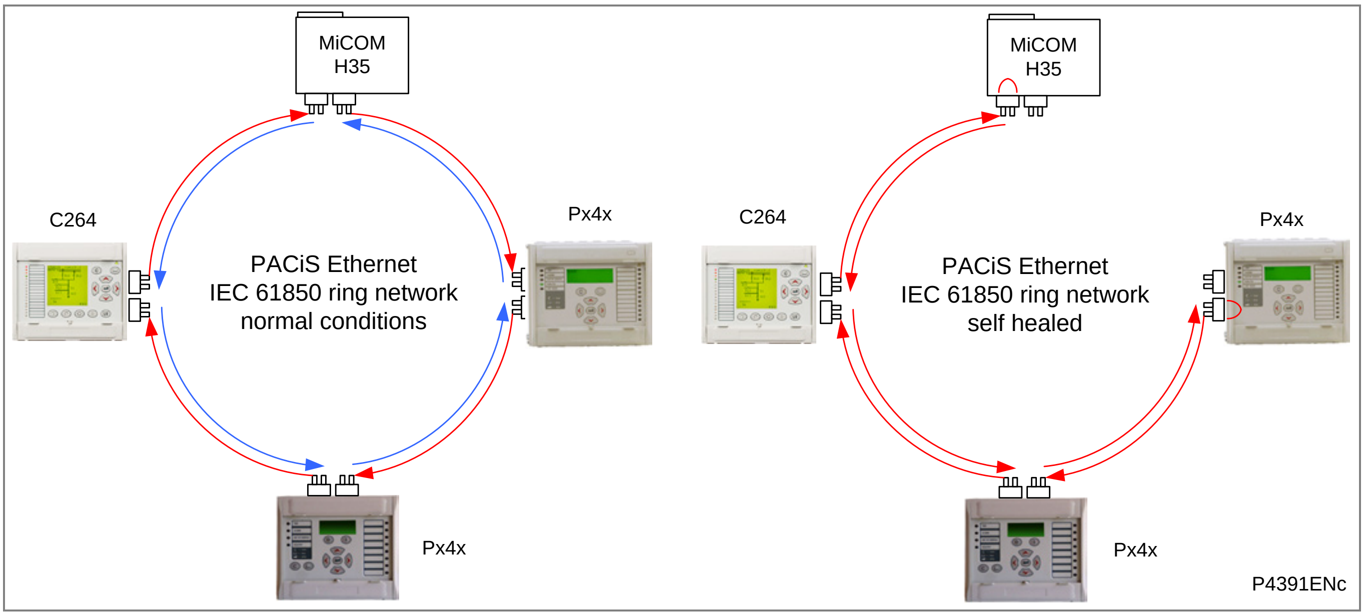

MiCOM
H35
C264
Px4x
PACiS Ethernet
IEC 61850 ring network
normal conditions
Px4x
MiCOM
H35
C264
Px4x
PACiS Ethernet
IEC 61850 ring network
self healed
Px4x
P4391ENc

Figure 3 - MiCOM Px4x, Px3x, C264 and Hx5x Ethernet switch with self healing ring facilities

The MiCOM Px4x, Px3x, C264 and Hx5x are repeaters with a standard 802.3 Ethernet switch plus the Self Healing Manager (SHM). Figure 4 shows the internal architecture of such a device.

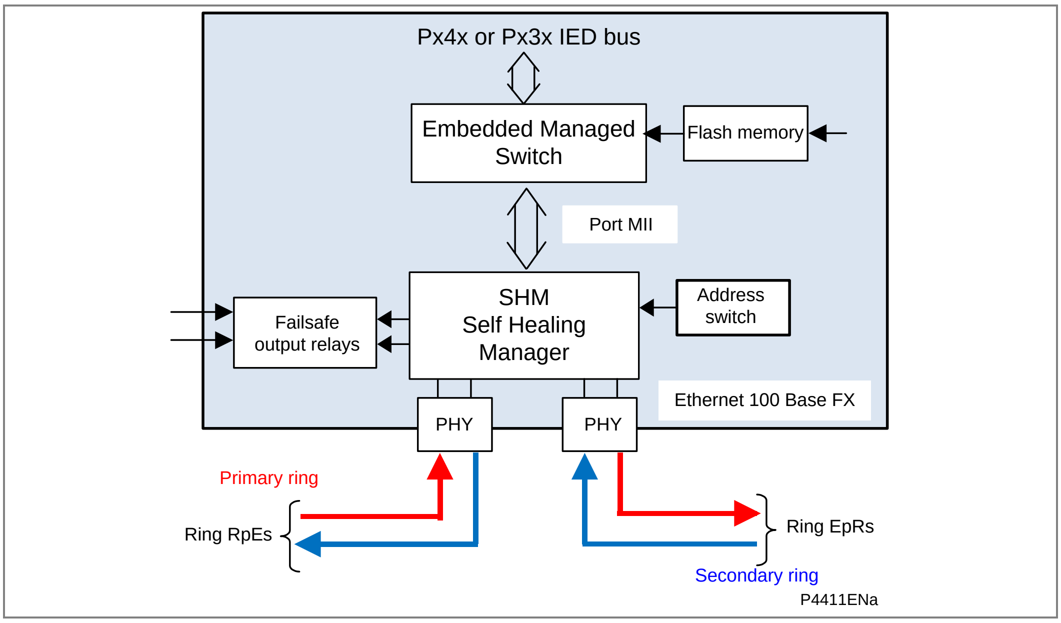

Px4x or Px3x IED bus
Embedded Managed Switch
Flash memory
Port MII
SHM
Self Healing
Manager
Address switch
Failsafe output relays
Ethernet 100 Base FX
PHY
PHY
Primary ring
Ring RpEs
Ring EpRs
Secondary ring
P4411ENa

Figure 4 - Internal architecture of MiCOM Px4x, Px3x, C264 and Hx5x

The SHM functions manage the ring. If the fiber optic connection between two devices is broken, the network continues to run correctly.

Normally the Ethernet packets travel on the primary fiber in the same direction, and only a checking frame (4 octets) is sent every 5 µs on the secondary fiber in the opposite direction.

If the link goes down, both SHMs immediately start the network self-healing. At one side of the break, received messages are no longer sent to the primary fiber but are sent to the secondary fiber. On the other side of the break, messages received on the secondary fiber are sent to the primary fiber and the new topological loop is closed in less than 1 ms.

It is therefore possible to extend the number of devices, or the size of a sub-station network, without stopping the network. The loop is opened and it self heals, then new equipment is connected and it self heals again, closing the loop.

To increase the reliability some specific mechanisms are used:

- The quality of transmission is monitored. Each frame (Ethernet packet or checking frame) is controlled by the SHM. If a large error rate is detected, the self healing starts and the fault is eliminated.
- Even if there is no traffic in the primary link, the secondary link is still supervised by sending out checking frames every 5 µs.

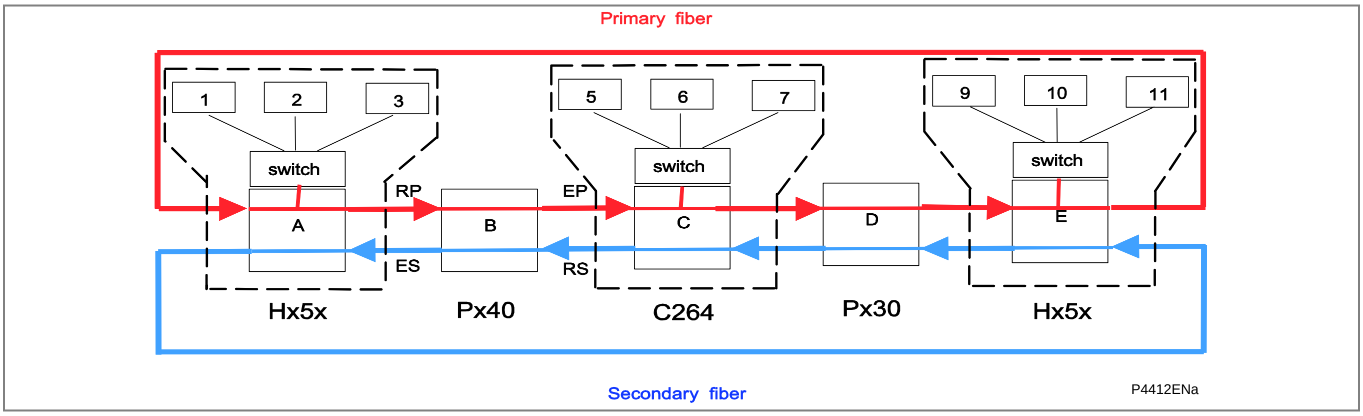

Primary fiber
1
2
3
switch
A
RP
ES
B
5
6
7
switch
EP
RS
C
D
9
10
11
switch
E
Hx5x
Px40
C264
Px30
Hx5x
Secondary fiber
P4412ENa

Figure 5 - Nominal redundant Ethernet ring architecture with MiCOM Px4x, Px3x, C264 and Hx5x switches

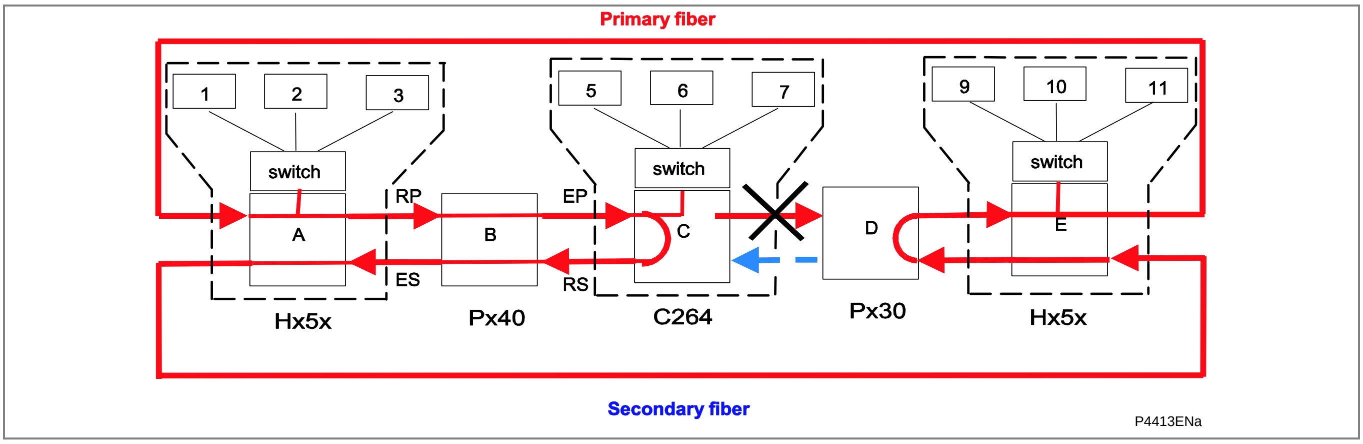

Primary fiber
1
2
3
switch
A
RP
ES
B
5
6
7
switch
EP
RS
C
D
9
10
11
switch
E
Hx5x
Px40
C264
Px30
Hx5x
Secondary fiber
P4413ENa

Figure 6 - Ethernet ring architecture with MiCOM Px4x, Px3x, C264 and Hx5x switches after failure

3.3 Dual Homing Protocol (DHP)

The Dual Homing Manager (DHM) functions manage the double star. If the optical fiber connection between two devices is broken, the network continues to operate correctly.

The DHM handles topologies where a device is connected to two independent networks. One is the main link, the other is the backup. Both are active at the same time.

In sending mode, packets from the device are sent by the DHM to the two networks. In receive mode, the duplicate discard principle is used. This means that when both links are up, the MiCOM H16x receives the same Ethernet frame twice. The DHM transmits the first frame received to upper layers for processing, and the second frame is discarded. If one link is down, the frame is sent through the link, received by the device, and passed to upper layers for processing.

Schneider Electric's dual homing mechanism fulfils automation requirements by delivering a very fast recovery time for the entire network (less than 1 ms).

To increase reliability some specific mechanisms are used:

- Each frame carries a sequence number which is incremented and inserted into both frames.
- Specific frames are used to synchronize the discard mechanism.

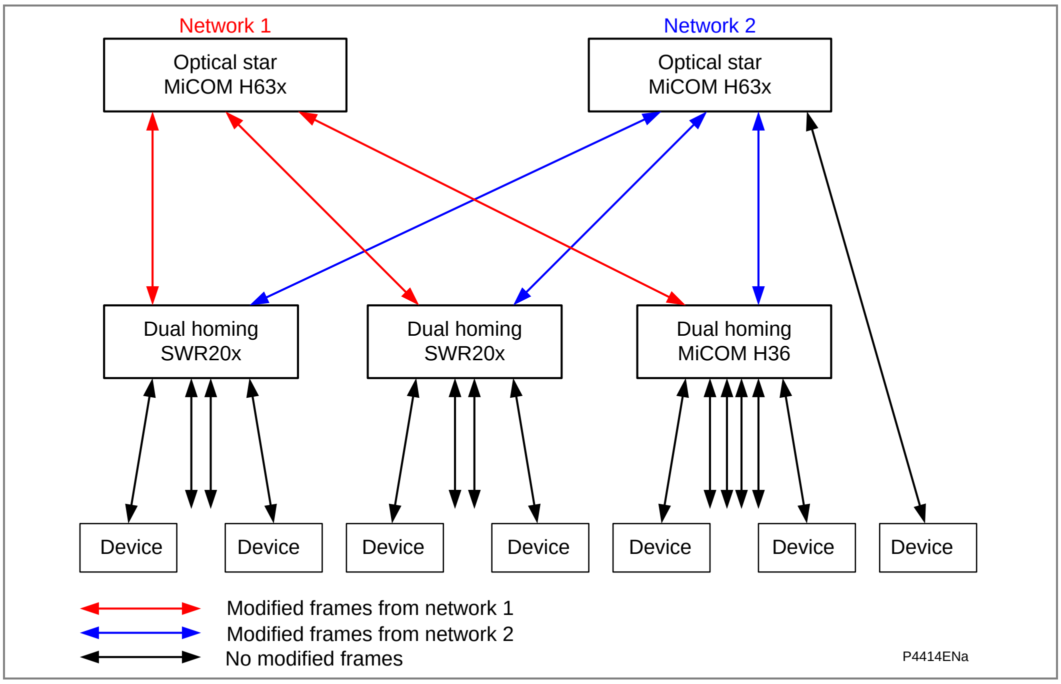

Network 1
Optical star
MiCOM H63x
Network 2
Optical star
MiCOM H63x
Dual homing
SWR20x
Dual homing
SWR20x
Dual homing
MiCOM H36
Device
Device
Device
Device
Device
Device
Device
Modified frames from network 1
Modified frames from network 2
No modified frames
P4414ENa

Figure 7 - Dual homing mechanism

The MiCOM H36x is a repeater with a standard 802.3 Ethernet switch, plus the dual homing manager. Figure 8 shows the internal architecture of such a device.

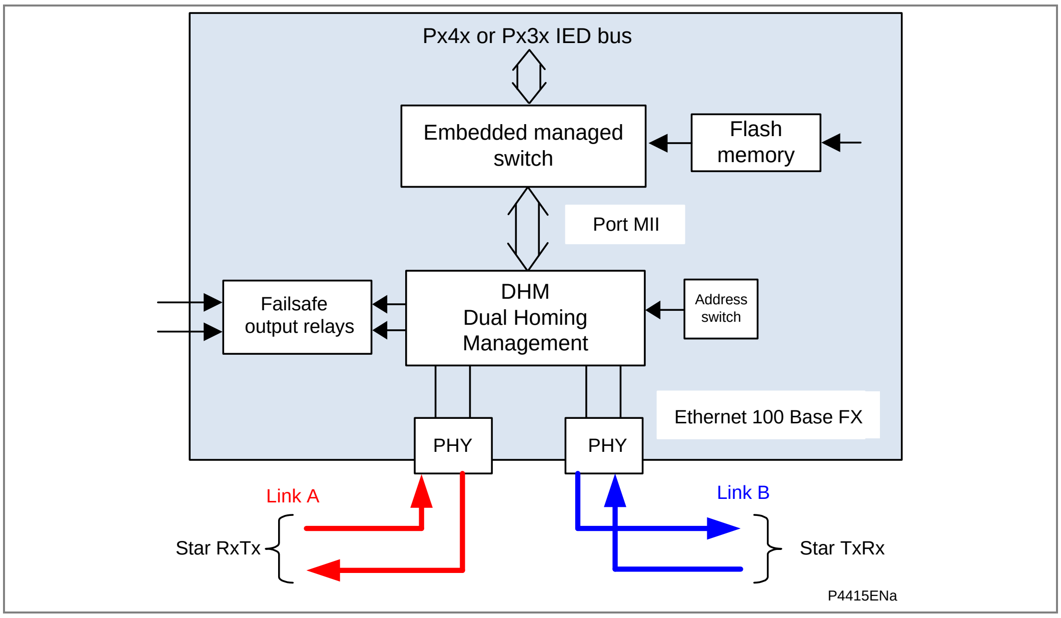

Px4x or Px3x IED bus
Embedded managed switch
Flash memory
Port MII
Failsafe output relays
DHM Dual Homing Management
Address switch
Ethernet 100 Base FX
PHY
PHY
Link A
Link B
Star RxTx
Star TxRx
P4415ENa

Figure 8 - Internal architecture of MiCOM Px4x, Px3x, C264 and H36x

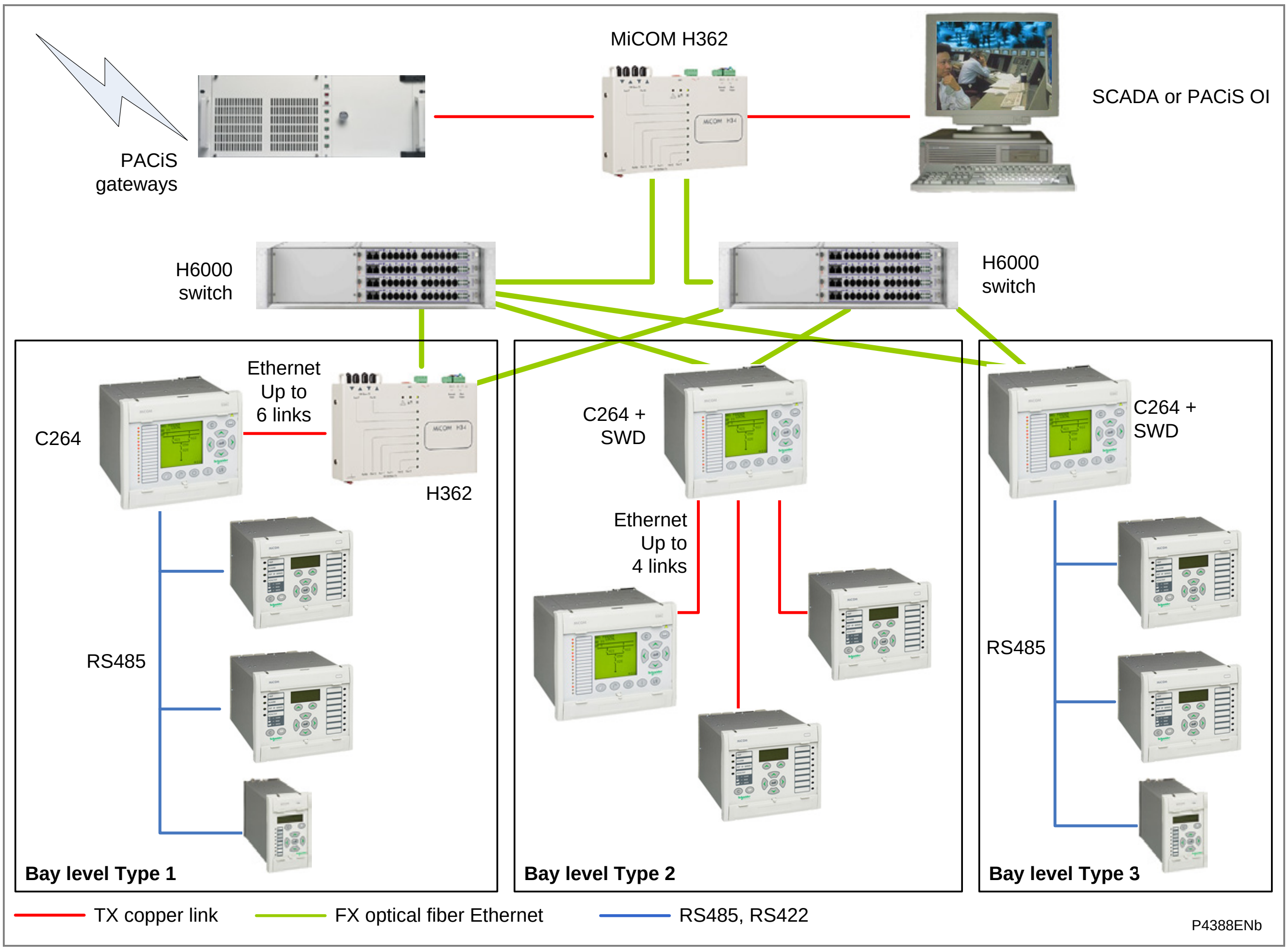

MiCOM H362
SCADA or PACiS OI
PACiS gateways
H6000 switch
H6000 switch
Ethernet Up to 6 links
C264
H362
C264 + SWD
C264 + SWD
Ethernet Up to 4 links
RS485
RS485
Bay level Type 1
Bay level Type 2
Bay level Type 3
TX copper link
FX optical fiber Ethernet
RS485, RS422
P4388ENb

Figure 9 - Application of dual homing star at substation level

3.4 Generic Functions for all Redundant Ethernet Boards

The following apply to all three redundant Ethernet protocols (RSTP, SHP and DHP).

3.4.1 Ethernet 100Base Fx

The fiber optic ports are full duplex 100 Mbps ST connectors.

3.4.2 Forwarding

The MiCOM Px4x, Px3x, C264, Hx1x and Hx5x switches support store and forward mode. The MiCOM switch forwards messages with known addresses to the appropriate port. The messages with unknown addresses, the broadcast messages and the multicast messages are forwarded out to all ports except the source port. MiCOM switches do not forward error packets, 802.3x pause frames or local packets.

3.4.3 Priority Tagging

802.1p priority is enabled on all ports.

3.4.4 Simple Network Management Protocol (SNMP)

Simple Network Management Protocol (SNMP) is the network protocol developed to manage devices in an IP network. SNMP relies on a Management Information Base (MIB) that contains information about parameters to supervise. The MIB format is a tree structure, with each node in the tree identified by a numerical Object IDentifier (OID). Each OID identifies a variable that can be read or set using SNMP with the appropriate software. The information in the MIBs is standardized.

3.4.4.1 Redundant Ethernet Board MIB Structure

The SNMP MIB consists of distinct OIDs, each of which refers to a defined collection of specific information used to manage devices on the Schneider Electric ring. The Schneider Electric MIB uses three types of OID.

Address												Name	
0												Ccitt	
	1											ISO	
		3										Org	
			6									DOD	
				1								Internet	
					2							mgmt	
						1						Mib-2	
							1					sys	
								1				sysDescr	Schneider Electric repeater
								3				sysUpTime	xday yh:zm:zzs:yyms
								4				sysName	

Table 4 - Redundant Ethernet board MIB Structure

3.4.5 RMON

Address												Name
0												Ccitt
	1											ISO
		3										Org
			6									DOD
				1								Internet
					2							mgmt
						1						Mib-2
							16					Rmon
								1				stat
									1			etherstat
										1	9	Port number (*)
											10	etherStatsIndex etherStatsUndersizePkts
											12	etherStatsIndex etherStatsOversizePkts
											13	etherStatsIndex etherStatsJabbers
											14	etherStatsIndex etherStatsCollisions
											15	etherStatsIndex etherStatsPkts64Octets
											16	etherStatsIndex etherStatsPkts65to127Octets
											17	etherStatsIndex etherStatsPkts128to255Octets
											18	etherStatsIndex etherStatsPkts256to511Octets
											19	etherStatsIndex etherStatsPkts512to1023Octets

Table 5 - Redundant Ethernet board MIB Structure

*Port number: 1 to 6 for the RJ45, port 7 management, port 8 ring

Various SNMP client software tools can be used with the MiCOM Px4x, C264 and Hx5x range. Schneider Electric recommends using an SNMP MIB browser which can perform the basic SNMP operations such as GET, GETNEXT, RESPONSE.

To access the network using SNMP, use the IP address of the embedded switch in the redundant Ethernet board. See section 4.2.

3.4.6 Simple Network Time Protocol (SNTP)

Simple Network Time Protocol (SNTP) is supported by both the IED and the redundant Ethernet switch. SNTP is used to synchronize the clocks of computer systems over packet-switched, variable-latency data networks. A jitter buffer is used to reduce the effects of variable latency introduced by queuing in packet switched networks, ensuring a continuous data stream over the network.

The IED receives the synchronization from the SNTP server. This is done using the IP address of the SNTP server entered into the IED from the IED Configurator software.

4 CONFIGURATION

An Internet Protocol (IP) address is a logical address assigned to devices in a computer network that uses the Internet Protocol for communication between nodes. IP addresses are stored as binary numbers but they are usually displayed in the following format.

10 . 86 . 254 . 85

Both the IED and the redundant Ethernet board each have their own IP address. Figure 10 shows the IED as IP1 and the redundant Ethernet board (REB) as IP2. Note that IP1 and IP2 must be different and are in the same subnet mask.

The switch IP address must be configured through the network.

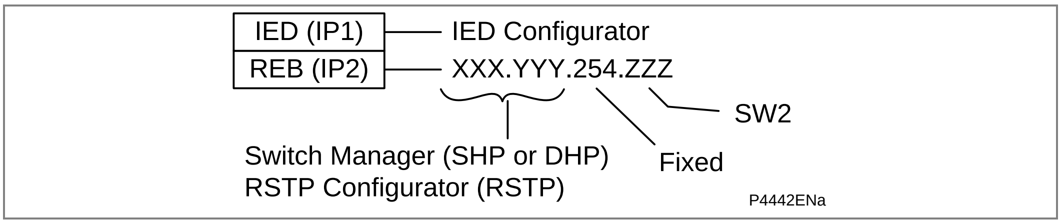


Figure 10 - IED and redundant Ethernet board IP address configuration

4.1 Configuring the IED IP Address

The IP address of the IED is configured using the IED Configurator software in MiCOM S1 Studio. If using IEC 61850 the IED IP address is set using the IED Configurator. If using DNP3 over Ethernet, the IED IP address is managed directly through the DNP3 file. The available range is 128 to 254 in the last octet of the IED IP address.

Note: In the IED Configurator, set the port type to **Copper**, not **Fiber**.

4.2 Configuring the Board IP Address

The IP address of the redundant Ethernet board is configured in both software and hardware, as shown in Figure 10. Therefore this must be configured before connecting the IED to the network to avoid an IP address conflict.

4.2.1 Configuring the First Two Octets of the Board IP address

If using Self Healing Protocol or Dual Homing Protocol, the first two octets are configured using Switch Manager (see section 4.3) or an SNMP MIB browser (see section 3.4.4). An H35 (SHP) or H36 (DHP) network device is needed in the network to configure the Px40 redundant Ethernet board IP address using SNMP.

If using Rapid Spanning Tree Protocol, the first two octets are configured using the RSTP Configurator software tool (see section 4.4) or using an SNMP MIB browser (see section 3.4.4).

4.2.2 Configuring the Third Octet of the Board IP Address

The third octet is fixed at 254, regardless of the protocol.

4.2.3 Configuring the Last Octet of the Board IP Address

The last octet is configured using board address switch SW2 on the board. It is necessary to first remove the IED front cover to gain access to the board address switch, regardless of the redundant protocol.

1. Refer to the safety section of the IED.
2. Switch the IED off. Disconnect the power and all connections.
3. Before the front cover is removed take precautions to prevent electrostatic discharge damage, according to the ANSI/ESD-20.20 -2007 standard.
4. Wear a 1 MΩ earth strap and connect it to the ground (earth) point on the back of the IED. See Figure 11.

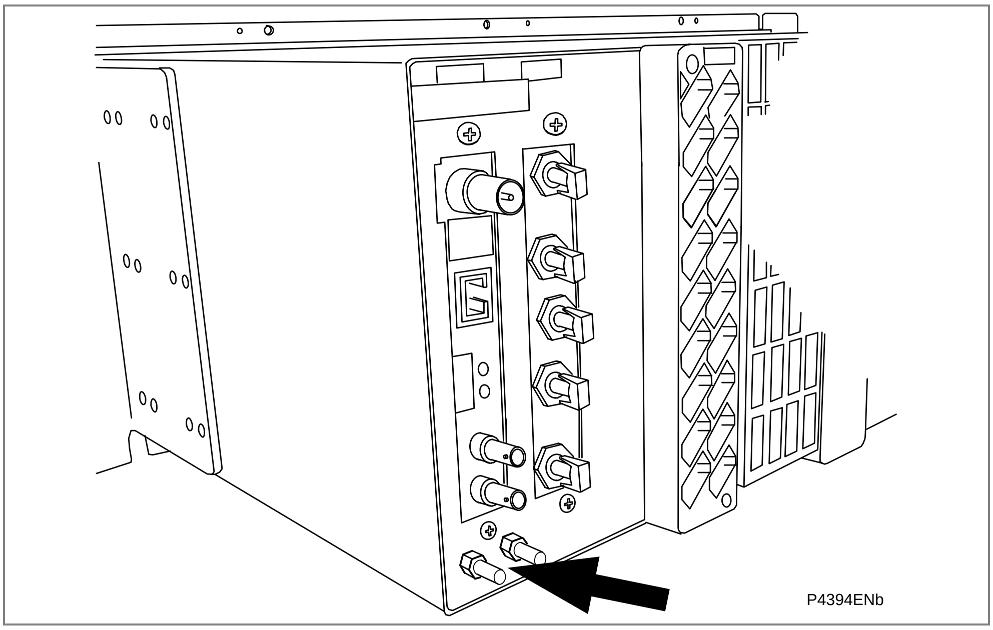


Figure 11 - IED earth (ground) point

5. Remove the six screws securing the front panel.

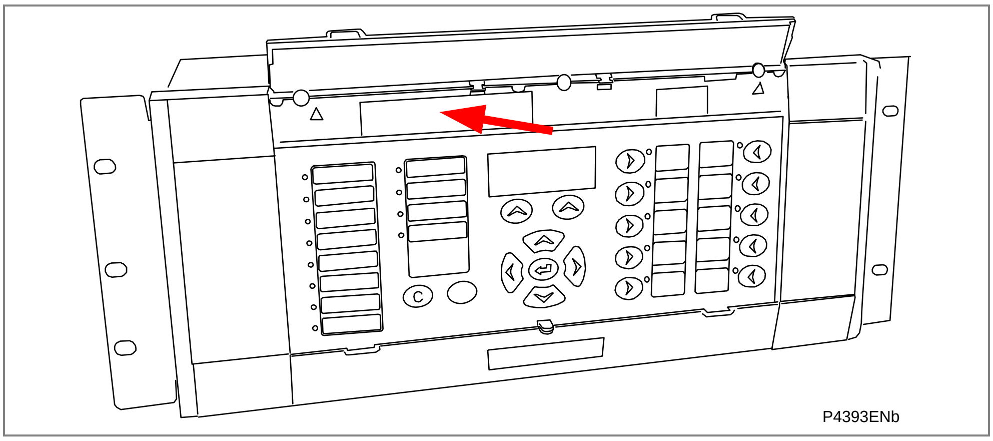


Figure 12 - IED front panel

6. Remove the front panel and disconnect the ribbon cable from the front panel. You now have access to the address switches on the dual Ethernet board.

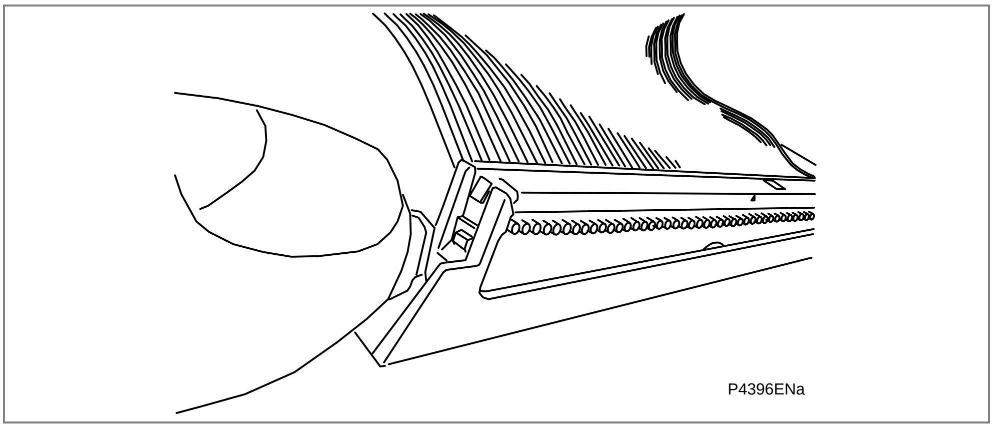


Figure 13 - Ribbon cable connector

7. Set the last octet of the board IP address. The available address range is 1 to 127. See Figure 14.

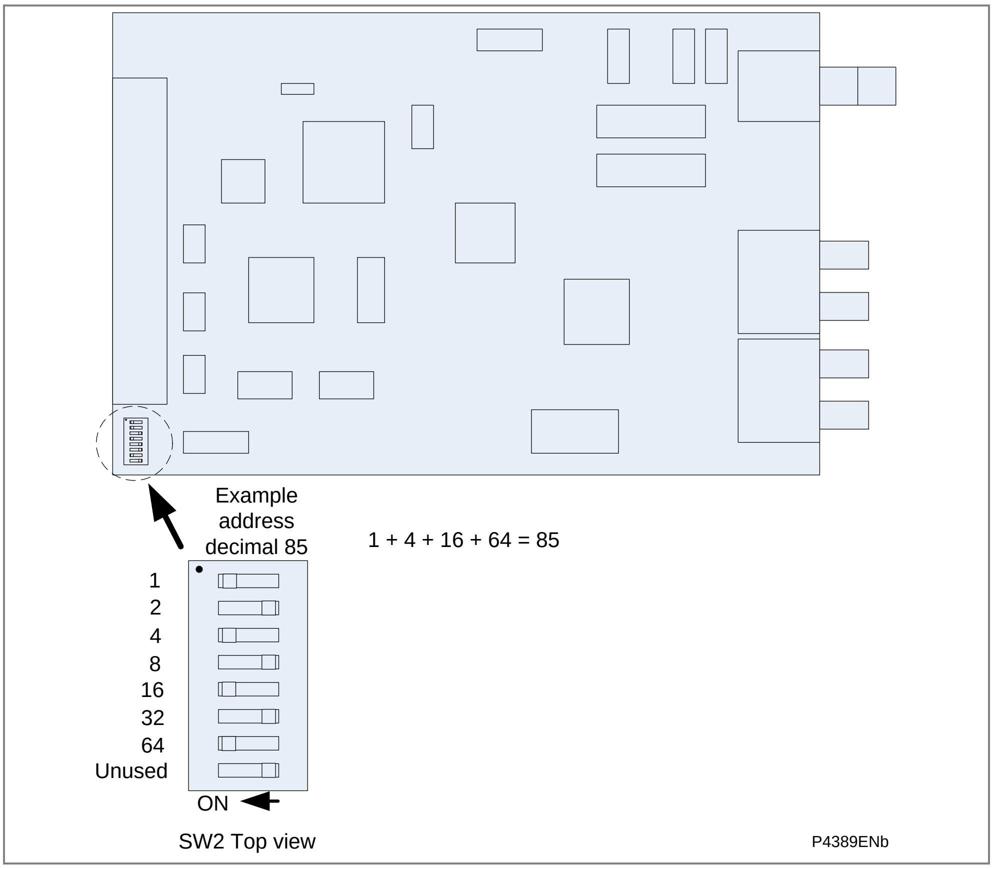

Example address decimal 85
1 + 4 + 16 + 64 = 85
1
2
4
8
16
32
64
Unused
ON
SW2 Top view
P4389ENb

Figure 14 - Dual Ethernet board address switches (SW2)

8. Once the IP address of the board is changed, reassemble the relay in the reverse order. Take care not to damage the pins of the ribbon cable connector on the front panel when reinserting the ribbon cable.

4.3 Switch Manager Software

For further information see the *Switch Manager Operation Guide*.

4.4 RSTP Configurator Software

When running the RSTP protocol, the RSTP Configurator software is used to identify a device, configure the IP address, configure the SNTP IP address and configure RSTP settings.

4.4.1 Connecting the IED to a PC

Connect the IED to the PC on which RSTP Configurator will run. This connection is done through an Ethernet switch or through a media converter. See Figure 15.

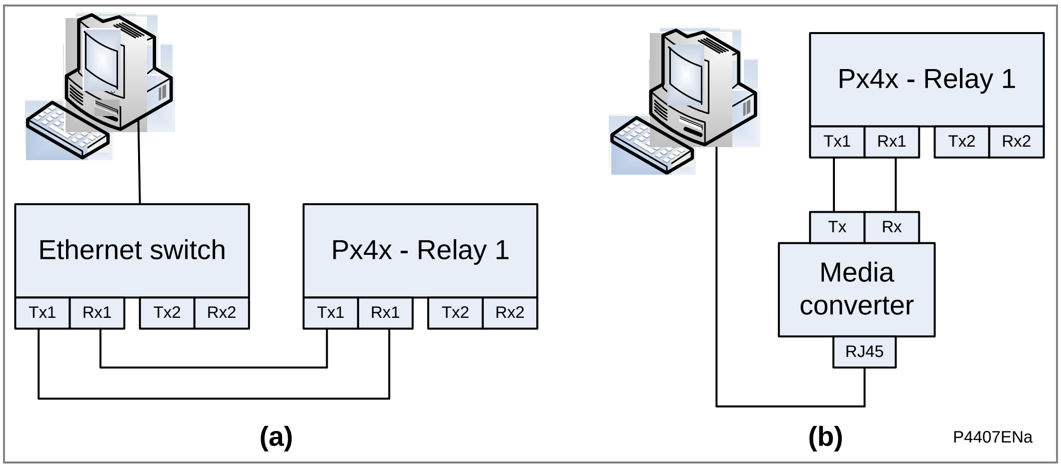

Ethernet switch
Tx1
Rx1
Tx2
Rx2
Px4x - Relay 1
Tx1
Rx1
Tx2
Rx2
(a)
Px4x - Relay 1
Tx1
Rx1
Tx2
Rx2
Tx
Rx
Media converter
RJ45
(b)
P4407ENa

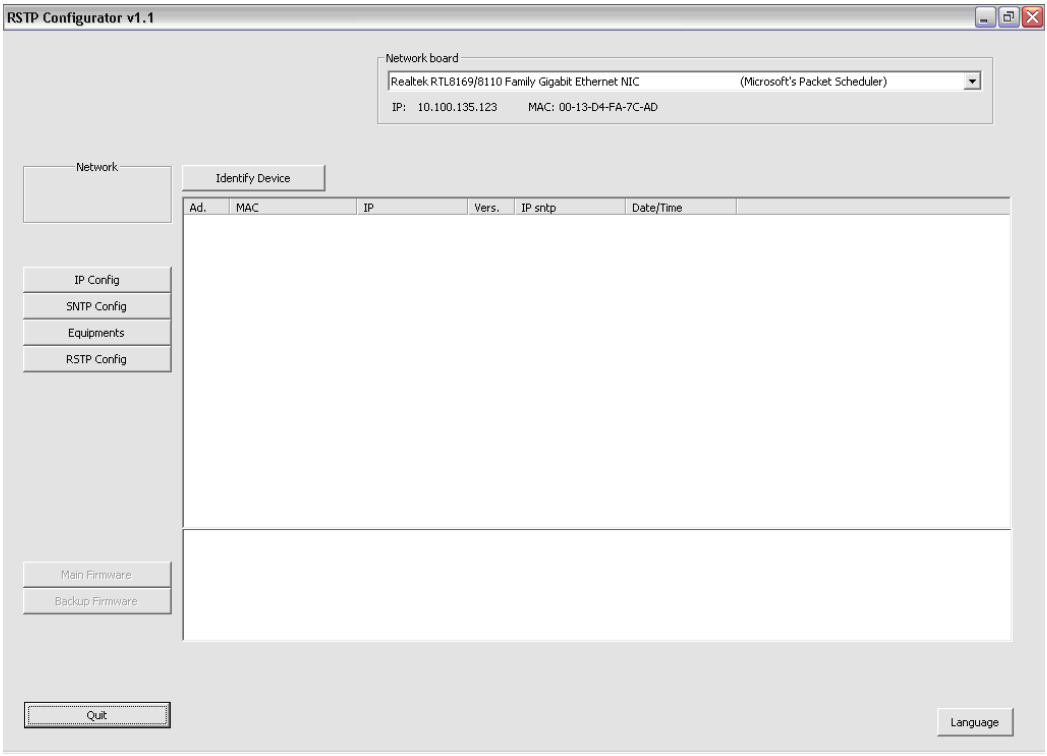
Figure 15 - Connection using (a) an Ethernet switch and (b) a media converter

4.4.2 Installing RSTP Configurator

1. Double click **WinPcap_4_0.exe** to install WinPcap.
2. Double click **Schneider-RSTP Configurator.msi** to install the RSTP Configurator.
3. The setup wizard appears. Click **Next** and follow the on-screen instructions to run the installation.

4.4.3 Starting the RSTP Configurator

1. To start the RSTP Configurator, select **Programs** > **RSTP Configurator** > **RSTP Configurator**.
2. The Login screen appears. For user mode login, enter the **Login name** as **User** and click **OK** with no password.
3. If the login screen does not appear, check all network connections.
4. The main window of the RSTP Configurator appears. The **Network Board** drop-down list shows the Network Board, IP Address and MAC Address of the PC in which the RSTP Configurator is running.



RSTP Configurator v1.1

Network board

Realtek RTL8169/8110 Family Gigabit Ethernet NIC (Microsoft's Packet Scheduler)

IP: 10.100.135.123 MAC: 00-13-D4-FA-7C-AD

Network
Identify Device
Ad.
MAC
IP
Vers.
IP sntp
Date/Time
IP Config
SNTP Config
Equipments
RSTP Config
Main Firmware
Backup Firmware
Quit
Language

P0301ENa

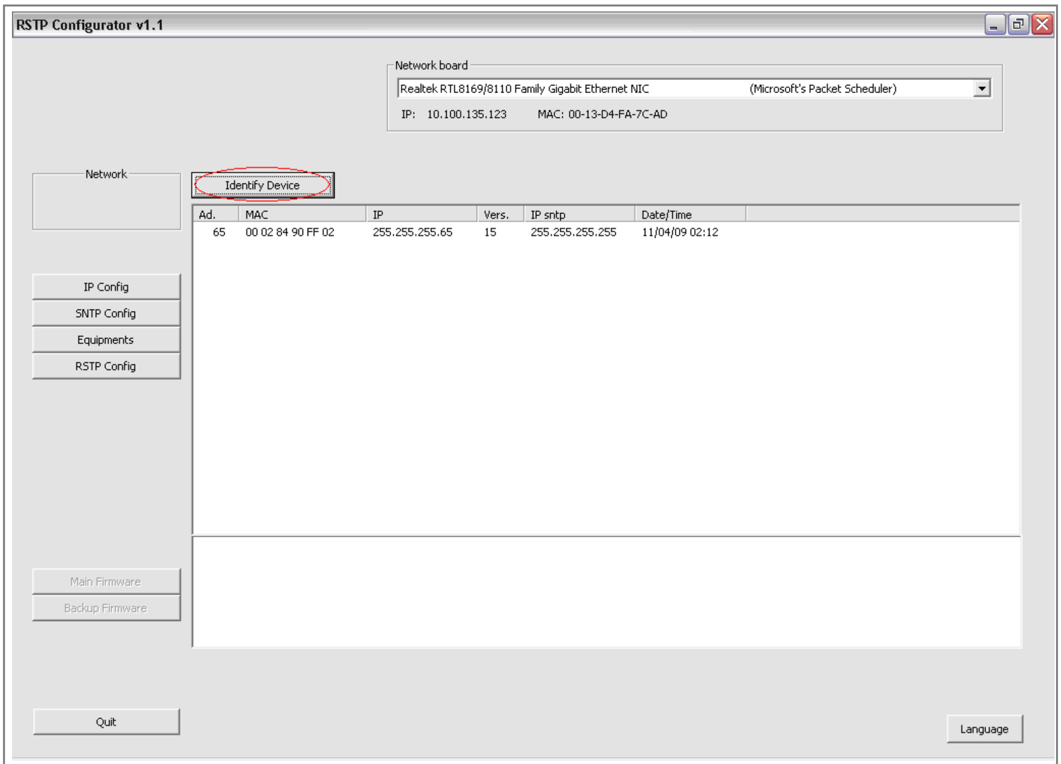
4.4.4 Device Identification

To configure the redundant Ethernet board, go to the main window and click **Identify Device**.

Note *Due to the time needed to establish the RSTP protocol, it is necessary to wait 25 seconds between connecting the PC to the IED and clicking the **Identify Device** button.*

The redundant Ethernet board connected to the PC is identified and its details are listed.

- Device address
- MAC address
- Version number of the firmware
- SNTP IP address
- Date & time of the real-time clock, from the board.


RSTP Configurator v1.1
Network
IP Config
SNTP Config
Equipments
RSTP Config
Main Firmware
Backup Firmware
Quit
Identify Device
Language

Network board: Realtek RTL8169/8110 Family Gigabit Ethernet NIC (Microsoft's Packet Scheduler)

IP: 10.100.135.123 MAC: 00-13-D4-FA-7C-AD

Ad.	MAC	IP	Vers.	IP sntp	Date/Time
65	00 02 84 90 FF 02	255.255.255.65	15	255.255.255.255	11/04/09 02:12

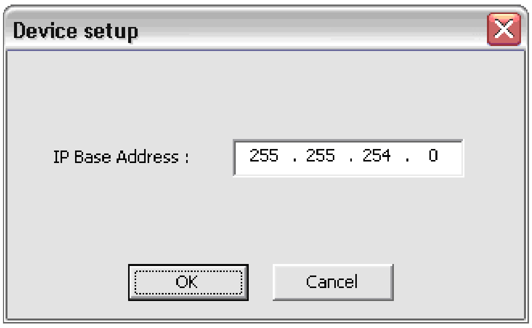
P0302ENa

4.4.5 IP Address Configuration

To change the network address component of the IP address, go to the main window and click the **IP Config** button.

The **Device setup** screen appears. The first three octets of the board IP address can be configured. The last octet is set using the DIP switches (SW2) next to the ribbon connector. See Figure 14.

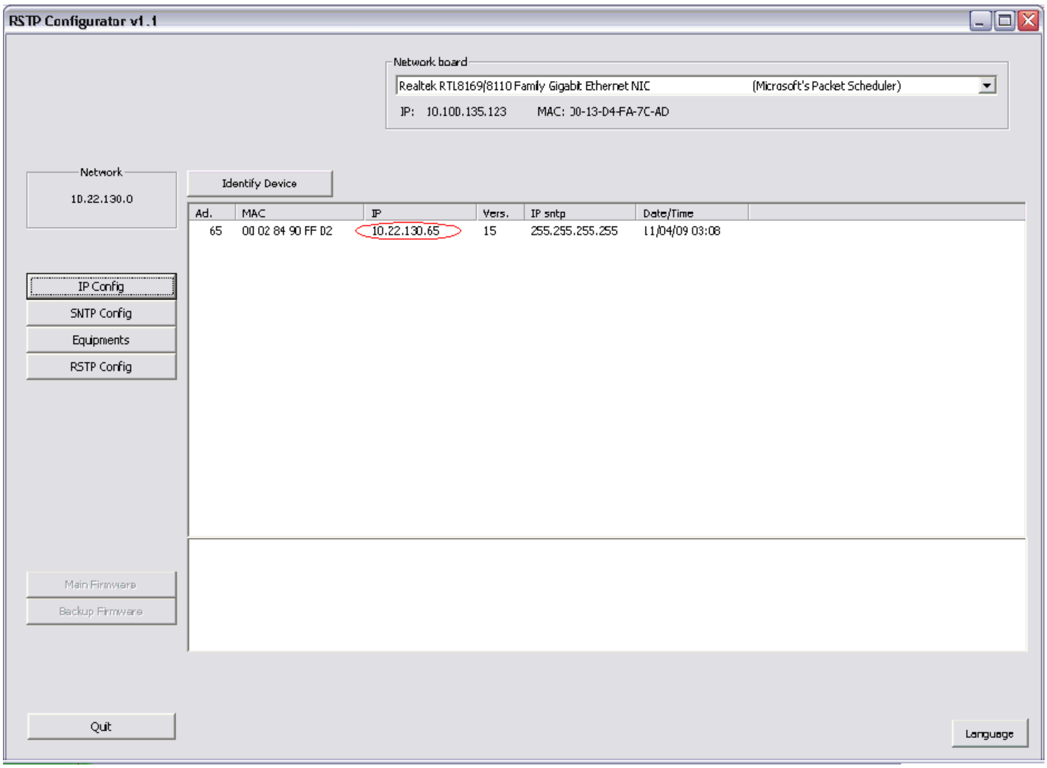
Enter the required board IP address in the IP Base Address box, then click **OK**.


Device setup
OK
Cancel

IP Base Address : 255 . 255 . 254 . 0

P0303ENa

The board network address is updated and displayed in the main window.


RSTP Configurator v1.1
Network board
Network
Identify Device
IP Config
SNTP Config
Equipments
RSTP Config
Main Firmware
Backup Firmware
Quit
Language

Network board: Realtek RTL8169/8110 Family Gigabit Ethernet NIC (Microsoft's Packet Scheduler)

IP: 10.100.135.123 MAC: 00-13-D4-FA-7C-AD

Network: 10.22.130.0

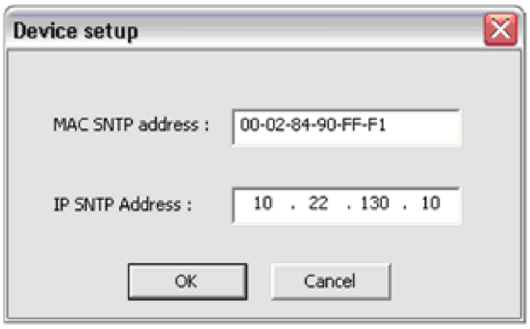
Ad.	MAC	IP	Vers.	IP sntp	Date/Time
65	00 02 84 90 FF 02	10.22.130.65	15	255.255.255.255	11/04/09 03:08

P0304ENa

4.4.6 SNTP IP Address Configuration

To Configure SNTP server IP address, go to the main window and click the **SNTP Config** button. The **Device setup** screen appears.

Enter the required SNTP MAC and server IP address. Then click **OK**.

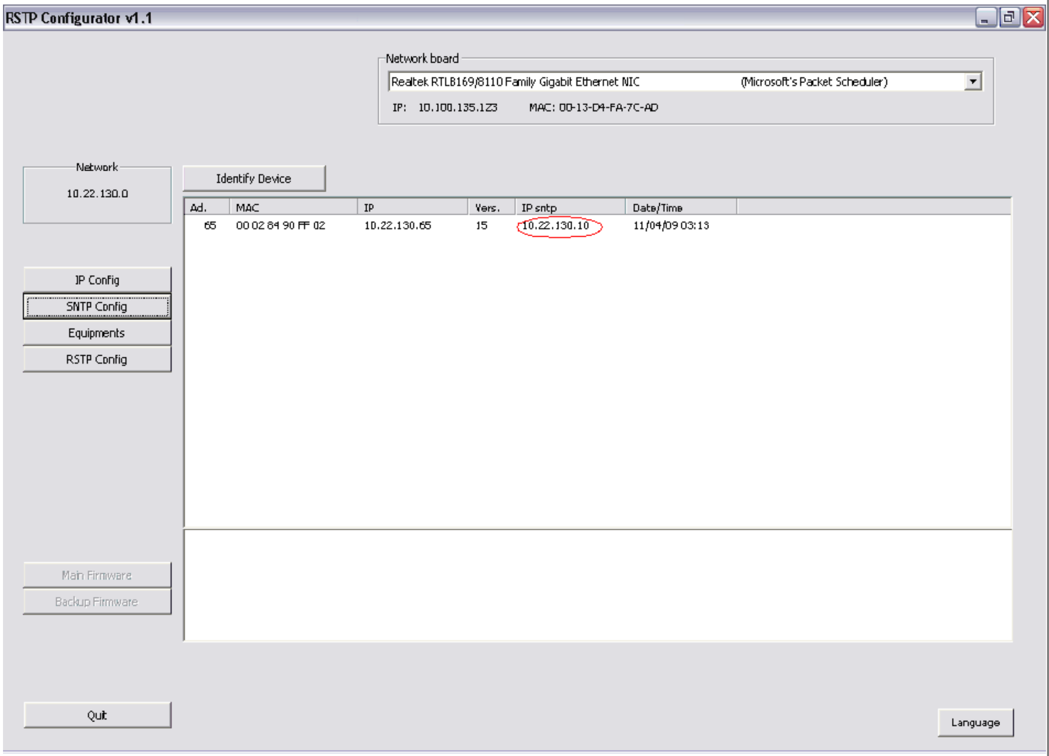

Device setup
OK
Cancel

MAC SNTP address : 00-02-84-90-FF-F1

IP SNTP Address : 10 . 22 . 130 . 10

P0305ENa

The updated SNTP server IP address appears in the main screen.


RSTP Configurator v1.1

Network board: Realtek RTL8169/8110 Family Gigabit Ethernet NIC (Microsoft's Packet Scheduler)

IP: 10.100.135.123 MAC: 00-13-D4-FA-7C-AD

Network: 10.22.130.0

Ad.	MAC	IP	Vers.	IP sntp	Date/Time
65	00 02 84 90 FF 02	10.22.130.65	15	10.22.130.10	11/04/09 03:13

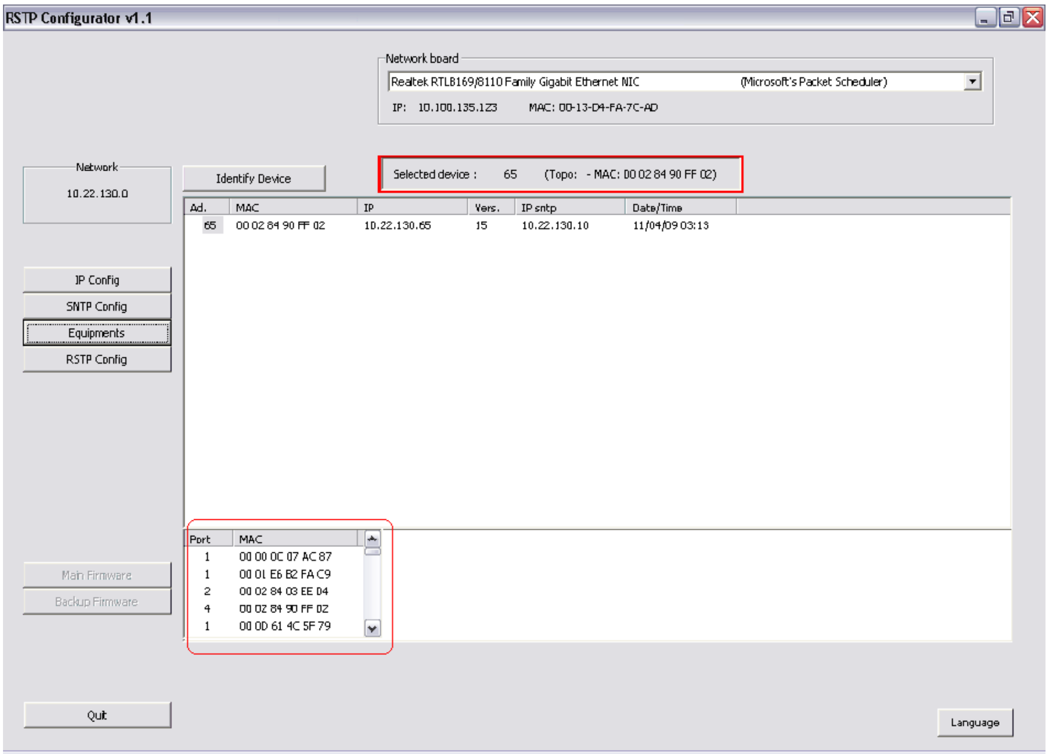
Identify Device
IP Config
SNTP Config
Equipments
RSTP Config
Main Firmware
Backup Firmware
Quit
Language

P0306ENa

4.4.7 Equipment

To view the MAC addresses learned by the switch, go to the main window and click the **Identify Device** button. The selected device MAC address then appears highlighted.

Click the **Equipment** button. The list of MAC addresses learned by the switch and the corresponding port number are displayed.


RSTP Configurator v1.1
Network board
Network
Identify Device
IP Config
SNTP Config
Equipments
RSTP Config
Main Firmware
Backup Firmware
Quit
Language

Realtek RTL8169/8110 Family Gigabit Ethernet NIC (Microsoft's Packet Scheduler)

IP: 10.100.135.123 MAC: 00-13-D4-FA-7C-AD

Network: 10.22.130.0

Selected device : 65 (Topo: - MAC: 00 02 84 90 FF 02)

Ad.	MAC	IP	Vers.	IP sntp	Date/Time
65	00 02 84 90 FF 02	10.22.130.65	15	10.22.130.10	11/04/09 03:13

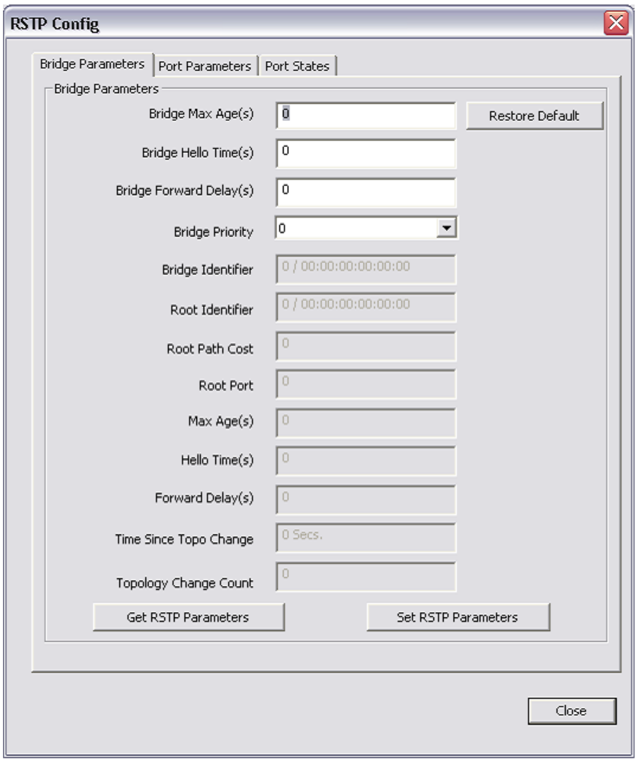
Port	MAC
1	00 00 0C 07 AC 87
1	00 01 E6 B2 FA C9
2	00 02 84 03 EE D4
4	00 02 84 90 FF 02
1	00 0D 61 4C 5F 79

P0307ENa

4.4.8 RSTP Configuration

To view or configure the RSTP Bridge Parameters, go to the main window and click the device address to select the device. The selected device MAC address appears highlighted.

Click the **RSTP Config** button. The RSTP Config screen appears.



RSTP Config
Bridge Parameters
Port Parameters
Port States
Bridge Parameters
Restore Default
Get RSTP Parameters
Set RSTP Parameters
Close

Bridge Max Age(s): 0
Bridge Hello Time(s): 0
Bridge Forward Delay(s): 0
Bridge Priority: 0
Bridge Identifier: 0 / 00:00:00:00:00:00
Root Identifier: 0 / 00:00:00:00:00:00
Root Path Cost: 0
Root Port: 0
Max Age(s): 0
Hello Time(s): 0
Forward Delay(s): 0
Time Since Topo Change: 0 Secs.
Topology Change Count: 0

P0308ENa

To view the available parameters in the board that is connected, click the **Get RSTP Parameters** button.

To set the configurable parameters such as **Bridge Max Age**, **Bridge Hello Time**, **Bridge Forward Delay**, and **Bridge Priority**, modify the parameter values according to Table 1 and click **Set RSTP Parameters**.

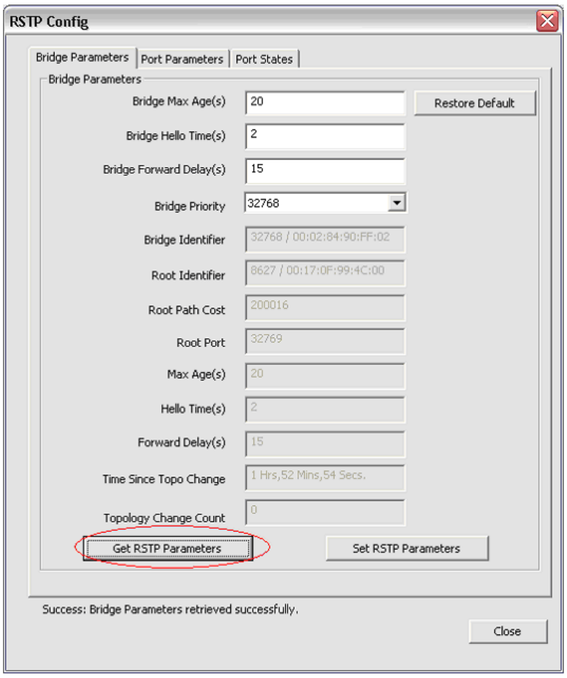
S.No	Parameter	Default value (second)	Minimum value (second)	Maximum value (second)
1	Bridge Max Age	20	6	40
2	Bridge Hello Time	2	1	10
3	Bridge Forward Delay	15	4	30
4	Bridge Priority	32768	0	61440

Table 6 - RSTP configuration parameters range and default values

4.4.8.1 Bridge Parameters

To read the RSTP bridge parameters from the board, go to the main window and click the device address to select the device. The **RSTP Config** window appears and the default tab is **Bridge Parameters**.

Click the **Get RSTP Parameters** button. This displays all the RSTP bridge parameters from the Ethernet board.


RSTP Config
Bridge Parameters
Port Parameters
Port States
Bridge Parameters
Restore Default
Get RSTP Parameters
Set RSTP Parameters
Close

Bridge Max Age(s)	20
Bridge Hello Time(s)	2
Bridge Forward Delay(s)	15
Bridge Priority	32768
Bridge Identifier	32768 / 00:02:84:90:FF:02
Root Identifier	8627 / 00:17:0F:99:4C:00
Root Path Cost	200016
Root Port	32769
Max Age(s)	20
Hello Time(s)	2
Forward Delay(s)	15
Time Since Topo Change	1 Hrs,52 Mins,54 Secs.
Topology Change Count	0

Success: Bridge Parameters retrieved successfully.

P0309ENa

To modify the RSTP parameters, enter the values according to Table 6 and click **Set RSTP Parameters**.

To restore the default values, click **Restore Default** and click **Set RSTP Parameters**.

The grayed parameters are read-only and cannot be modified.

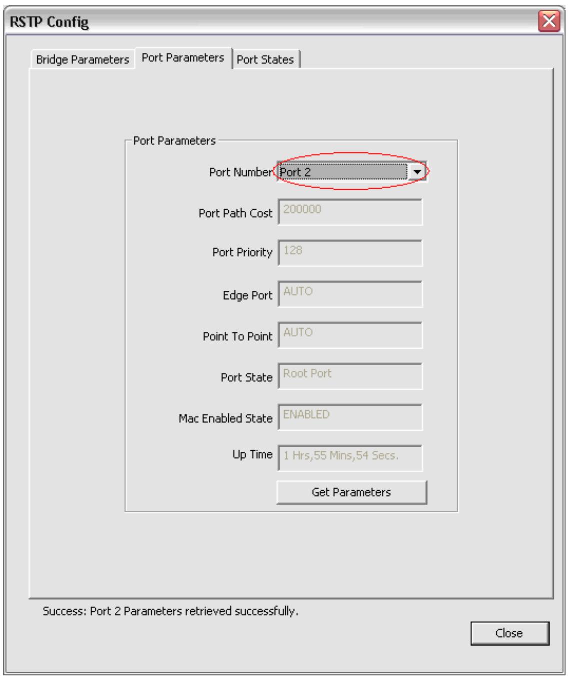
4.4.8.2 Port Parameters

This function is useful if you need to view the parameters of each port.

From the main window, click the device address to select the device and the **RSTP Config** window appears.

Select the **Port Parameters** tab, then click **Get Parameters** to read the port parameters.

Alternatively, select the port numbers to read the parameters.


RSTP Config
Bridge Parameters
Port Parameters
Port States
Port Parameters
Get Parameters
Close

Port Number: Port 2

Port Path Cost: 200000

Port Priority: 128

Edge Port: AUTO

Point To Point: AUTO

Port State: Root Port

Mac Enabled State: ENABLED

Up Time: 1 Hrs,55 Mins,54 Secs.

Success: Port 2 Parameters retrieved successfully.

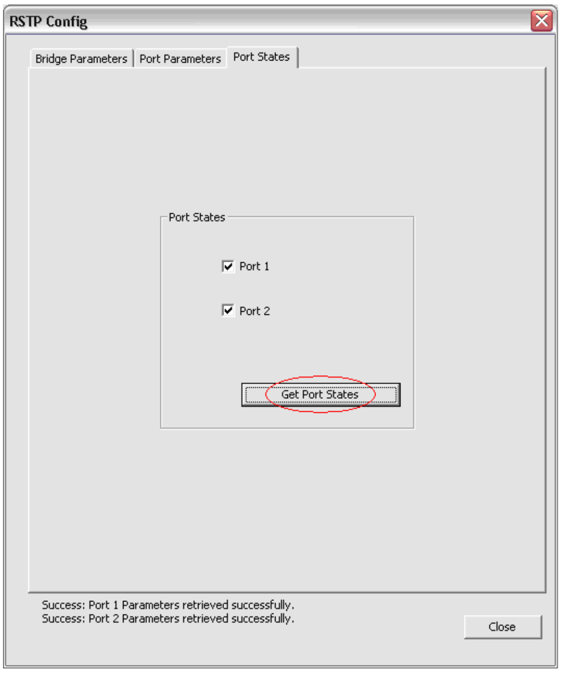
P0310ENa

4.4.8.3 Port States

This is used to see which ports of the board are enabled or disabled.

From the main window, click the device address to select the device. The **RSTP Config** window appears.

Select the **Port States** tab then click the **Get Port States** button. This lists the ports of the Ethernet board. A tick shows they are enabled.


RSTP Config
Bridge Parameters
Port Parameters
Port States
Port States
Get Port States
Close

☑ Port 1

☑ Port 2

Success: Port 1 Parameters retrieved successfully.
Success: Port 2 Parameters retrieved successfully.

P0311ENa

5 COMMISSIONING

5.1 SHP Ring Connection

Connect Es to Rs and Ep to Rp until it makes a ring, as shown in Figure 16.

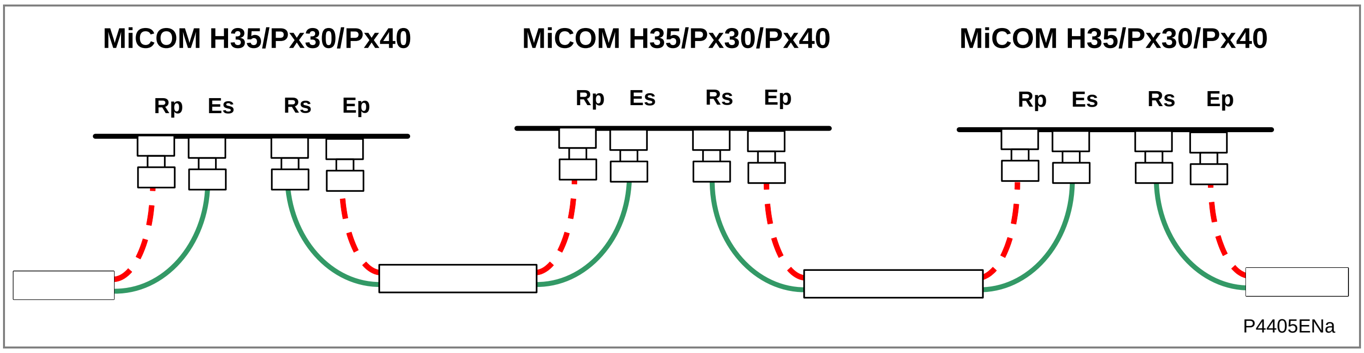

MiCOM H35/Px30/Px40
Rp
Es
Rs
Ep
MiCOM H35/Px30/Px40
Rp
Es
Rs
Ep
MiCOM H35/Px30/Px40
Rp
Es
Rs
Ep
P4405ENa

Figure 16 - Dual Ethernet ring connections

5.2 DHP Star Connection

Connect Tx to Rx and Rx to Tx on each device until it makes a star, as shown in the following diagram.

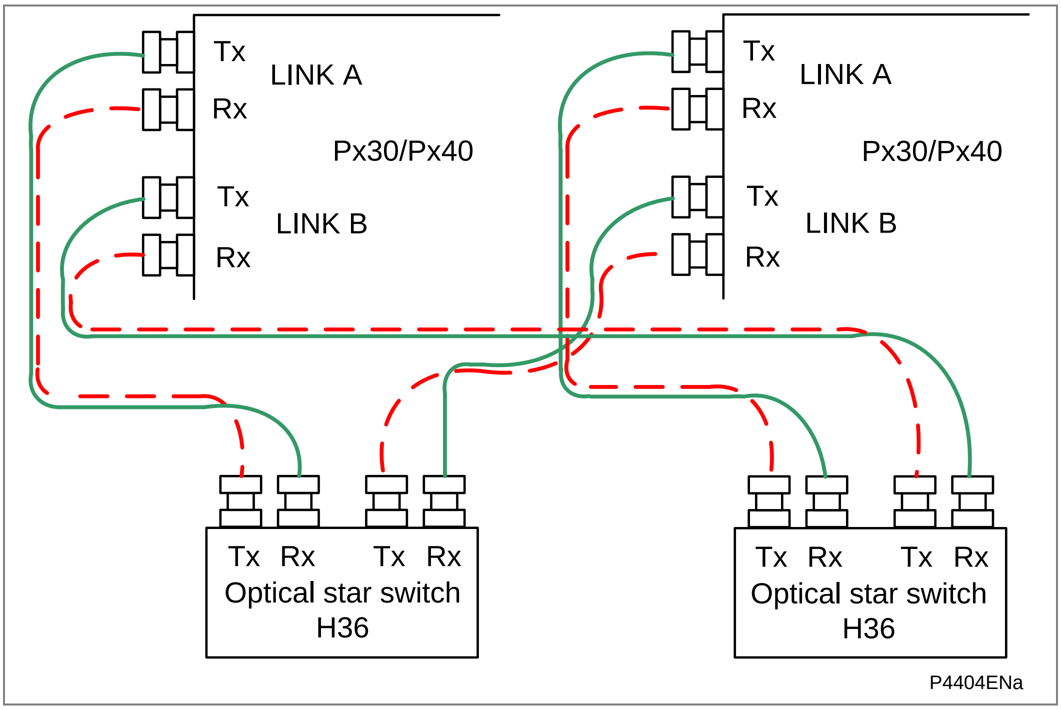

Tx
LINK A
Rx
Px30/Px40
Tx
LINK B
Rx
Tx
LINK A
Rx
Px30/Px40
Tx
LINK B
Rx
Tx Rx Tx Rx
Optical star switch
H36
Tx Rx Tx Rx
Optical star switch
H36
P4404ENa

Figure 17 - Dual Ethernet star connections

5.3 RSTP Ring Connection

Figure 18 shows the Px4x IEDs (Px4x – IED 1 to IED N) with the RSTP variant of redundant Ethernet boards connected in a ring topology. The ring topology can have one or more high-end RSTP-enabled Ethernet switches to interface with another network or control center. The Ethernet switch is an RSTP enabled switch with a higher number of ports.

The Ethernet switch, which is connected to the controlling PC, should be configured as the root bridge. The bridge priority of the Ethernet switch should be configured to the minimum value in the network shown in Figure 18.

The maximum number of IEDs that can be connected in the ring network depends on the Max Age parameter configured in the root bridge, see Figure 20.

The Max Age parameter can be varied from 6 to 40 seconds.

If Max Age = 6 seconds, the minimum number of IEDs in the ring is 6 - 1 = 5.

If Max Age = 40 seconds, the maximum number of IEDs in the ring is 40 - 1 = 39.

Therefore the number of IEDs that can be connected in the ring can vary from 5 to 39.

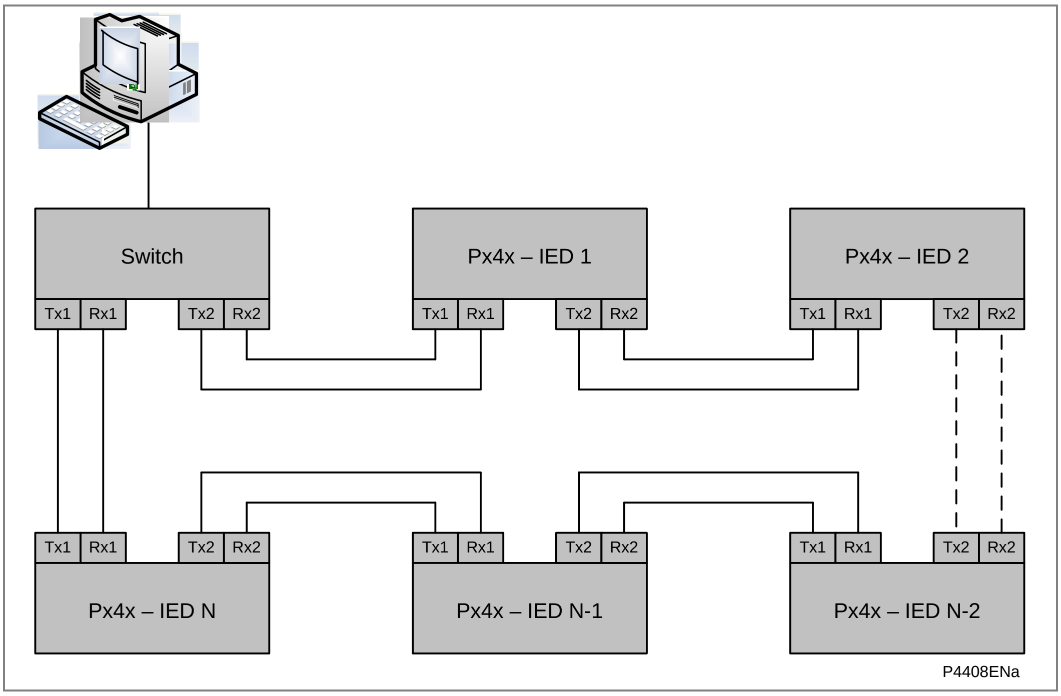


Figure 18 - Dual Ethernet ring topology

5.4 RSTP Star Connection

Figure 19 shows the Px4x IEDs (Px4x – IED 1 to IED N) with the RSTP variant of redundant Ethernet boards connected in a star topology. The star topology can have one or more high-end RSTP-enabled Ethernet switches to interface with other networks, control centers, or Px4x IEDs. The Ethernet switch is an RSTP enabled switch with a greater number of ports. The Ethernet switch, which is connected to the controlling PC, should be configured as the root bridge. The bridge priority of the Ethernet switch should be configured to the minimum value in the network shown in Figure 20.

The Px4x IEDs are placed at two hop distance from the root bridge, therefore the Max Age parameter has no impact on star topology.

The maximum number of IEDs that can be connected in the star network depends on the number of ports available in the Ethernet switch, provided that the hop count from the root bridge is less than the Max Age parameter.

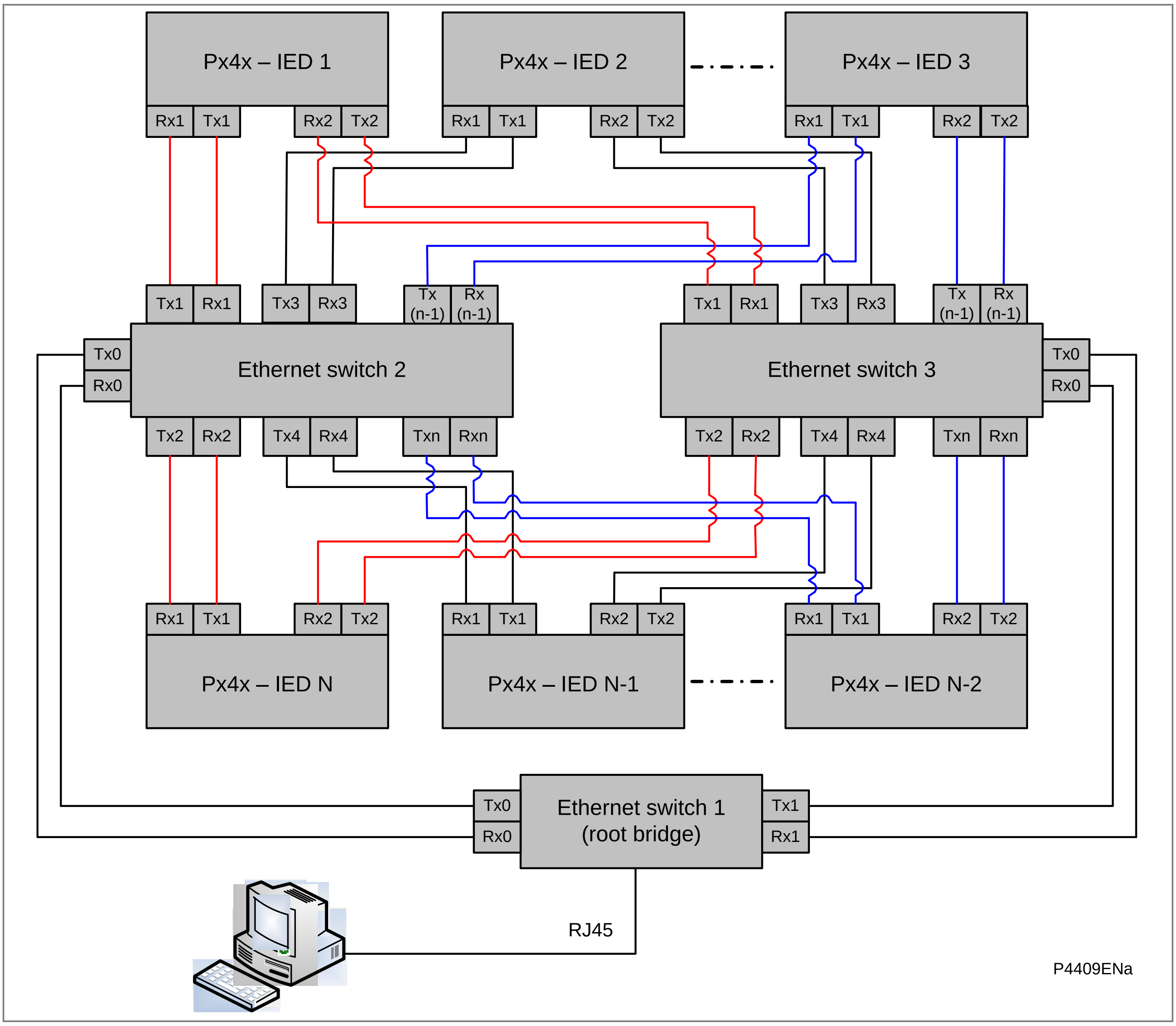

Px4x – IED 1
Px4x – IED 2
Px4x – IED 3
Rx1
Tx1
Rx2
Tx2
Tx3
Rx3
Tx (n-1)
Rx (n-1)
Ethernet switch 2
Ethernet switch 3
Tx0
Rx0
Tx4
Rx4
Txn
Rxn
Px4x – IED N
Px4x – IED N-1
Px4x – IED N-2
Ethernet switch 1 (root bridge)
RJ45
P4409ENa

Figure 19 - Dual Ethernet star topology

5.5 Large RSTP Networks Combining Star and Ring

Figure 20 shows a star of four rings. Each ring is connected to the root bridge. The root bridge is a high-end RSTP enabled bridge with the maximum number of ports as required. The devices A1, A2…Anmax, B1, B2…Bnmax, C1, C2…Cnmax, D1, D2…Dnmax, represent the RSTP variant of redundant Ethernet boards.

The maximum number of boards that can be connected in single ring in an RSTP-enabled network depends on the Max Age parameter. The hop count from the root bridge can not be greater than the Max Age parameter.

The maximum number of RSTP bridges in a ring is given by

Nmax = (Max Age – 1)

Where:

Nmax = maximum number of devices in a ring
Max Age = Max Age value configured in the root bridge.

Assuming the default value of Max Age as 20 seconds in the topology shown 0, the maximum number of devices that can be connected in ring A is 19.

If Max Age is configured as 40 seconds, the maximum number of IEDs that can be connected in the network is (40-1) = 39. According to the IEEE 802.1D 2004 standard, the maximum value for the Max Age parameter is limited to 40. To use the maximum number of IEDs in the ring, the following configuration should be used.

Max Age	40 seconds
Forward Delay	30 seconds
Hello Time	2 seconds

Bridge Priority As required by the end user.

The IEEE 802.1D 2004 standard defines the relation between Max Age and Forward Delay as:

2 * (Forward Delay – 1.0 seconds) >= Max Age

To have the maximum number of nodes in the RSTP network, the number of rings can be increased, depending on the number of ports available in the root bridge.

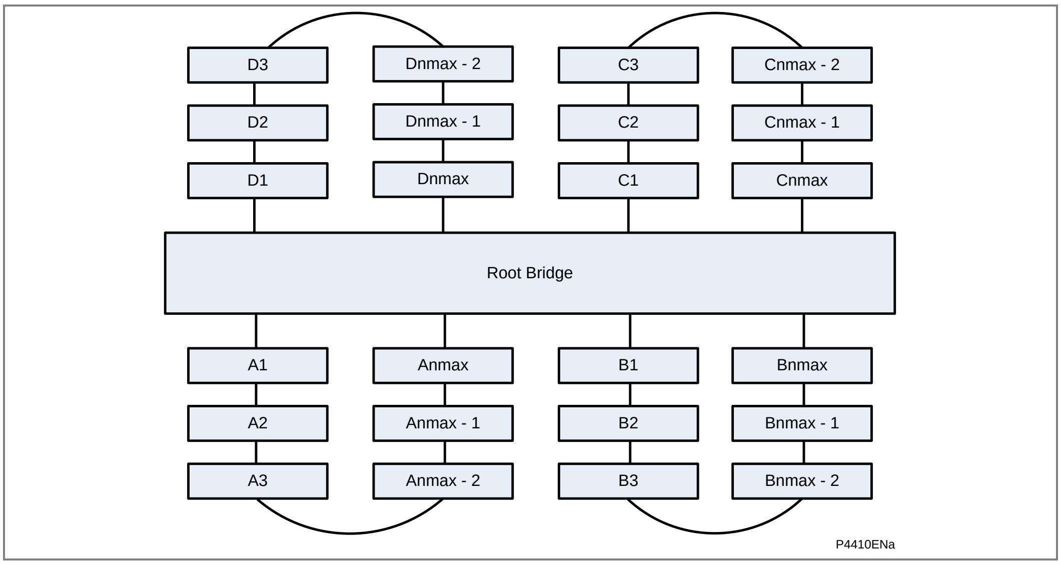


Figure 20 - Combined RSTP star and ring topology

6 TECHNICAL DATA

The technical data applies to a redundant Ethernet board fitted into the following IEDs.

- P141, P142, P143, P144, P145
- P241, P242, P243
- P341, P342, P343, P344, P345
- P442, P443, P444, P445, P446
- P543, P544, P545, P546
- P642, P643, P645
- P741, P743, P746
- P841

6.1 Board Hardware

6.1.1 100 Base FX Interface (in accordance with IEEE802.3 and IEC 61850)

Optical fiber cable	multi-mode 50/125 µm or 62.5/125 µm
Center wavelength	1310 nm
Connector style	BFOC 2.5 -(ST®)
Maximum distance	6.4 km
Full Duplex	100 Mbps

Table 7 - 100 Base FX interface

6.1.2 Transmitter Optical Characteristics

Parameter	Sym	Min.	Typ.	Max.	Unit
Output Optical Power BOL 62.5/125 µm, NA = 0.275 Fiber EOL	PO	-19 -20	-16.8	-14	dBm avg.
Output Optical Power BOL 50/125 µm, NA = 0.20 Fiber EOL	PO	-22.5 -23.5	-20.3	-14	dBm avg.
Optical Extinction Ratio				10 -10	% dB
Output Optical Power at Logic “0” State	PO (“0”)			-45	dBm avg.
BOL - Beginning of life EOL - End of life					

Table 8 - Tx optical characteristics

6.1.3 Receiver Optical Characteristics

Parameter	Sym	Min.	Typ.	Max.	Unit
Input Optical Power Minimum at Window Edge	PIN Min. (W)		-33.5	–31	dBm avg.
Input Optical Power Minimum at Eye Center	PIN Min. (C)		-34.5	-31.8	dBm avg.
Input Optical Power Maximum	PIN Max.	-14	-11.8		dBm avg.

Table 9 - Rx optical characteristics

6.1.4 Fiber Defect Connector (Watchdog Relay)

Connector (3 terminals)	2 NC contacts potential free
Rated voltage	250 VAC
Rated continuous current	5 A
Make current	Max. 30 A and carry for 3s
Breaking capacity AC	1500 VA resistive (cos F = unity) 1500 VA inductive (cos F = 0.5)
Breaking capacity DC	50 W, 250 VDC resistive 25 W inductive (L/R=40 ms)

Table 10 - Fiber defect connector characteristics

6.1.5 IRIG-B and Real-Time Clock

6.1.5.1 Performance

Year 2000: Compliant

Real time accuracy: < ±1 second / day

External clock synchronization: Conforms to IRIG standard 200-98, format B

6.1.5.2 Features

Real time 24 hour clock settable in hours, minutes and seconds

Calendar settable from January 1994 to December 2092

Clock and calendar maintained via battery after loss of auxiliary supply

Internal clock synchronization using IRIG-B Interface for IRIG-B signal is BNC

6.1.5.3 Optional Rear IRIG-B interface (Modulated or Unmodulated)

BNC plug

Isolation to SELV level.

50 ohm coaxial cable.

6.2 Type Tests

6.2.1 Insulation

As for EN 60255-27: 2005 (incorporating corrigendum March 2007):

Insulation resistance > 100 MΩ at 500 Vdc (Using only electronic/brushless insulation tester).

6.2.2 Creepage Distances and Clearances

EN 60255-27: 2005 (incorporating corrigendum March 2007)

Pollution degree 3,

Overvoltage category III,

Impulse test voltage 5 kV.

6.2.3 High Voltage (Dielectric) Withstand

(EIA RS-232 ports excepted and normally-open contacts of output relays excepted).

(i) As for EN 60255-27: 2005 (incorporating corrigendum March 2007), 2 kV rms AC, 1 minute:

Between terminals of all independent circuits.

Between all case terminals connected together, and the case earth (ground).

1 kV rms AC for 1 minute, across open watchdog contacts.

1 kV rms AC for 1 minute, across open contacts of changeover output relays.

1 kV rms AC for 1 minute for all D-type EIA(RS)-232 or EIA(RS)-485 ports between the communications port terminals and protective (earth) conductor terminal.

(ii) As for ANSI/IEEE C37.90-1989 (reaffirmed 1994):

1.5 kV rms AC for 1 minute, across open contacts of normally open output relays.

1k V rms AC for 1 minute, across open watchdog contacts.

1k V rms AC for 1 minute, across open contacts of changeover output relays.

6.2.4 Impulse Voltage Withstand Test

As for EN 60255-27: 2005 (incorporating corrigendum March 2007):

Front time: 1.2 µs, Time to half-value: 50 µs,

Peak value: 5 kV, 0.5 J

Between all independent circuits.

Between all independent circuits and case earth ground).

EIA(RS)-232 & EIA(RS)-485 ports and normally open contacts of output relays excepted.

6.3 ElectroMagnetic Compatibility (EMC)

6.3.1 1 MHz Burst High Frequency Disturbance Test

As for EN 60255-22-1: 2008, Class III

Common-mode test voltage: 2.5 kV
Differential test voltage: 1.0 kV
Test duration: 2 s, Source impedance: 200 Ω (EIA(RS)232 ports excepted)

6.3.2 100 kHz Damped Oscillatory Test

EN 61000-4-18: 2007: Level 3

Common mode test voltage: 2.5 kV
Differential mode test voltage: 1 kV

6.3.3 Immunity to Electrostatic Discharge

As for EN 60255-22-2: 1997, Class 4.

15 kV discharge in air to user interface, display, communication ports and exposed metalwork.

8 kV point contact discharge in air to all communications ports.

6 kV point contact discharge to any part of the front of the product.

6.3.4 Electrical Fast Transient or Burst Requirements

As for IEC 60255-22-4, Class B:

Power supply: Amplitude: 2 kV, Burst frequency: 5 kHz
Inputs / Outputs: Amplitude: 2 kV, Burst frequency: 5 kHz
Communication: Amplitude: 1 kV, Burst frequency: 5 kHz

As for DIN EN 61000-4-4, severity level 4:

Power supply: Amplitude: 4 kV, Burst frequency: 2.5 kHz and 5 kHz
Inputs / Outputs: Amplitude: 2 kV, Burst frequency: 5 kHz
Communication: Amplitude: 2 kV, Burst frequency: 5 kHz
Rise time of one pulse: 5 ns
Impulse duration (50% value): 50 ns
Burst duration: 15 ms
Burst cycle: 300 ms
Source impedance: 50 Ω

6.3.5 Surge Withstand Capability

As for IEEE/ANSI C37.90.1: 2002:

4 kV fast transient and 2.5 kV oscillatory applied directly across each output contact, optically isolated input, and power supply circuit.

6.3.6 Surge Immunity Test

(EIA(RS)232 ports excepted)

As for EN 61000-4-5: 2006 Level 4,

Time to half-value: 1.2 to 50 µs,
Amplitude: 4 kV between all groups and case earth (ground),
Amplitude: 2 kV between terminals of each group.

6.3.7 Immunity to Radiated Electromagnetic Energy

As for EN 61000-4-3:2002 and EN 60255-22-3:2001, Class 3

Test field strength, frequency band 80 to 1000 MHz: 10 V/m,
Test using AM: 1 kHz / 80%, Spot tests at 80, 160, 450, 900 MHz

As for IEEE/ANSI C37.90.2: 2004:

25, 80 MHz to 1000 MHz, zero and 100% square wave modulated, 1 kHz 80% am and am pulse modulated.
Field strength 35 V/m.

6.3.8 Radiated Immunity from Digital Communications

As for EN61000-4-3: 2002, Level 4:

Test field strength, frequency band 800 to 960 MHz, and 1.4 to 2.0 GHz:

30 V/m,
Test using AM: 1 kHz/80%.

6.3.9 Radiated Immunity from Digital Radio Telephones

As for EN 61000-4-3: 2002: 10 V/m, 900 MHz and 1.89 GHz.

6.3.10 Immunity to Conducted Disturbances Induced by Radio Frequency Fields

As for EN 61000-4-6: 1996, Level 3, Disturbing test voltage: 10 V.

6.3.11 Power Frequency Magnetic Field Immunity

As for EN 61000-4-8: 2001, Level 5,

100 A/m applied continuously,
1000 A/m applied for 3 s.

As for EN 61000-4-9: 2001, Level 5,

1000 A/m applied in all planes.

As for EN 61000-4-10: 2001, Level 5,

100 A/m applied in all planes at 100 kHz to 1 MHz with a burst duration of 2 s.

6.3.12 Conducted Emissions

As for EN 55022: 1998 Class A:

0.15 - 0.5 MHz, 79 dBμV (quasi peak) 66 dBμV (average)
0.5 - 30 MHz, 73 dBμV (quasi peak) 60 dBμV (average).

6.3.13 Radiated Emissions

As for EN 55022: 1998 Class A:

30 to 230 MHz, 40 dBμV/m at 10 m measurement distance
230 to 1 GHz, 47 dBμV/m at 10 m measurement distance.

6.4 Environmental Conditions

Ambient Temperature Range

As for EN 60255-6: 1988

Operating temperature range:	-25°C to +55°C (or -13°F to +131°F).
Storage and transit:	-25°C to +70°C (or -13°F to +158°F).

Ambient Humidity Range

As for IEC 60068-2-3: 1969:	56 days at 93% relative humidity and +40°C
As for IEC 60068-2-30: 1980:	Damp heat cyclic, six (12 + 12) hour cycles, 93% RH, +25 to +55°C

6.5 EU Directives

6.5.1 EMC Compliance

As for 2004/108/EC:

Compliance to the European Commission Directive on EMC is demonstrated using a Technical File.

Product Specific Standards were used to establish conformity:

EN 50263: 2000

6.5.2 Product Safety

Refer to MiCOM Px4x Safety Section or four languages Safety Guide (SFTY/4L M/F11)

Compliance to the European Low Voltage Directive 2006/95/EC demonstrated by reference to product safety standard:

CE EN 60255-27: 2005 (incorporating corrigendum March 2007)

6.5.3 R&TTE Compliance

Radio and Telecommunications Terminal Equipment (R & TTE) directive 99/5/EC.

Compliance demonstrated by compliance to both the EMC directive and the Low voltage directive, down to zero volts.

Applicable to rear communications ports.

6.5.4 Other Approvals

For ATEX Potentially Explosive Atmospheres directive 94/9/EC compliance, consult Schneider Electric.

For other approvals such as UL / CUL / CSA, consult Schneider Electric.

6.6 Mechanical Robustness

6.6.1 Vibration Test

As for EN 60255-21-1: 1996:

Response Class 2
Endurance Class 2

6.6.2 Shock and Bump

As for EN 60255-21-2: 1996:

Shock response Class 2
Shock withstand Class 1
Bump Class 1

6.6.3 Seismic Test

As for EN 60255-21-3: 1995:

Class 2

7 CORTEC

This is a generic Cortec to cover all IEDs using the redundant Ethernet board.

Variants Order Number	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
MiCOM Protection	P														
Application/Platform:															
Feeder Management		1	4	*											
Motor Protection		2	4	*											
Generator Protection Relay		3	4	*											
Distance Protection Relay		4	4	*											
Current Differential		5	4	*											
Transformer		6	4	*											
Busbar		7	4	*											
Breaker Fail		8	4	*											
Vx Aux Rating															
24 – 48 Vdc					1										
48-110 Vdc (40-100 Vac)					2										
110-250 Vdc (100-240 Vac)					3										
In/Vn Rating						*									
Hardware Options:															
Standard: no options							1								
IRIG-B only (modulated)							2								
Fibre optic converter only							3								
IRIG-B only (modulated) & fibre optic converter only							4								
Ethernet (10Mbit/s)							5								
Ethernet with 100Mbit/s fibre optic port							6								
2nd Rear Comms Port (Courier EIA232/EIA485/k-bus)							7								
2nd Rear Comms Port + IRIG-B (Courier EIA232/EIA485/k-bus)							8								
Ethernet (100Mbit/s) + IRIG-B only (modulated)							A								
Ethernet (100Mbit/s) + IRIG-B only (unmodulated)							B								
IRIG-B (unmodulated)							C								
IRIG-B (unmodulated) plus Second Rear Comms							D								
InterMiCOM + Courier Rear Port							E								
InterMiCOM + Courier Rear Port + IRIG-B modulated							F								
Redundant Ethernet Self-healing Ring, 2 multi-mode fibre ports + modulated IRIG-B							G								
Redundant Ethernet Self-healing Ring, 2 multi-mode fibre ports + unmodulated IRIG-B							H								
Redundant Ethernet RSTP, 2 multi-mode fibre ports + modulated IRIG-B							J								
Redundant Ethernet RSTP, 2 multi-mode fibre ports + unmodulated IRIG-B							K								
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + modulated IRIG-B							L								
Redundant Ethernet Dual-Homing Star, 2 multi-mode fibre ports + unmodulated IRIG-B							M								
Redundant Ethernet Parallel Redundancy Protocol (PRP), 2 multi-mode fibre ports + modulated IRIG-B							N								
Redundant Ethernet Parallel Redundancy Protocol (PRP), 2 multi-mode fibre ports + unmodulated IRIG-B							P								
Product Specific Options								*							
Protocol Options															
K-Bus / Courier									1						
Modbus									2						
IEC60870-5-103 (VDEW)									3						
DNP3.0									4						
UCA2 + Courier via rear RS485 port									5						
IEC61850 over Ethernet and Courier via rear K-Bus/RS485									6						
IEC61850 over Ethernet with CS103 rear port RS485 protocol									7						
DNP3 over Ethernet with Courier rear port K-Bus/RS485 protocol									8						
Mounting Options															
Panel Mounting										M					
Rack Mounting										N					
Language Options															
Multilingual – English, French, German, Spanish											0				
Multilingual – English, French, German, Italian											4				
Multilingual – English, French, German, Russian											5				
Chinese, English or French via HMI, with English or French via Communications port											C				
Software Version:												*	*		
Settings Files:															
Default														0	
Customer version														A	
Design Suffix:															*

P0361ENa

8 EXTERNAL CONNECTION DIAGRAM

This applies to all IEDs using the redundant Ethernet board.

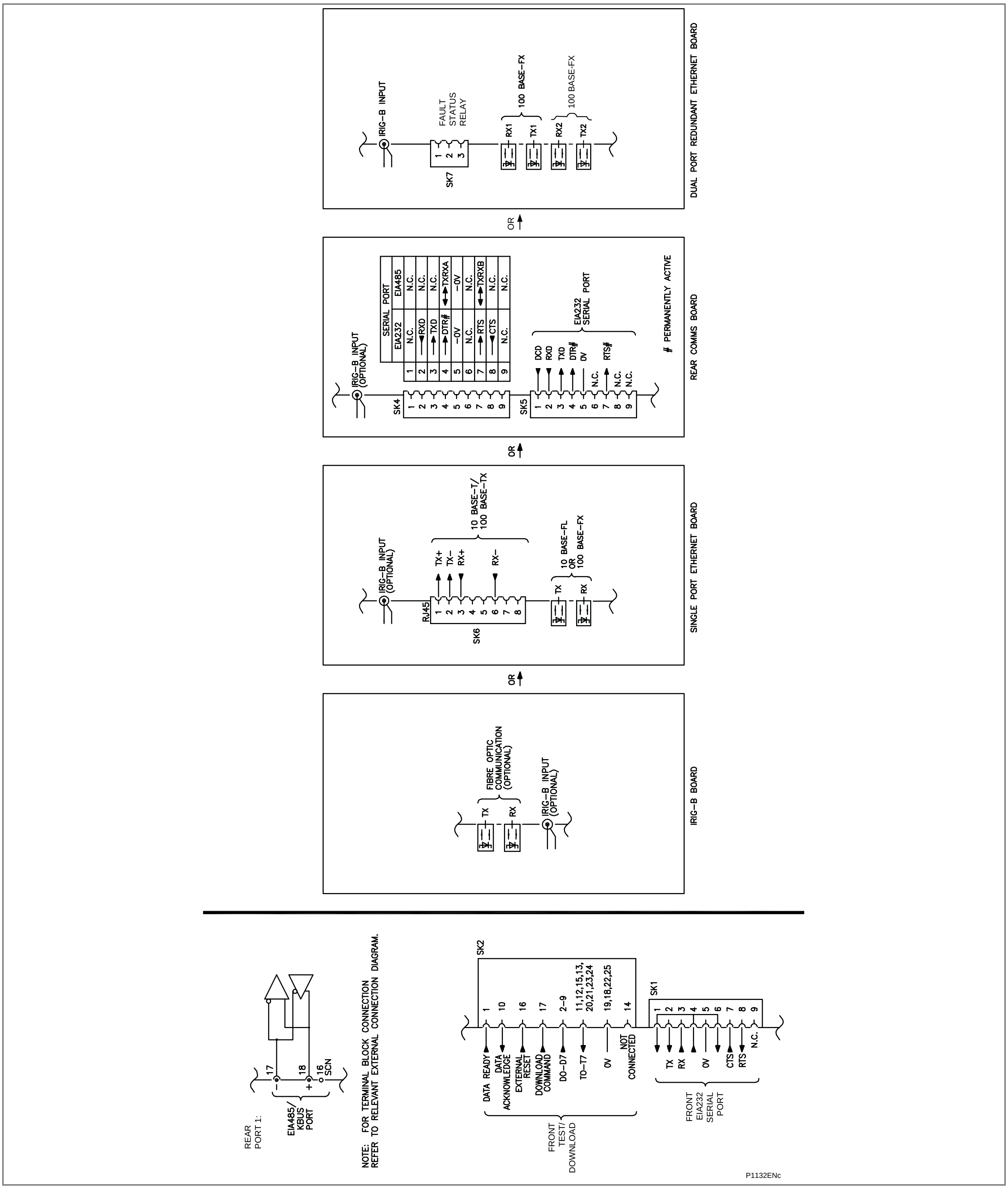

DUAL PORT REDUNDANT ETHERNET BOARD
IRIG–B INPUT
FAULT STATUS RELAY
SK7
1 2 3
RX1
TX1
RX2
TX2
100 BASE–FX
100 BASE-FX
OR
REAR COMMS BOARD
IRIG–B INPUT (OPTIONAL)
SK4
SK5
SERIAL PORT
EIA232
EIA485
N.C.
RXD
TXD
DTR#
–0V
RTS
CTS
TXRXA
TXRXB
EIA232 SERIAL PORT
DCD
RXD
TXD
DTR#
0V
RTS#
N.C.
# PERMANENTLY ACTIVE
SINGLE PORT ETHERNET BOARD
IRIG–B INPUT (OPTIONAL)
RJ45
SK6
TX+
TX–
RX+
RX–
10 BASE–T/ 100 BASE–TX
TX
RX
10 BASE–FL OR 100 BASE–FX
IRIG–B BOARD
FIBRE OPTIC COMMUNICATION (OPTIONAL)
TX
RX
IRIG–B INPUT (OPTIONAL)
REAR PORT 1:
EIA485/ KBUS PORT
17
18
16
SCN
NOTE: FOR TERMINAL BLOCK CONNECTION REFER TO RELEVANT EXTERNAL CONNECTION DIAGRAM.
SK2
1
10
16
17
2–9
11,12,15,13, 20,21,23,24
19,18,22,25
14
DATA READY
DATA ACKNOWLEDGE
EXTERNAL RESET
DOWNLOAD COMMAND
D0–D7
T0–T7
0V
NOT CONNECTED
FRONT TEST/ DOWNLOAD
SK1
1 2 3 4 5 6 7 8 9
TX
RX
0V
CTS
RTS
N.C.
FRONT EIA232 SERIAL PORT
P1132ENc

Figure 21 - Comms options for the MiCOM Px4x platform

PRP NOTES

CHAPTER 18

Date (month/year):	04/2013
Hardware suffix:	See Table 2 for details
Software version:	See Table 2 for details

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1 PARALLEL REDUNDANCY PROTOCOL (PRP) NOTES

1.1 Introduction to PRP

This section gives an introduction to the Parallel Redundancy Protocol (PRP); and how it is implemented on MiCOM-based products manufactured by Schneider Electric.

1.2 Protocols

Industrial real-time Ethernets typically need much better levels of availability and uninterrupted operation than normal office-type Ethernet solutions. For power networks, even a short loss of connectivity may result in a significant loss of functionality or impaired safety. To recover from a network failure, various redundancy schemes have been considered, including: Rapid Spanning Tree Protocol (RSTP), Media Redundancy Protocol (MRP) and Parallel Redundancy Protocol (PRP). The key properties of these are as follows:

RSTP	this uses mesh-based topologies and computes a tree, based on path costs and priorities. In case of network failure, a typical reset time for RSTP-based system is normally a few seconds.
MRP	this uses ring-based topologies. In case of network failure, the network is broken into two separate lines, which are reconnected by de-blocking the previously blocked part. The guaranteed reset time for MRP protocol-based systems is typically around 100ms.
PRP	this does not change the active topology as it uses two independent networks. Each message is replicated and sent over both networks. The first network node to receive it acts on it, with all later copies of the message being discarded. Importantly, these details are controlled by the low-level PRP layer of the network architecture, with the two networks being hidden from the higher level layers. Consequently, PRP-based networks are continuously available.

Power networks need to be able to respond to problems very quickly (typically in less than 10ms), and PRP is the only available protocol which is quick enough to achieve this. The PRP protocol used in the MiCOM relay/IEDs is defined in the IEC62439-3 (2012) standard and is configured using the existing redundant Ethernet card(s).

1.3 PRP Summary (IEC 62439-3 Clause 4)

A summary of the main PRP features is given below:

- Ethernet redundancy method independent of any industrial Ethernet protocol or topology (tree, ring or mesh).
- Seamless switchover and recovery in case of failure, which supports real-time communication.
- Supervises redundancy continuously for better management of network devices.
- Suitable for hot swap - 24 hour/365 day operation in substations.
- Allows the mixing of devices with single and double network attached nodes on the same Local Area Network (LAN).
- Allows laptops and workstations to be connected to the network with standard Ethernet adapters (on double or single attached nodes).
- Particularly suited for substation automation, high-speed drives and transportation.

1.4 Example of a PRP Network

Essentially a PRP network is a pair of similar Local Area Networks (LANs) which can be any topology (tree, ring or mesh). An example of a PRP network is shown in Figure 1:

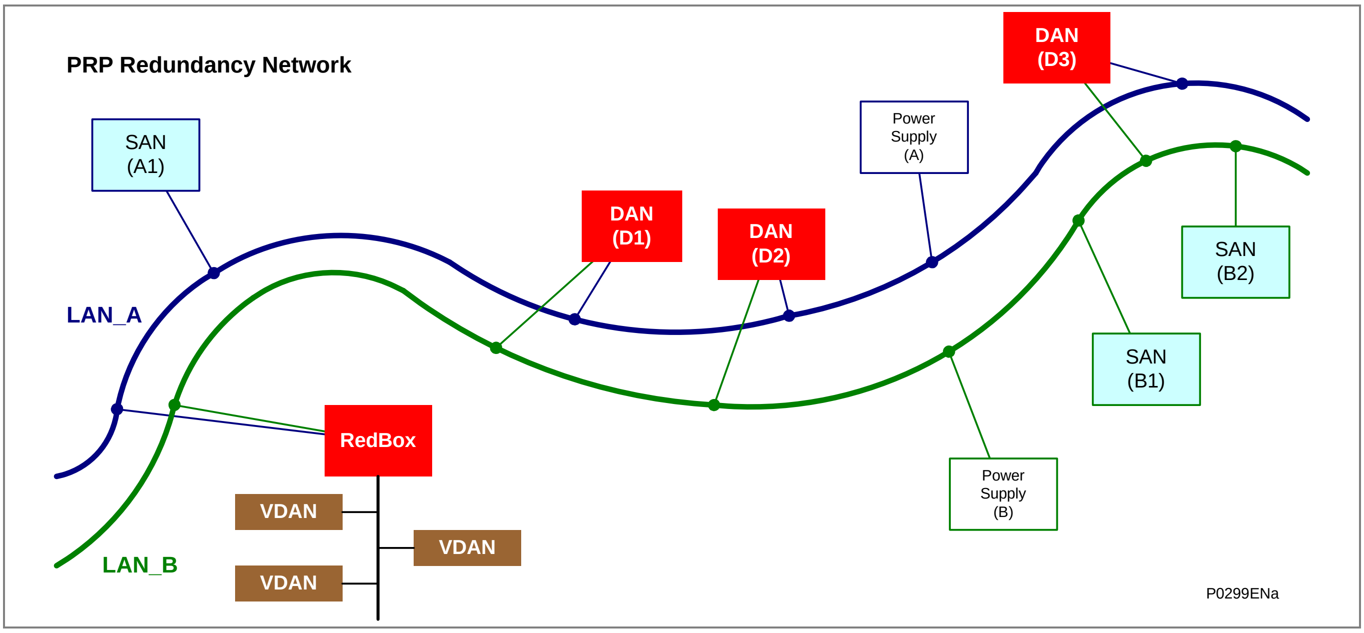

Figure 1 - PRP Redundancy Network

Figure 1 shows two similar Local Area Networks (LANs) which have various Nodes in common. The key features of these networks include:

- With the exception of a RedBox (see below), no direct cable connections can be made between the two LANs.
- Each of these LANs can have one or more Single Attached Nodes (SANs). These are normally non-critical devices that are attached only to a single network. SANs can talk to one another, but only if they are on the same LAN.
- Matched pairs of devices which are critical to the operation of the overall scheme are connected one to each network at single Dual Attached Nodes (DANs).
- To be sure that network messages (also known as frames) are transferred correctly to each device at the DAN, each device must have the same Media Access Control (MAC) code and Internet Protocol (IP) address. This will also mean that TCP/IP traffic will automatically communicate with both of the paired devices, so it will be unaware of any two-layer redundancy or frame duplication issues.
- A Redundancy Box (RedBox) is used when a single interface node has to be connected to both networks. The RedBox can talk to all other nodes. So far as other nodes are concerned, the RedBox behaves like a DAN, so a RedBox is also called a Virtual Doubly Attached Node (VDAN). The RedBox must have its own unique IP address.
- Transmission delays can also be different between related Nodes of the two LANs.
- Each LAN (i.e. LAN_A and LAN_B) must be powered from a different power source and must be failure independent.
- The two LANs can differ in terms of performance and topology, but the Ethernet interface to the relay must be made using an optical fibre connection with an ST connector type. There is no need for an optical interface away from the relay.

1.5 Structure of a DAN

Each DAN has two ports that operate in parallel. They are attached to the upper layers of the communications stack through the Link Redundancy Entity (LRE) as in Figure 2:

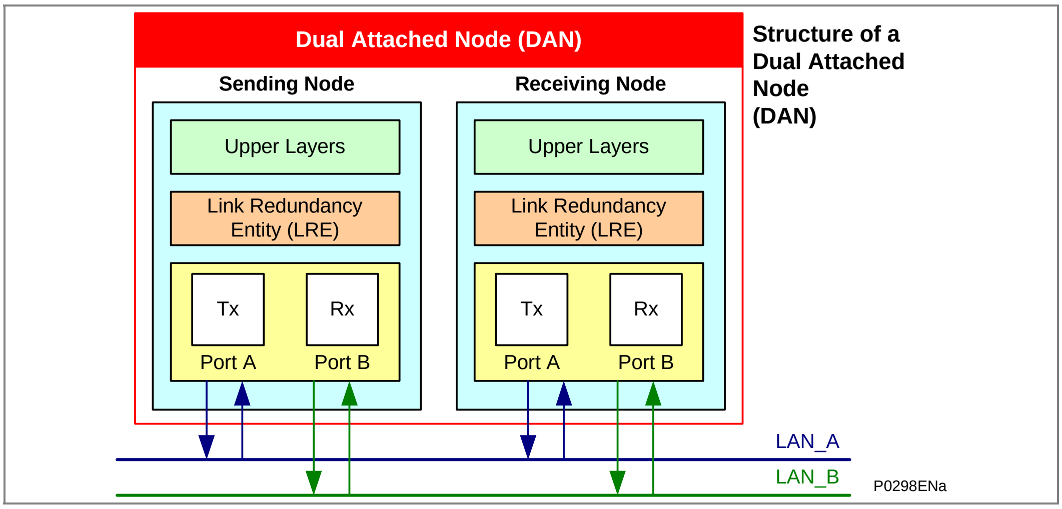
Dual Attached Node (DAN)
Sending Node
Receiving Node
Upper Layers
Link Redundancy Entity (LRE)
Tx
Rx
Port A
Port B
Upper Layers
Link Redundancy Entity (LRE)
Tx
Rx
Port A
Port B
Structure of a Dual Attached Node (DAN)
LAN_A
LAN_B
P0298ENa

Figure 2 - Communication between two DANs

The LRE has two main tasks:

- handling message frames and
- management of redundancy

When an upper layer sends a frame to the LRE, the LRE replicates the frame and sends it through both its ports at nearly the same time. The two frames move through the two LANs with slightly different delays, ideally arriving at the destination node within a small time window.

When receiving frames, the LRE forwards the first frame it received to its upper layers and then discards the duplicate.

As both DAN nodes have the same MAC and IP addresses, this makes redundancy transparent to the upper layers. This allows the Address Resolution Protocol (ARP) to work in the same way as with a SAN. Accordingly, to the upper layers of a DAN, the LRE layer shows the same interface as the network adapter of a non-redundant adapter.

To manage redundancy, the LRE:

- Adds a 32-bit Redundancy Check Tag (RCT) to each frame it sends and
- Removes the RCT from each frame it receives

1.6 Communication between SANs and DANs

A SAN can be connected to any LAN and can communicate with any other SAN or DAN on the same LAN. However, a SAN which connected to one LAN can not communicate directly to a SAN which is connected to the other LAN.

A DAN is connected to both LANs and can communicate with the RedBox or any other DANs or any SANs on either network. For communication purposes, a DAN views the RedBox as a VDAN.

When a SAN generates a basic frame, it sends the frame only onto the LAN to which it is connected.

Originating at the SAN, a typical frame contains these parameters:

• dest_addr	Destination Address
• src_addr	Source Address
• type	Type
• data	
• fcs	Frame Check Sequence (i.e. extra checksum characters added to allow error detection and correction)

The frame from the SAN is then received by the DAN; which sends the frame to its upper layers, which act accordingly.

When a DAN generates a frame, it needs to send the frame onto both of the LANs to which it is connected. When it does this, it extends the frame by adding the 32-bit Redundancy Control Trailer (RCT) into the frame.

The RCT consists of these parameters:

- 16-bit Sequence Number
- 4-bit LAN identifier, 1010 (0xA) for LAN_A and 1011 (0xB) for LAN_B
- 12-bit frame size
- PRP suffix

Note *The Sequence number is a measure of the number of messages which have been sent since the last system reset. Each time the link layer sends a frame to a particular destination the sender increases the sequence number corresponding to that destination and sends the (nearly) identical frames over both LANs.*

Accordingly, originating at the DAN, a typical frame then contains these parameters:

• dest_addr	Destination Address
• src_addr	Source Address
• type	Type
• lsdu	Link Service Data Unit
• Padding	if needed

- RCT data:
    - 16-bit sequence number:
      4-bit LAN identifier

12-bit frame size

- 16-bit PRP suffix (0X88 0XFB)

- fcs Frame Check Sequence

LSDU	*The Link Service Data Unit (LSDU) data allows PRP frames to be distinguished from none-PRP frames.*
Padding	*After the LSDU data, there may be some data padding. This is added to frames which would otherwise be too short for conventional network traffic (minimum frame size is 64 octets).*
Size	*The frame size will vary depending on the contents of the frame and how it has been tagged by the various SANs and DANs. In VLANs, frame tags may be added or removed during transit through a switch. To make the length field independent of tagging, only the LSDU and the RCT are considered in the size.*

Figure 3 shows the frame types with different types of data.

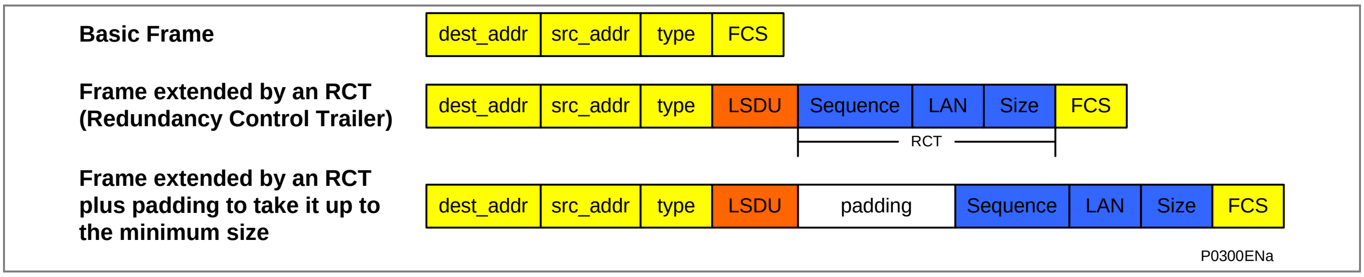
Basic Frame
dest_addr
src_addr
type
FCS
Frame extended by an RCT (Redundancy Control Trailer)
dest_addr
src_addr
type
LSDU
Sequence
LAN
Size
FCS
RCT
Frame extended by an RCT plus padding to take it up to the minimum size
dest_addr
src_addr
type
LSDU
padding
Sequence
LAN
Size
FCS
P0300ENa

Figure 3 - Frames without and with RCT and padding

The key points about these differing frame structures is that:

- SANs do not implement any redundancy features, so they generate basic frames which SANs and DANs can understand.
- SANs can still understand the frames that come from DANs, as SANs ignore the RCT components in frames which come from DANs (a SAN can not distinguish the RCT from the IEEE802.3 padding)
- If a DAN receives a frame which does not include the RCT component, it sends a single copy of the frame to its upper layers.
- If a DAN receives a frame which does include the RCT component, it does not send a duplicate copy of the frame to its upper layers.
- If a DANP can not identify that the remote Node is a DAN, it inserts no RCT.

Rejection Algorithm

A Nodes table maintains a list of all the Nodes (SANs and DANs) on each network. This table is used by the rejection algorithm to assess the possibility of frames being duplicates and for network integrity monitoring. The table maintains a list of all the sequence numbers so it can keep track of the frames which have been sent.

For every node on BOTH networks, the table also maintains:

- The expected next sequence number (so it can establish whether messages are not being received or are being received in an incorrect order)
- Message counts to show how many messages have been received
- Error counts to show whether frames were received out-of-order or were not received or were sent/received on the incorrect LAN

- A time field to keep track of when a frame was last received from the node
- An indicator to track whether the node is a SAN or not

The receiver scans the frames starting from the end and uses the algorithm to analyse the frames it has already received and the various data included in the current frame. The algorithm then combines the frame data with the information in the Nodes table to decide whether the frame is the first one it has received, or whether it is a candidate for rejection.

1.7 PRP Technical Data

- One VLAN tag supported.
- 128 VDANs supported.
- Up to 100Mbit/s full duplex Ethernet.
- Dynamic frame memory allocation (page manager).
- Configurable duplicate detection.
- Wishbone interface for configuration and status registers.
- CPU port interface - Ethernet or Wishbone.
- Support for link-local protocols - CPU may send to specific ports only - CPU knows receive port.
- Configurable frame memory and queue length.
- Duplicate detection with configurable size and aging time.
- MAC address filtering (8 filter masks for interlink, 6 for CPU).
- Support for interfaces with or without Ethernet preamble.

2 PRP AND MICOM FUNCTIONS

2.1 MiCOM Products and PRP

The PRP functions being introduced as part of the overall MiCOM product range provide additional functionality, which is backwards compatible with existing Schneider Electric MiCOM equipment. This means that existing MiCOM relays/IEDS can be used on networks which use PRP functions, with no changes being made to those relays/IEDs.

The new MiCOM products that use the PRP, will interrogate other equipment to determine the equipment model number, and then use the model number to decide (at runtime), whether that particular item of equipment can support PRP or not.

The model number to denote PRP functionality uses the Digit 7 Hardware option. This is shown in Table 1:

Hardware Option	Type	Example Model Number
“N” at digit number 7	Modulated PRP board	P14221**N**A6M0440J
“P” at digit number 7	Unmodulated PRP board	P14221**P**A6M0440J

Table 1 - MiCOM model numbers for PRP options

The MiCOM relay/IED firmware has been modified to allow the PRP options to be accepted for the power-up tests in addition to the implementation of the supervision frame transmission.

2.2 Planned PRP Product Releases

To clarify the dependency between the new firmware and the hardware option for PRP, the PRP feature is normally associated with a major firmware release. The planned releases are shown in Table 2 below:

Relay	SW	HW	Previous Platform	Released Platform
P141	46 (cyber)	J	M2.3	M2.5
P142 *	46 (cyber)	J	M2.3	M2.5
P143 *	46 (cyber)	J	M2.3	M2.5
P144	46 (cyber)	J	M2.3	M2.5
P145	46 (cyber)	J	M2.3	M2.5
P741 P743	51	K	L4.6	L4.10 without Lx_NO_ctse10045
P742	51	J	L4.6	L4.10 without Lx_NO_ctse10045
P746	02	K	K4.8	L4.10
P642	04 (cyber)		L6.4	L6.5
P643 *	04 (cyber)		L6.4	L6.5
P645	04 (cyber)		L6.4	L6.5
P543 *	C0/D0 (cyber)		M4.x	M4.2
P544	C0/D0 (cyber)		M4.x	M4.2
P545	C0/D0 (cyber)		M4.x	M4.2
P546 *	C0/D0 (cyber)		M4.x	M4.2
P547	D0 (cyber)		M4.x	M4.2
P443	D0 (cyber)		M4.x	M4.2

Relay	SW	HW	Previous Platform	Released Platform
P445	F0 (cyber)		M4.x	M4.2
P446	D0 (cyber)		M4.x	M4.2
P841A	C0/D0 (cyber)		M4.x	M4.2
P841B	C0/D0 (cyber)		M4.x	M4.2
P441 P442 P444	C7	J	M3.1	M3.2
P442 P444	D6	K	L5.4 + NCIT	L5.7 + NCIT
P34x				
P443	B0		L7.x	
P445	E0		L7.x	
P446	B0		L7.x	
P543	A0/B0		L7.x	
P544	A0/B0		L7.x	
P545	A0/B0		L7.x	
P546	A0/B0		L7.x	
P547	B0		L7.x	
P642	04		L6.4	L6.5
P643	04		L6.4	L6.5
P645	04		L6.4	L6.5
P841A	A0		L7.x	
P841B	B0		L7.x	
P849	A0A			
P241	C7	J	L3.1_a	L4.10
P242 P243	C7	K	L3.1_a	L4.10

Table 2 - MiCOM relay/IED Models which will support PRP

The MiCOM relay/IED cortec shows that the Hardware options identified in Table 1 are only available with the new firmware version.

2.3 MiCOM S1 Studio Software

The addition of the PRP feature has no impact of the MiCOM S1 Studio support files so there is no need to upgrade any MiCOM S1 Studio software.

2.4 MiCOM Relay Configuration

There is no need to change the configuration of any relay (as relays which include support for PRP will be able to recognize other devices which support PRP).

2.5 Firmware Changes

2.5.1 Main Card

The relay main card has only a minimal change for the implementation of the PRP Protocol. The change required is to recognize the two new hardware options (see Table 1) during the power up tests. For the two new options, the relay firmware will verify the presence of the Ethernet card. The relay firmware will not be able to differentiate between the PRP and non-PRP variants of the Ethernet card; as the only difference between them is a different FPGA.

2.5.2 Ethernet Card

An extension to the Ethernet board software is needed to support the transmission of the PRP supervision frame. To keep the same number of released software executables this feature is integrated into the standard software with the transmission of the supervision frame being controlled by the IED/relay model number.

2.6 Hardware Changes

The PRP protocol is implemented using the existing dual redundant Ethernet card as a starting point. The PRP Frame management is achieved by re-programming the Field-Programmable Gate Array (FPGA).

The low-level management of the redundant frames is performed within the FPGA; this being defined as the Link Redundancy Entity (LRE). This will involve the addition of the Redundancy Check Tag (RCT) to a frame to be transmitted; this identifies the LAN and the sequence number of the message over the two networks. The FPGA is also responsible for the stripping of the RCT from received frames and discarding the duplicated messages such that only a single application frame is received by the Ethernet processor.

The LRE functionality of the supervision frame transmission is performed by the Ethernet processor card.

The new version of the dual redundant Ethernet card is based on the ZN0071 part 007, but has a new part number of 2072082 (Part 9 for the modulated IRIG-B option and Part 10 for the Unmodulated IRIG-B option).

Warning **The main feature of PRP is a high level of network availability due to the presence of two LANs. The dual redundant Ethernet card provides watchdog contacts to show a link failure on either of the dual redundant Ethernet interfaces. To use this feature effectively, it is very strongly recommended that the watchdog contacts are connected to the supervision system.**

2.7 PRP Parameters

The Redundant Ethernet standard (IEC 62439-3:2011/FDIS A) defines several parameters for the PRP protocol; these being fixed at a default value within this release. The following values are set:

Parameter	Value	Description
Supervision Frame Multicast Address	01-15-4E-00-01-00	Target MAC Address for multicast supervision frame
Life Check Interval	2 seconds	Period between transmission of supervision frames
PRP Mode	Duplicate Discard	This is normal PRP mode, Duplicate address will not be supported.
Node Forget Time	60 s	
Entry Forget Time	400 ms	Duration that the received message Sequence number will be held to discard a duplicate message.
Node Reboot Interval	500ms	Duration following reboot for which no PRP frames should be transmitted.

Table 3 - PRP parameter values (for PRP Protocol Version 1)

2.8 Product Requirements

Here is a list of the main Product Requirements for MiCOM products which support PRP:

- The MiCOM relay/IED provides two redundant Ethernet ports using PRP.
- Redundancy protocols other than PRP (e.g. RSTP and MRP) are not implemented within this project.
- The MiCOM relay/IED must be connected to the redundant Ethernet network as a Double Attached Node (DAN) using PRP (DAN using PRP is known as DANP)
- The redundant Ethernet interface must be made using an optical fibre connection with an ST connector type.
- The management of the PRP redundancy is transparent to the application data provided via the Ethernet interface.
- The PRP option is available with any of the existing protocol options via the Ethernet Interface (IEC61850, DNP3.0)
- Loss of one of the LAN connections to the device does not cause any loss or degradation to the Application data over the Ethernet interface.
- The redundant Ethernet card provides watchdog contacts to show a link failure on either of the redundant Ethernet interfaces.
- The link fail alarm within the MiCOM relay/IED firmware can not detect the failure of the link on the redundant Ethernet interface.
- The MiCOM relay/IED supports the transmission of the PRP Supervision frame at a fixed time period (LifeCheckInterval) of 2s (+/- 100ms)
- The Media Access (MAC) Address for the two physical Ethernet interfaces must be the same and is defined by the MAC address for the Ethernet card (this is set during manufacturing).
- Each supervision frame includes a sequence number as defined in the IEC 62439-3:2011/FDIS specification. This will be incremented for each supervision message and the value will start from zero following a system restart.
- The IP address for the two physical Ethernet interfaces must be the same and will normally be defined using the MiCOM S1 Studio tool.
- The MiCOM relay/IED will not process received supervision frames to provide supervision of the redundant network.
- The MiCOM relay/IED does not provide for the PRP management to be configured (via either the MiCOM relay/IED HMI or the Ethernet interface). Accordingly, the default values (as defined within this document) are used for all PRP parameters.
- The performance of the Ethernet Interface is not degraded by using the PRP interface.
- We are stating that the PRP interface of the Px40 relay will support up to 32 connected DANP nodes. Note that the maximum number of connected DANP nodes is dependent on the memory size inside the FPGA which is used to manage the messages from each DANP mode and reject duplicates.

2.8.1 Abbreviations and Acronyms

Abbreviations / Acronyms	Meaning
CRC	Cyclic Redundancy Check
DAN	Dual Attached Nodes
DANP	Double Attached Node implementing PRP
FPGA	Field-Programmable Gate Array
HMI	Human Machine Interface
IED	Intelligent Electronic Devices
IP	Internet Protocol
LAN	Local Area Network
LRE	Link Redundancy Entity
MAC	Media Access Control
MRP	Media Redundancy Protocol
PRP	Parallel Redundancy Protocol
RCT	Redundancy Check Tag
RedBox	Redundancy Box
RSTP	Rapid Spanning Tree Protocol
SAN	Singly Attached Node
TCP	Transmission Control Protocol
VDAN	Virtual Doubly Attached Node

Notes:

VERSION HISTORY

CHAPTER NO 19

Date:	12/2013
Hardware Suffix:	J (P642) K (P643/P645)
Software Version:	04
Connection Diagrams:	10P642xx (xx = 1 to 5) 10P643xx (xx = 1 to 6) 10P645xx (xx = 1 to 9)

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Notes:

1 SOFTWARE AND HARDWARE VERSION CHANGES

Software version		Hardware suffix	Original date of issue	Description of changes	MiCOM S1 compatibility	Technical documentation
Major	Minor					
01	B	K	Oct. 2008	Original Issue for P643.	V2.14 V3.0	P64x/EN M/A11
01	D	J/K	Feb. 2009	Original Issue for P642/P645. The REF algorithm was enhanced, so that it can be applied in 1.5 breakers arrangements. The scaling factor used by the REF element is the right one. In the P643, the item “TV” is invisible from the options of the cell “Monit’d winding” when “Winding Config” is set to “HV+LV”. The REF fault record is independent from the Diff fault record. If the Diff is disabled, but the REF is enabled; the REF fault record is available. Is-CTS setting is invisible when CTS is disabled or in indication mode. The settings I>Inhibit and I2>Inhibit in the VTS function are in pu. PSL positional data extraction facility has been included.	V2.14 V3.0	P64x/EN AD/A21
02	B	J/K	April 2009	The differential and bias currents of the low impedance REF and differential functions are included in the disturbance recorder. The frequency measurement is included in the disturbance recorder. DNP3.0 over Ethernet. IEC-61850 Phases 2.0 and 2.1 are included. High-break contacts are included depending on the cortec option. An option to disable the VTS logic is included. Enhancement of the VTS logic.	V2.14 V3.0	P64x/EN M/A32
02	C	J/K	October 2009	Through fault monitoring function has been amended. The I2t calculation only starts when the current is above TF I> Trigger level and no differential element (87 or 64) has started. Date and time settings have been amended. The settings associated to UTC or SNTP have been included. In the default settings the circuitry fault alarm has been disabled since it is only intended for busbar protection. The cross blocking function has been enabled. A 100 ms dwell timer has been added to the fault record trigger input in the PSL to avoid triggering the trip led without generating a fault record when testing the relay. The dependency between the settings in simple and advanced mode has been improved. The relay recalls the settings (reactance, Is-HS1, Zero seq. Filt HV, Zero seq. Filt LV, Zero seq. Filt TV, HV Grounding, LV Grounding, and TV Grounding) when changing from simple to advanced mode and vice-versa. The setting cell 2nd harm blocked has been included. It can be set as either enabled or disabled. This is required in busbar applications where the second harmonic blocking is not needed. If the setting cell TOL status is disabled, Hot Spot T and Top Oil T measurements are not displayed. The setting cells Ambient T and Top Oil T can only be set to RTD or CLIO when the hardware is available. The thermal overload function has been improved. The DDB signal TFR De-energized and a corrected top oil time constant have been included. The CT para mismatch logic has been modified. If the amplitude matching factor of the TV winding is out of range and less than 0.05, the TV winding CT inputs are not considered in the differential calculation (under this condition the CT para mismatch alarm is not asserted and the differential is not automatically blocked).	V2.14 V3.1.1	P64x/EN M/A32

Software version		Hardware suffix	Original date of issue	Description of changes	MiCOM S1 compatibility	Technical document-ation
Major	Minor					
02	D	J/K	March 2010	It was reported that for P642 model, when 02C software with IEC61850 protocol was downloaded, an alarm was issued, indicating that NIC software miss-matched the main board software. This issue has been solved in 02D firmware. The latched states of relays or LEDs reflect the current properties of the individual relays and LEDs. The relays and LEDs are updated whenever their properties are changed, i.e. reset when their properties are not latch. IEC61850, the DDBs values that had not changed since startup are also reported. Integrity Period of X seconds results in Integrity reports being generated every X+1 seconds, hence an extra second is being added to the configured Integrity Period. IEC61850, the appropriate amendments were performed so that when the Integrity Period is set to “x” seconds the Integrity report is generated every “x” seconds and not “x+1” seconds. NIC no response alarm assertion has been amended. DNP3, the relay failure to respond to a class 1/2/3 poll following a confirmation to another relay has been corrected.	V2.14 V3.1.1	P64x/EN M/A32
02	E	J/K	October 2010	The appropriate amendments have been done to avoid displaying 1/25 of the injected power in 'MEASUREMENTS 2' column. DNP3.0 over Ethernet, appropriate amendments have been done so that when polling an offline analogue signal, the flag “Offline, Local forced” is displayed. Appropriate amendments have been done so that the menu text for setting "% Reactance” is displayed correctly in MiCOM Studio. The DNP3.0 over Ethernet application stack size has been enlarged to avoid asserting the error code 0X662005F8. IEC61850, the buffer has been enlarged to avoid loss of communication under heavy BRCB (buffer report circuit breaker). Note 02E firmware is only available for the P643.	V2.14 V3.1.1	P64x/EN M/A32
02	U	J/K	Feb 2011	Firmware rebranded from Areva to Schneider Electric.	V2.14 V3.1.1	P64x/EN M/A32
02	V	J/K		Support Dual Redundant Ethernet Board. Resolve the CT Ratio mismatch problem at LV and TV windings.	V2.14 V3.1.1	
02	W	J/K			V2.14 V3.1.1	
03	A	J/K	Not available (May 2011)	Cybersecurity Phase 1 has been included, for Software 03 only (i.e. not 01, 02 or 04). This is described only in the Cyber Security chapter. REB (Redundant Ethernet Board) has been included. Note Improvements in 02E for P643 were included in 03A for all P64x models.	V2.14 V3.1.1	P64x/EN M/A32
03	A	J/K	January 2011	Service Manual rebranded from Areva to Schneider Electric.	V2.14 V3.1.1	P64x/EN M/A42
03	U	J/K		Rebranded 03A		
03	V	J/K	May 2013	Parallel Redundancy Protocol (PRP) support: The IEC62439-3 (2012) PRP states “Each Double attached node implementing PRP (DANP) stall multicast a PRP_Supervision frame over both its ports”. Bug fixes.	V2.14 V3.1.1	P64x/EN M/A62

Software version		Hardware suffix	Original date of issue	Description of changes	MiCOM S1 compatibility	Technical document-ation
Major	Minor					
04	U	J/K	May 2011	Software 04 does not include cyber security. CT saturation and no gap detection algorithms have been included algorithm to improve the differential element operating time. External fault detection algorithm has been included to prevent the CT saturation and no gap detection from blocking the 2nd harmonic element during external faults. CT input exclusion. If a CT input is excluded, then it is not considered by any of the current based functions. The CBF logic has been modified so that it resets in less than a cycle. Also the settings are per current transformer input. A setting for the neutral current has also been included. User alarms have been included and improved. 32 user alarms are available and they can be set in the setting files as self reset or latch. The label for each user alarm can be set in the setting file (no need to use the text editor). This label is also displayed in the PSL. Two voltage controlled overcurrent stages are available. All the current based functions are now settable; they are no longer fixed as HV, LV and TV. For example, there are three overcurrent elements (four stages each one). Any of the overcurrent elements can be set to protect a particular winding or a feeder. Assigned inputs extension, the selection of CT inputs for each winding has been increased. Now all the possible combinations are considered. For example, in a P645 four CT inputs can be assigned to the HV side and one to the LV side. High impedance REF has been included. Low impedance REF for autotransformer has been included.	V2.14 V3.1.1	P64x/EN M/A52
04	U	J/K	May 2011	Software 04 does not include cyber security. Negative sequence overvoltage has been implemented. The thermal overload function has been enhanced; four cooling modes have been included. The two first stages of the negative phase sequence overcurrent element can be set as IDMT. An additional VT input can be ordered in the P642. As a result voltage functions and directional functions are available to some extent. The first two stages of the negative phase sequence overcurrent element can be set as IDMT. REB (Redundant Ethernet Board) is available. An additional VT input can be ordered in the P642. As a result negative phase sequence overvoltage function and directional functions are available to some extent. **Note** Improvements in 02E for P643 were included in 04U for all P64x models.	V2.14 V3.1.1	P64x/EN M/A52
04	V	J/K	December 2011	Updated the Px4x software platform which has improved the GOOSE performance. Bug fixes.	V2.14 V3.4.1	P64x/EN M/A52
04	W	J/K	June 2012	The GOOSE performance improvements that implemented in the old Platform will be modified in order to provide a better solution. The modification will be included in a new platform. Bug fixes.	V2.14 V3.4.1	P64x/EN M/B52
04	X	J/K	May 2013	Parallel Redundancy Protocol (PRP) support: The IEC62439-3 (2012) PRP states “Each Double attached node implementing PRP (DANP) stall multicast a PRP_Supervision frame over both its ports”. Bug fixes.	V2.14 V3.5.2	P64x/EN M/A62

Table 1 - Software and hardware version changes

2 SETTING FILE AND RELAY SOFTWARE VERSION

Setting File Software Version	Relay Software Version			
	01	02	03	04
01	✓			
02		✓		
03				
04				✓

Table 2 - Setting file and relay software version

3 PSL FILE AND RELAY SOFTWARE VERSIONS

PSL File Software Version	Relay Software Version			
	01	02	03	04
01	✓			
02		✓		
03			✓	
04				✓

Table 3 - PSL file and relay software versions

4 MENU TEXT FILE AND RELAY SOFTWARE VERSIONS

Menu Text File Software Version	Relay Software Version			
	01	02	03	04
01	✓			
02		✓		
03			✓	
04				✓

Table 4 - Menu text file and relay software versions

Customer Care Centre

http://www.schneider-electric.com/CCC

Schneider Electric
35 rue Joseph Monier
92506 Rueil-Malmaison
FRANCE

Phone: +33 (0) 1 41 29 70 00
Fax: +33 (0) 1 41 29 71 00

www.schneider-electric.com

Publisher: Schneider Electric

Publication: P64x/EN M/A62 Software Version: 04 Hardware Suffix: J (P642) & K (P643/P645)

02/2014

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